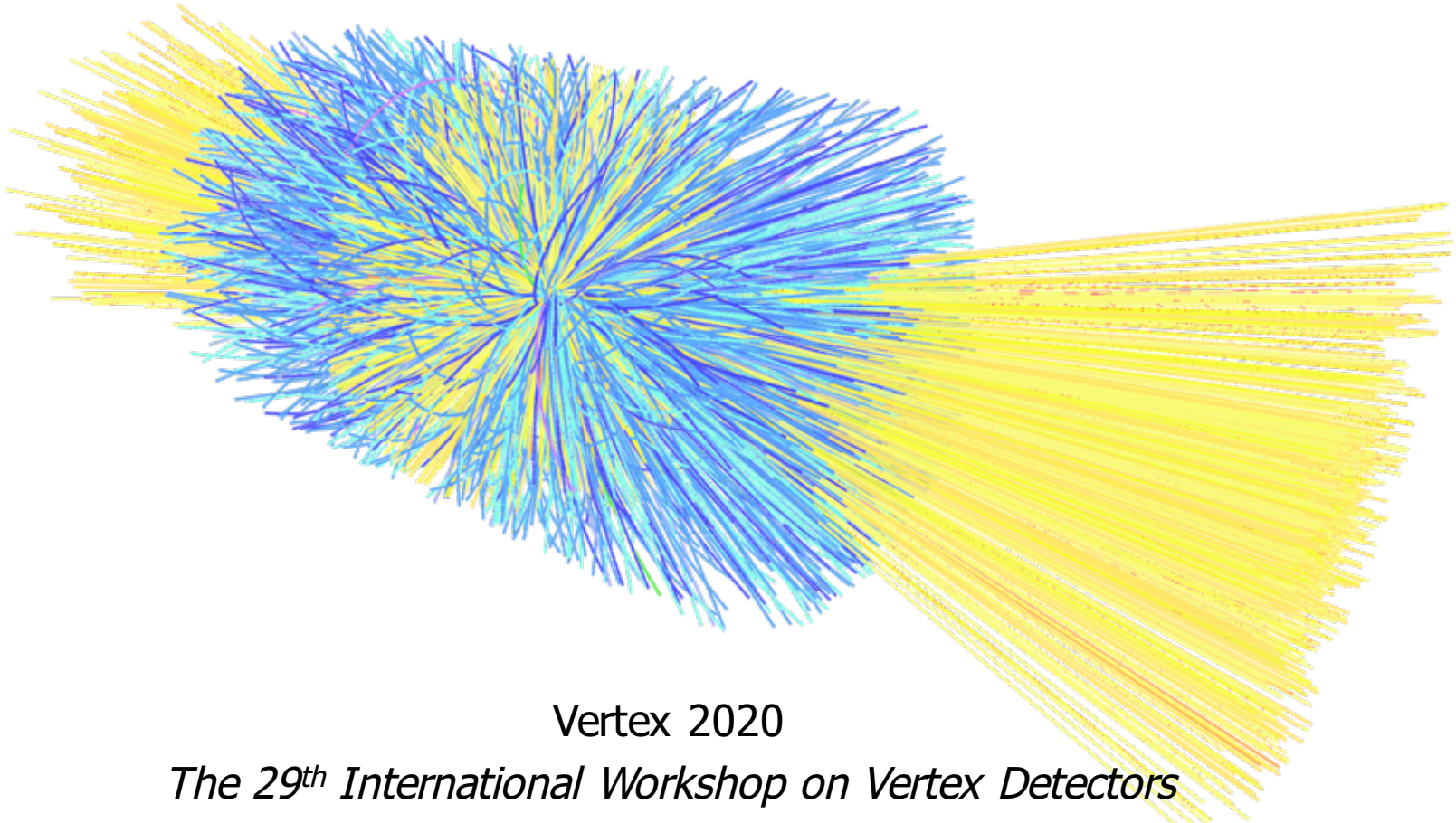
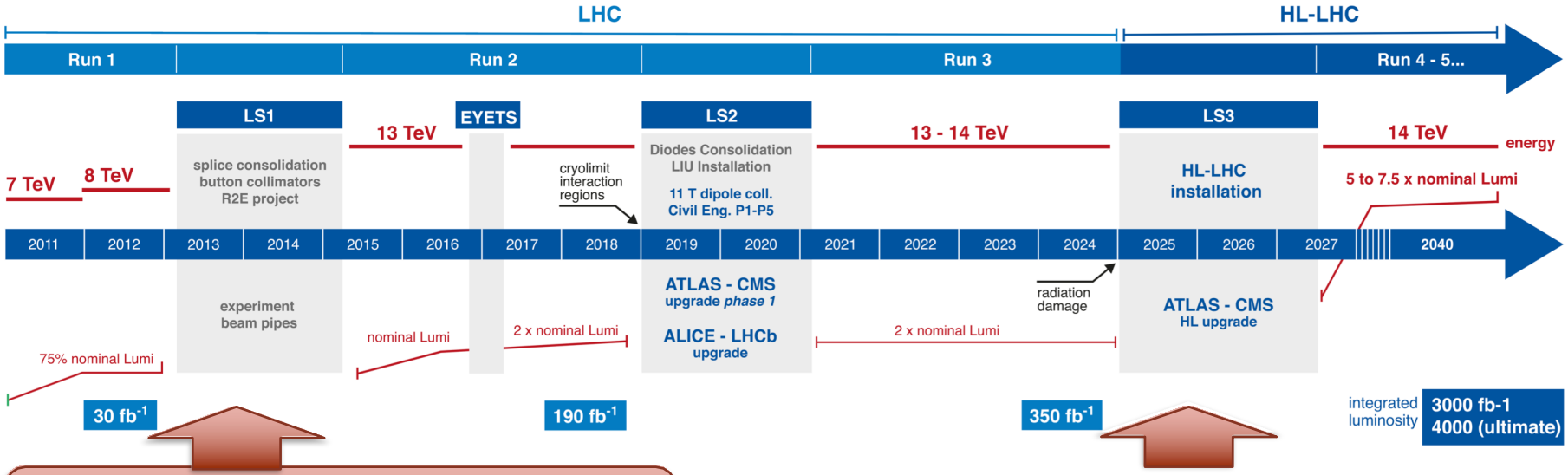
The ATLAS ITk detector for HL-LHC

C. Gemme, INFN Genova /CERN
on behalf of the ATLAS ITk Collaboration



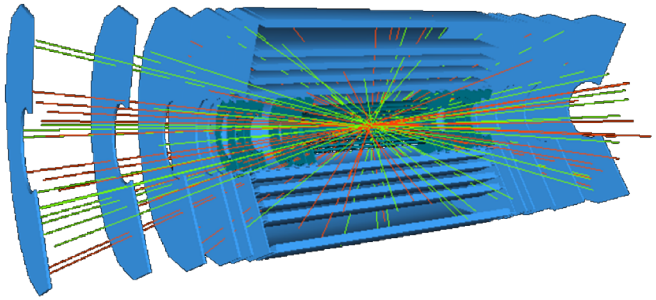
Vertex 2020
The 29th International Workshop on Vertex Detectors

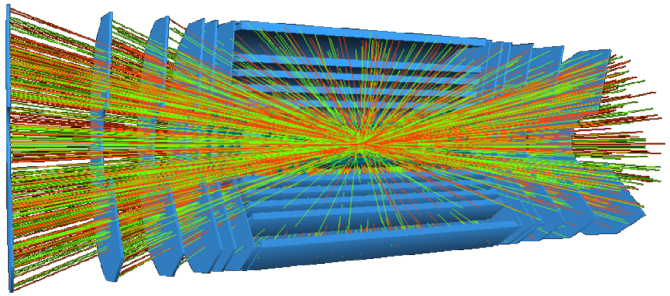
LHC Upgrade



Inner Detector (ID): Pixel+Strip+TRT upgraded by IBL

"Phase II": full inner detector replacement (Pixel+Strip)





LHC

19 - 55 Pile-up events

High Luminosity LHC (HL-LHC)

140-200 Pile-up events

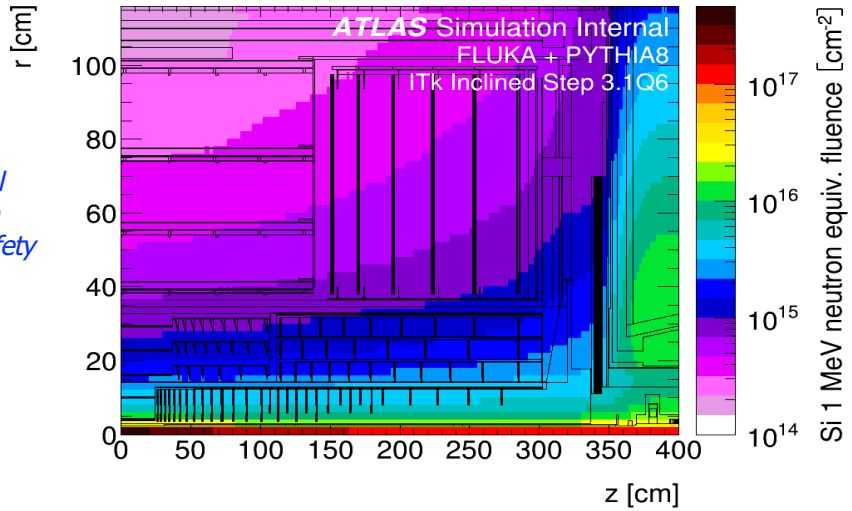
ATLAS ITk

Limitations of the current tracker

- ✓ HL-LHC scenario implies significant scaling of the ID design parameters:
  - *Peak luminosity:* 5-7 x 10^{34} $cm^{-2}s^{-1}$ → ~x5-7
  - *Average pile-up:* up to <μ> ~200 → ~x8
  - *Integrated luminosity:* 4000 fb^{-1} → ~x10
  - Requested *radiation hardness: up to* 2x10^{16} n_{eq}/cm^2 → x20

High particle fluences up to
- *1.2*10^{16} n_{eq}/cm^2 for pixel*
- *1.6*10^{15} n_{eq}/cm^2 for strip*

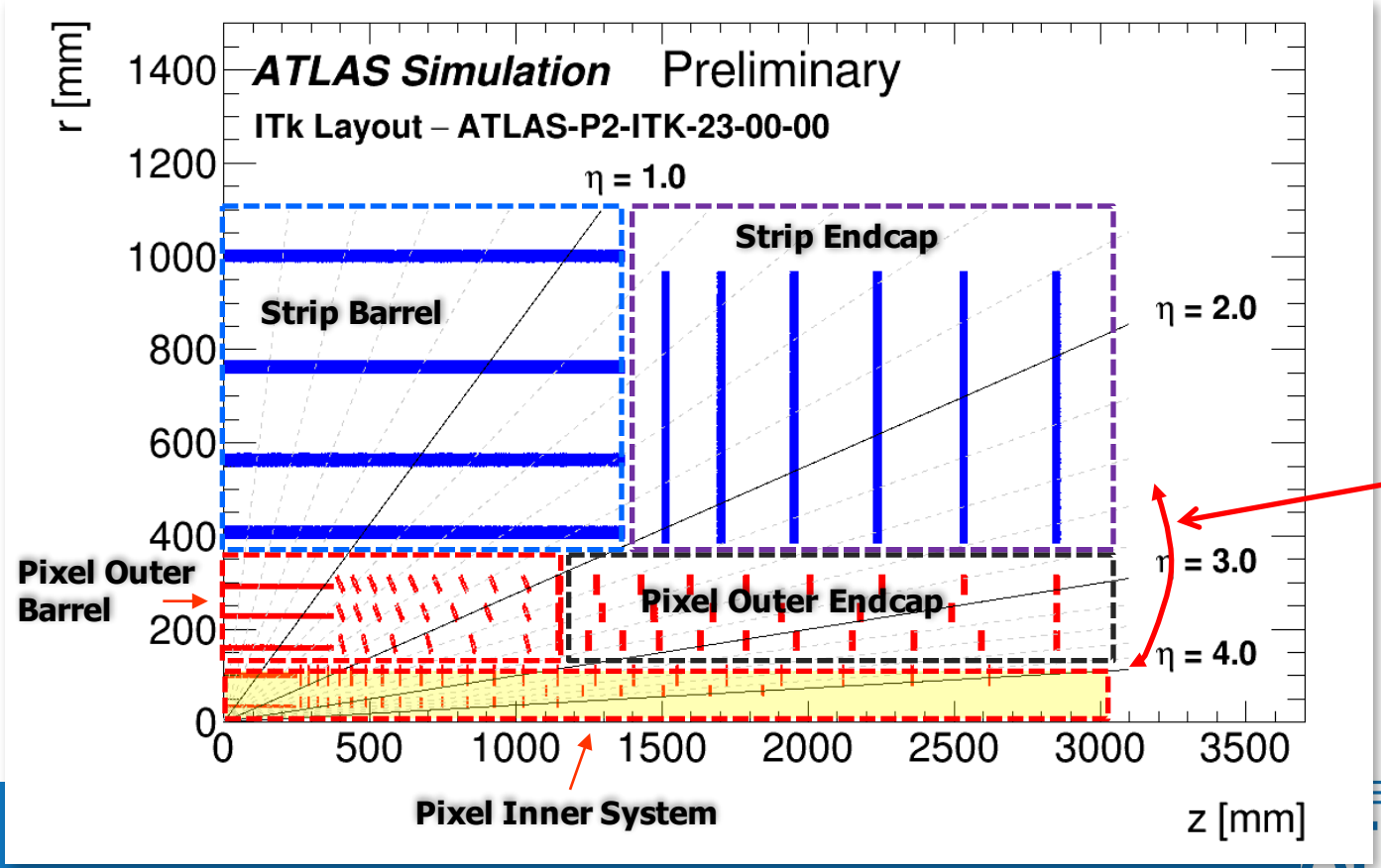
Requested Additional 1.5 Safety factor.



- ✓ Requirements for the new tracker:
  - **Similar or better performance** than the ID in these harsher conditions.

Layout of the ITk detector

- ✓ All-silicon detector in 2T magnetic field.
  - Strip subsystem covering up to $|\eta|$ <2.7 with 4 Barrel layers 6 End-cap disks
  - Pixel subsystem covering up to $|\eta|$ <4.0 with 5 Barrel layers + endcap rings
  - Possibility to replace the two innermost pixel layers
  - In Jan, Updated the Innermost layer radius finalized at 34/33 mm (B/EC, was 39/36)

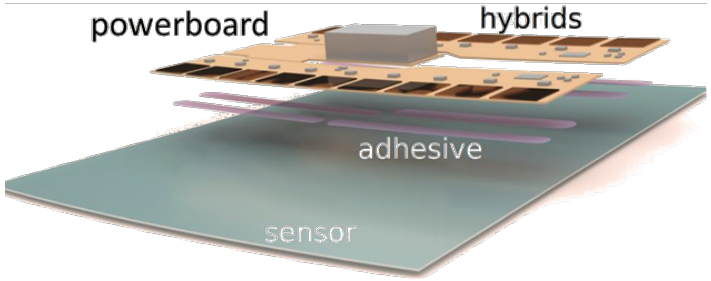


ITk Modularity

	Surface [m²]	# Channels	# modules
Pixel	13	5.1 G	9.2 k
Strip	165	60 M	18 k

Large Strip system compared to current SCT system in Run 2

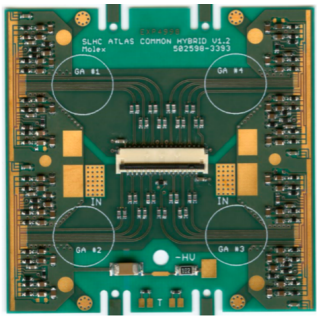
- ~10x channels,
- ~3x size,
- ~5x modules

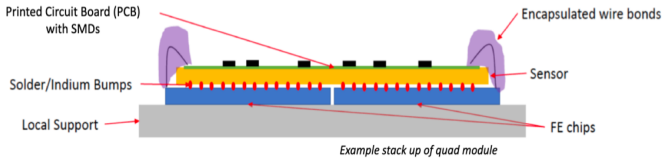


Modules loaded on Local supports: Barrel Stave or Endcap Petals

Large Pixel system compared to current pixel in Run 2

- ~60x channels,
- ~7x size,
- ~5x modules

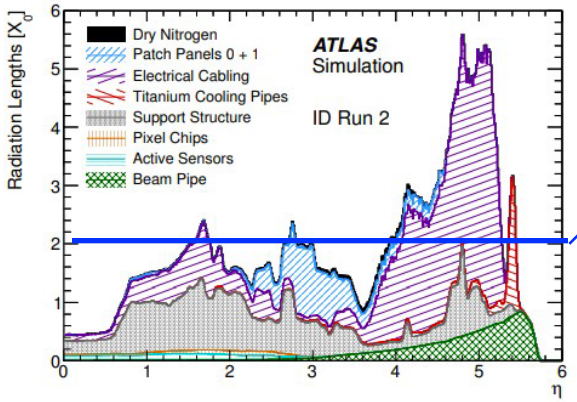




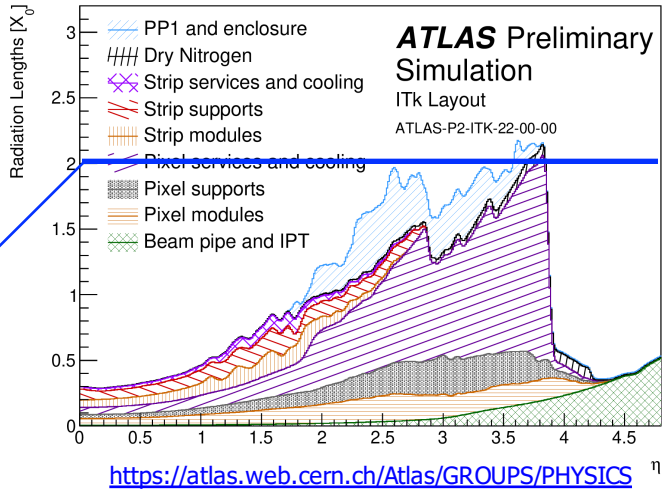
Modules loaded on different structures according to the subsystem

Material Budget

- ✓ With the increased surface and granularity wrt ID, X_0 mitigation thanks to:
  - Strip: DC-DC powering and data transmission with optical links and lpGBT
  - Pixel: Thinned sensors and FE, Serial powering, inclined region in the Outer Barrel, increased readout speed
  - Common (ITK and Strip): Light structures, cooling designs optimized as well as material choice wrt the requirements (precision, stability, contain the thermal run away, …)
  - *NB: Material budget is regularly updated as the engineering design evolves*



https://atlas.web.cern.ch/Atlas/GROUPS/PHYSICS/UPGRADE/CERN-LHCC-2017-021/



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Reduced material budget versus current ID in Run 2.

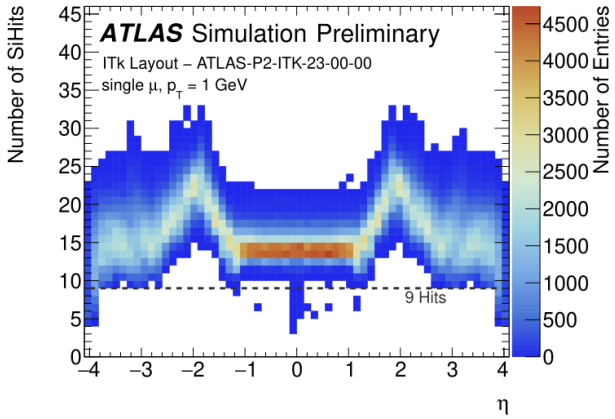
→ Minimize effects of multiple-scattering and energy losses before outer detectors.

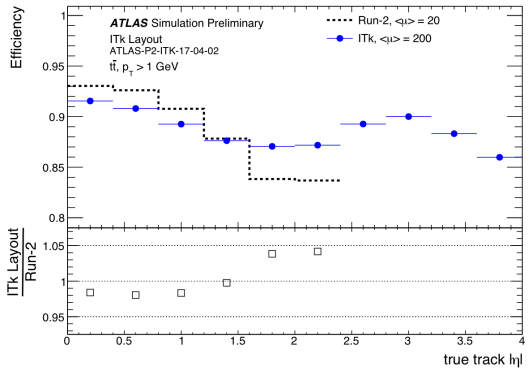
Tracking Performance

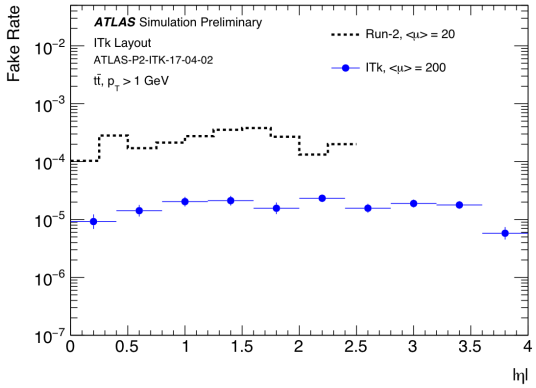
- ✓ ITk layout designed to guarantee **hermetic** coverage within $|\eta| < 4$
  - Provides at least **9 hits** for all particles with $p_T > 1$ GeV within $|z_{vertex}| < 150$ mm
    - Allows for **tighter track selections** without compromising reconstruction efficiency
  - Maintain **efficiencies over 85%** up to $|\eta| < 4$, comparable to Run2 ID at $<\mu> = 20$
  - Improves the **fake rate over Run2 ID,** even considering a 10x increase in pile-up.

Overall significant improvement thanks to
- Reduced material budget → minimize material interactions
- Increase in overall hit counts → tighter track selection
- Improved hermeticity ➔ more hits, fewer holes

https://atlas.web.cern.ch/Atlas/GROUPS/PHYSICS/PLOTS/ITK-2020-002





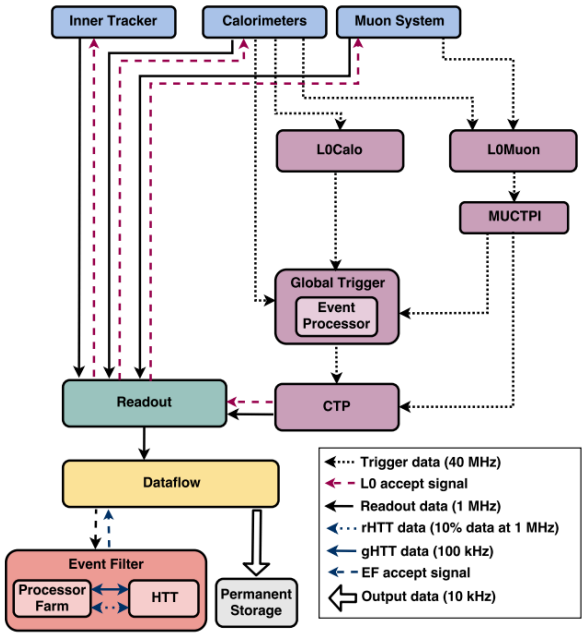


https://atlas.web.cern.ch/Atlas/GROUPS/PHYSICS/PLOTS/IDTR-2019-009/

Trigger and ITk: Baseline vs Evolved Scenarios

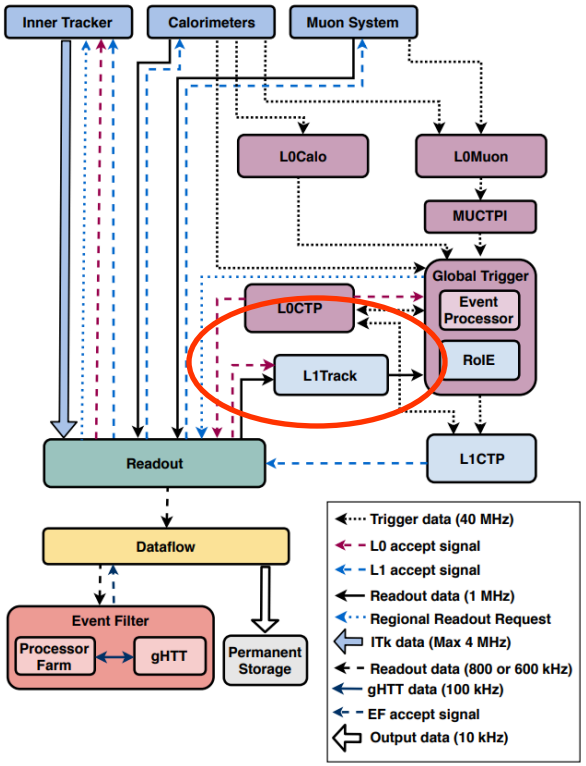
TDRs in 2018 have supported a *baseline L0-only* capable of operation at 1 MHz, with all hooks necessary to implement an *evolved L0+L1* system at a later stage with up to 4 MHz Level-0 rate capability.

L0-only



L0-only with operation at 1 MHz; very similar to current ATLAS L1/EF trigger configuration

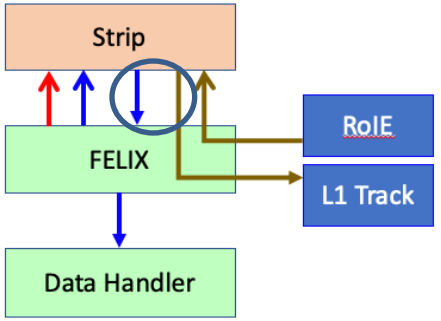
Evolved L0/L1



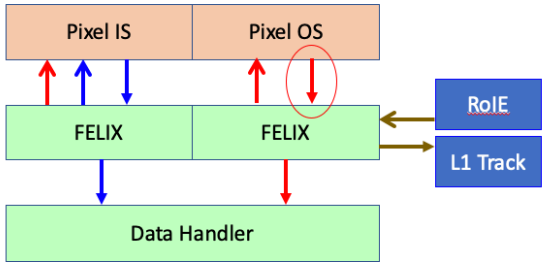
L0/L1 up to 4 MHz Level-0 rate capability, Level 1 rate refined ***by tracker information*** *at ~600-800 kHz*

Trigger and ITk: post-TDR

- ✓ In the TDR, ITk contributes to the L1A decision:
  - with Region of Interest for the full **Strip** detector
  - with full events from the **Pixel** Outer System



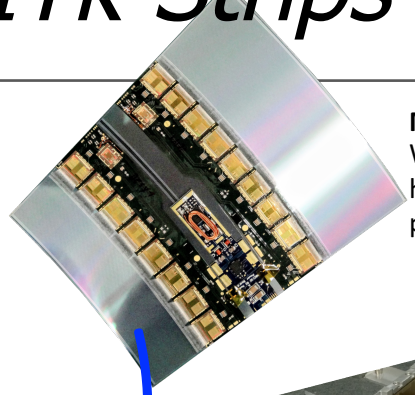
- ✓ More recently, several complications emerged in the solutions allowing the Pixel layers to be read out at 4 MHz:
  - → ATLAS decision in June 2020 that Pixel implements the services for an **effective maximum readout rate of 1 MHz**.



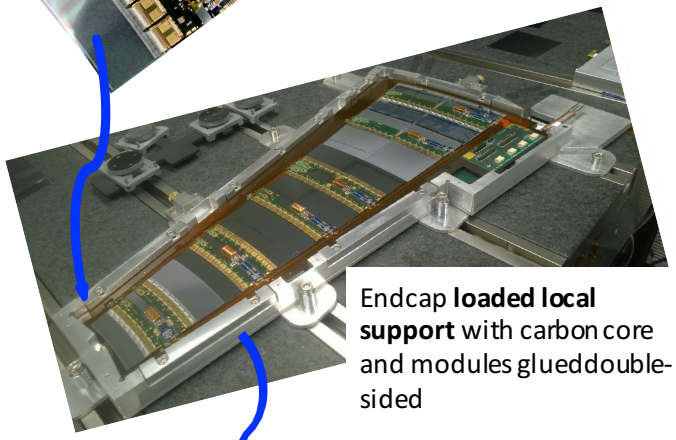
- ✓ Currently under general discussion in ATLAS if to maintain the evolved trigger scenario: Decision in mid-October.

Moving to construction: ITk Strips

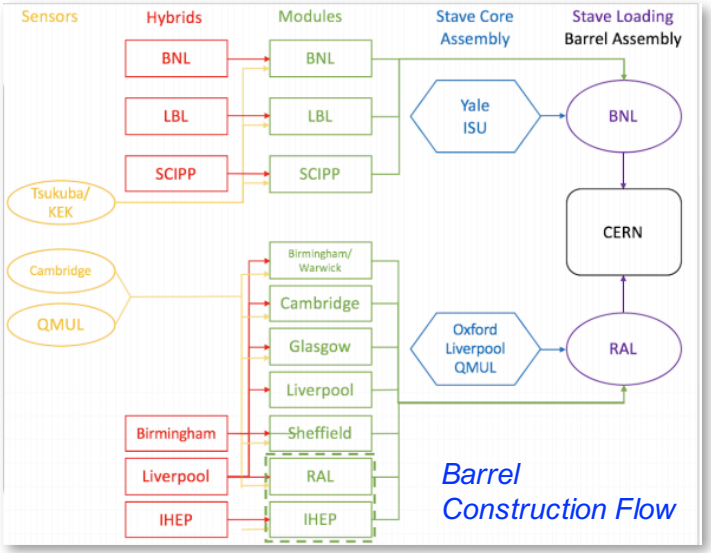
- ✓ Concept of modularity of components which are designed for manufacturability and mass production from the beginning (industry standard design rules, simplified construction,…)
  - Assembly and testing at multiple sites
  - Simplifies final assembly
  - Earlier test of full system

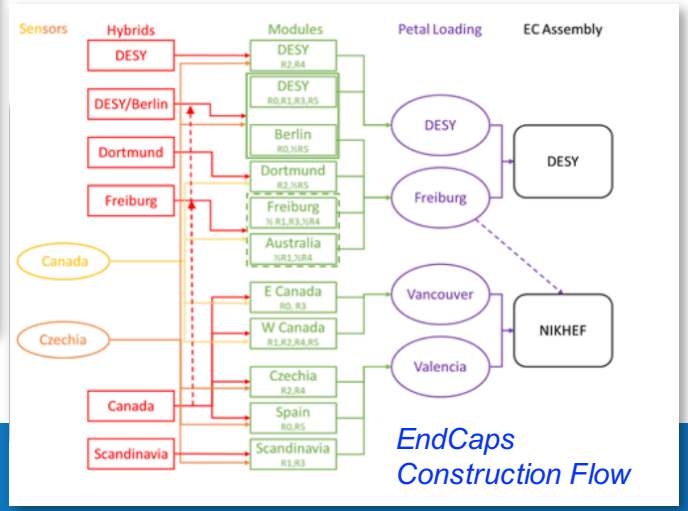


Module (endcap R0)
With FE chips, sensor and hybrid (DC-DC converter, power board, HCC chip)

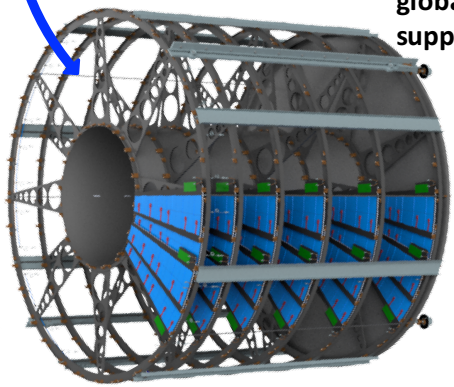


Endcap **loaded local support** with carbon core and modules glueddouble-sided



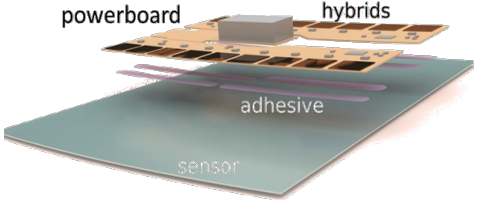


Endcap global support



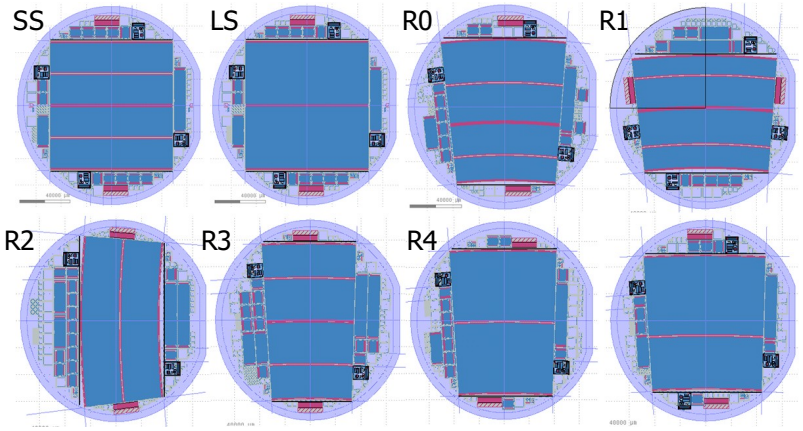
ATLAS ITk

Strip Sensors

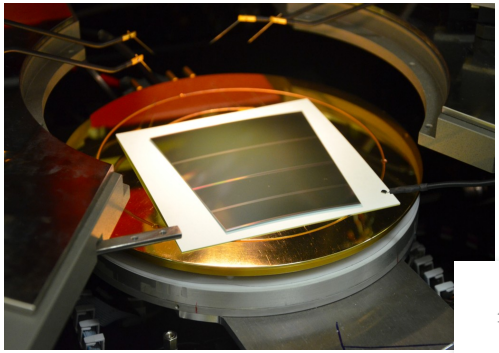


- n-in-p float-zone sensors with p-stop isolation,
- ~320 µm thickness
- 8 different sensor types (2 barrel, 6 end-cap)

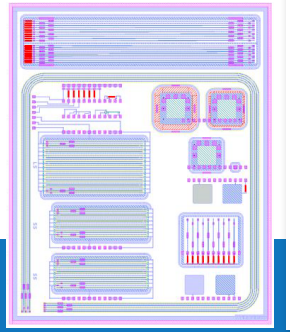
8 pre-production masks

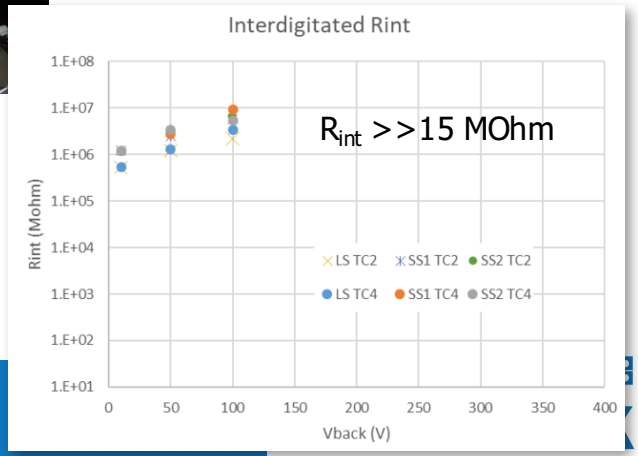


- ✓ Sensor produced by HPK.
- ✓ All of pre-production has been delivered including all EC sensor types.
  - Mini sensors and other test structures on each wafer. First test results are as expected from new Test Chip structures
- ✓ Qualification of sites on going.

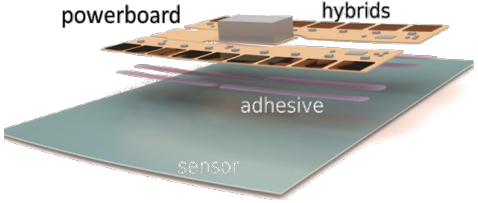


New Test Structures





Strip Readout FE Electronics



- **Hybrids:** Hosts Binary readout chip ABCStar, Hybrid controller chip HCCStar. 13 (EC) + 2 (Barrel) designs.
- **Power board:** Hosts monitor and control AMACStar, DC-DC converter and HV filter and switch. 4 (EC) + 1 (Barrel) designs.

https://arxiv.org/pdf/2009.03197

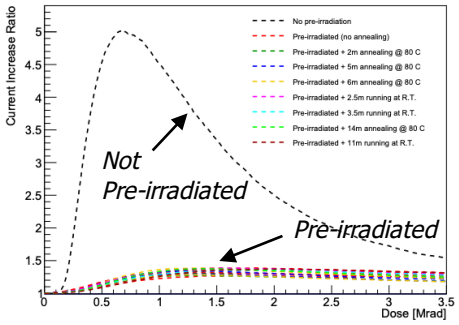
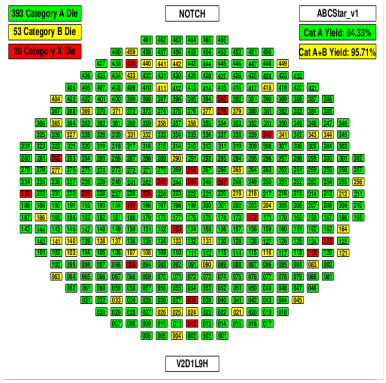


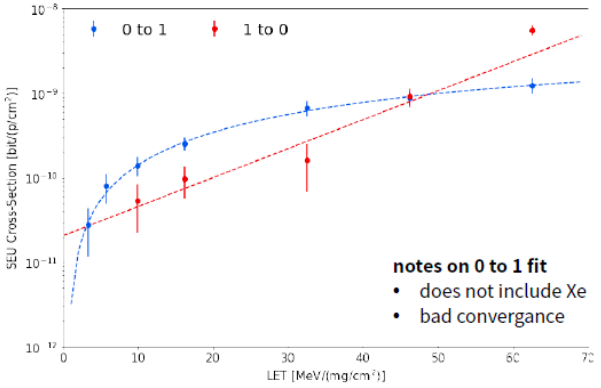
Figure 66: Comparison of current increase for un-pre-irradiated and pre-irradiated ASICs with various annealing processes carried out - chips were either left unpowered in an oven at 80 °C or powered and read-out constantly at room temperature. Independent of the annealing applied, pre-irradiated ASICs showed a current increase of less than 50 % - significantly less than the primary TID bump. Results are shown for multiple ASICs at each annealing option and all chips were taken from the same wafer.

- ✓ Pre-irradiation of ASICs baselined.
- ✓ Significant redesign required for measured SEE and potential SET effects of prototype chips.
  - Pre-production ABCStar/AMACStar design completed, and ASICs submitted. ABCstar back: Wafers probing development proceeding at DA (Canada) and RAL. Launched last week!
  - Significant work still required for HCCStar→ running into space constraints while adding necessary SEE mitigation.

ABCstar wafer probing Preproduction



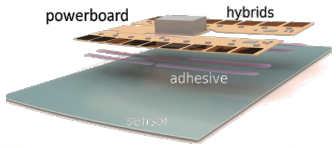
AMAC SEE test

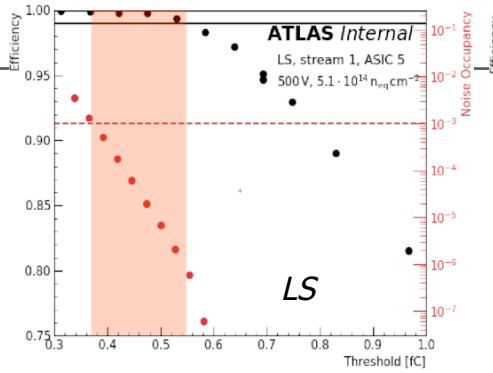


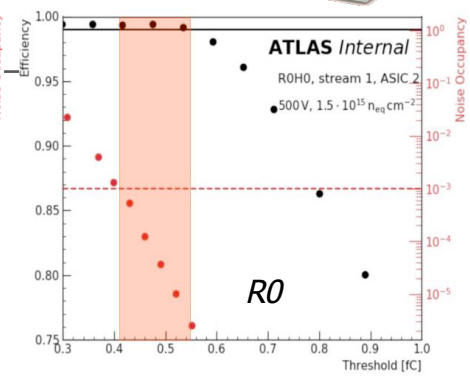
ATLAS ITk

Strip Modules

- Efficiency
- Noise Occupancy



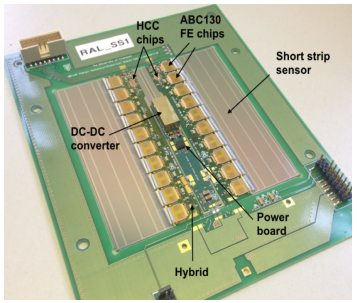




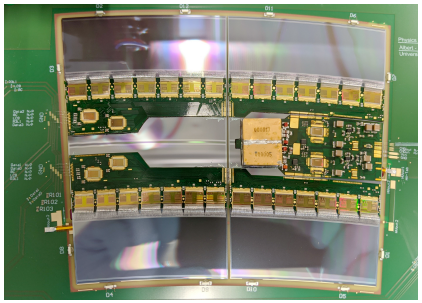
- ✓ Successful campaigns at DESY-II test beam facility of irradiated modules to the end-of-life
  - First results show clear operating windows meeting >99% efficiency, <0.1% noise occupancy requirement

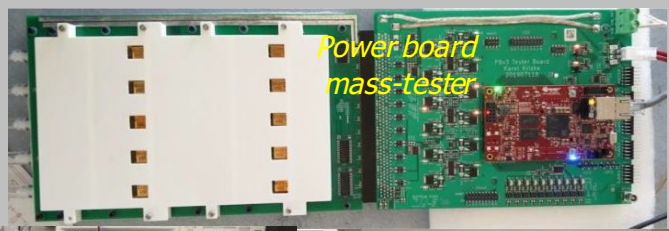
- ✓ Final Design Review for modules **passed** in September '19.
- ✓ Mass testers for power boards, hybrid burn-in and module thermal cycling all being rolled out
- ✓ Next big milestone is start of pre-production and site qualification.
  - Delayed by pre-production ASICs availability and COVID
  - Partially using prototypes chips, moving to preproduction ones as soon as available.

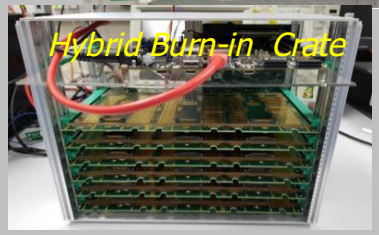
Barrel module

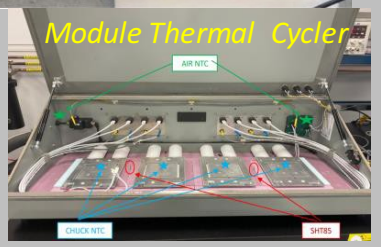


EndCap module

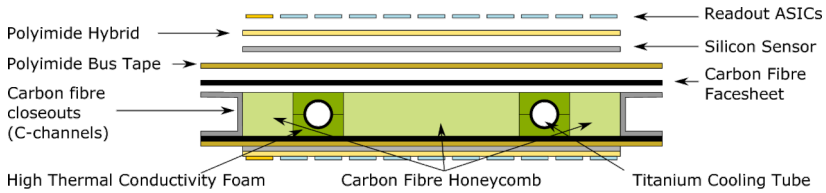




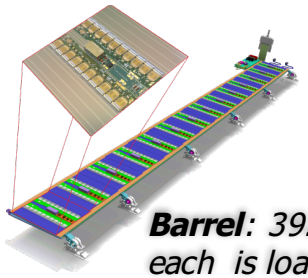




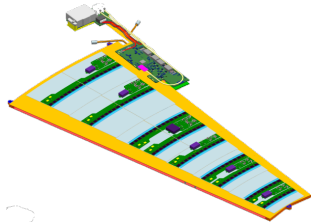
Strip Local Supports



- **Carbon-fibre composite structures** with co-cured copper **bus tapes** have **modules** glued on top of both sides with a stereo angle between them.
- Polyimide bus tapes for data, clock, command and power between modules and end-of-structure cards (EoS).
- EoS cards service the lpGBT and VTRX+ links to the outside world.

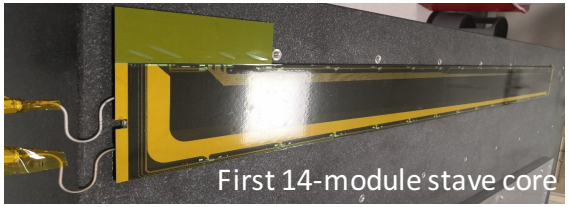


***Barrel**: 392 Staves, each is loaded with 28 modules. Length ~140 cm*

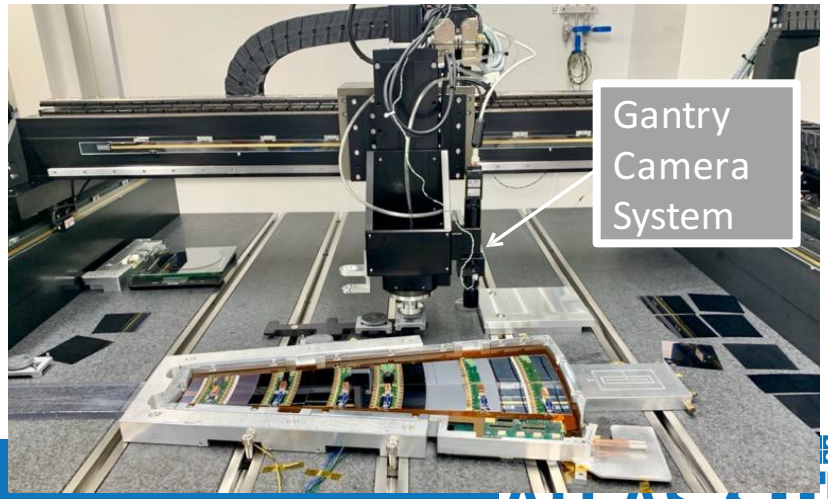


***Endcap**: 384 Petals, each is loaded with 18 modules. Length ~60 cm*

✓ Cores and the EoS are nearing pre-production.



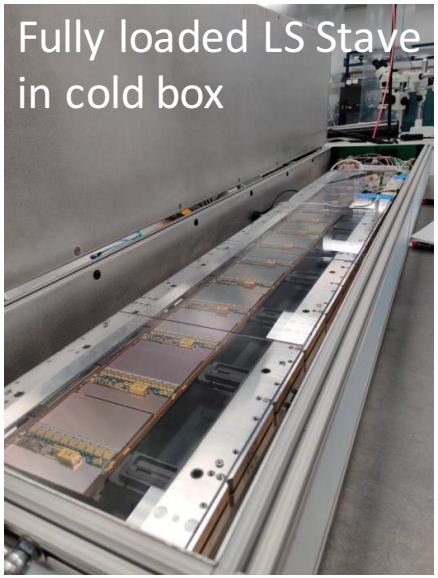
- Loading of modules to better than 40 μm accuracy with gantry systems.
- Tests include thermo-mechanical studies, stress tests and thermal cycling. Electrical test.



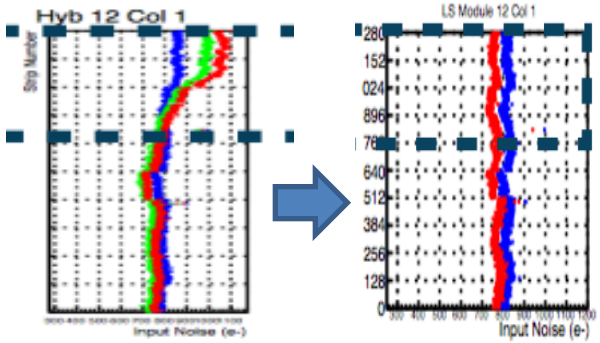
Strip System Test of loaded local supports

- ✓ Three large scale demonstrators were made to be ready for pre-production:
  - 14 Power Board Stave: Demonstrated multi-drop communication between AMAC/lpGBT
  - 5 SS Stave Segment: Demonstrated multi-drop command/clock between lpGBT and HCC/modules
  - Full LS stave: demonstrated master-slave Eos, noise performance warm T
    - Revealed an **unforeseen temperature dependence of noise**

- ✓ Further tests of LS stave confirm removing the AC-reference for the return of common mode in high speed signals removes the enhanced noise at cold temperatures:
  - As cold noise effect unexpected, test fully-electrical petal (DESY/FREIBURG), SS stave (RAL), LS stave (BNL). Further testing underway to explore other referencing options to use on SS/petals if required
  - LS bus tapes released for preproduction



Noise vs channel, one module on LS w/ and w/o AC-reference (Feb 2020)



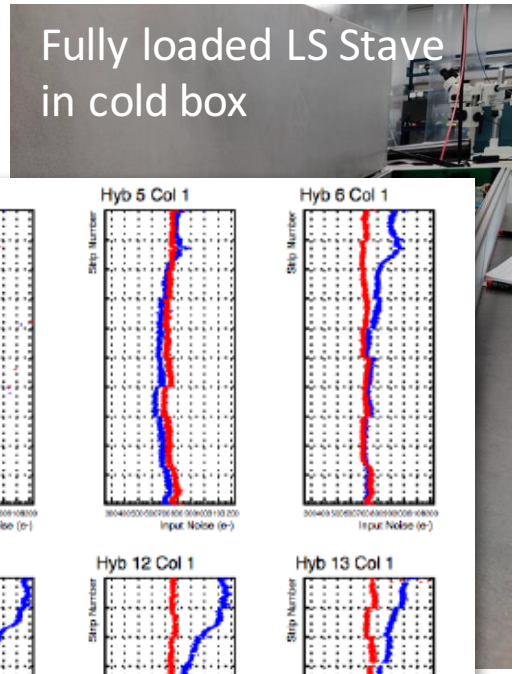
Chiller Set Point at -50°C,-40°C, 20°C

Strip System Test of loaded local supports

- ✓ Three large
  made to be
  - 14 Power E
    communic
  - 5 SS Stave
    command/
  - Full LS stav
    performan
    - Reve
      depe

- ✓ Further tes
  removing th
  return of cc
  speed signa
  noise at col
  - As cold n
    electrical
    (RAL), LS
    underway to explore other referencing options to use on SS/petals if required
  - LS bus tapes released for preproduction

LS stave 14 modules
Test at operation temperature
- February 2020 ACGND bond on
- August 2020 AVGND bond off



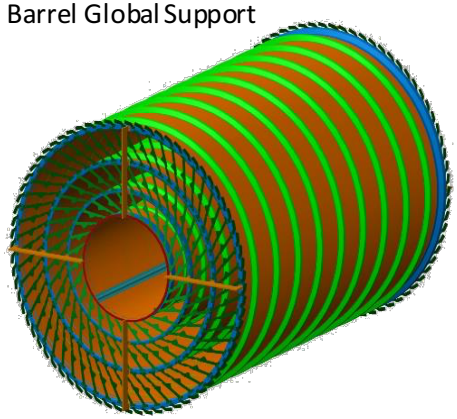
Chiller Set Point at -50°C,-40°C, 20°C

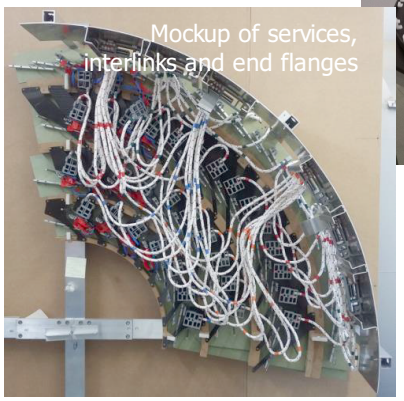
ATLAS ITk

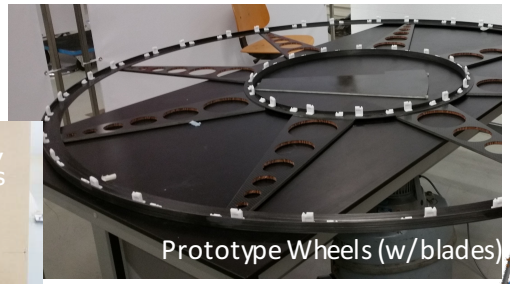
Strip Global Mechanics

- ✓ **Production review in Dec 2019, Production was delayed by ~6 months for fire safety concerns**
  - Materials have been tested and some modified to reduce the flammability of the global supports.
  - Orders for both systems have been launched.
- ✓ Due to COVID, both parts are delayed by availability of the carbon fiber and prices have increased.

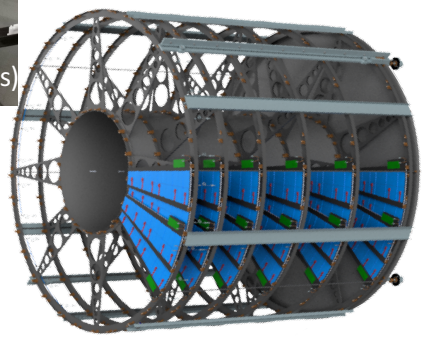
Barrel Global Support







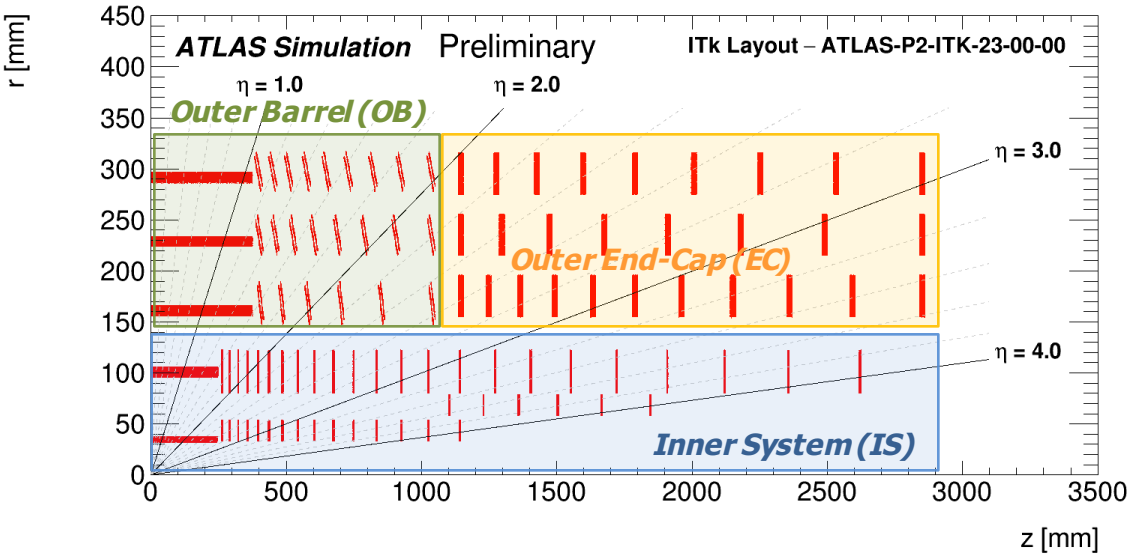
End-cap GlobalSupport



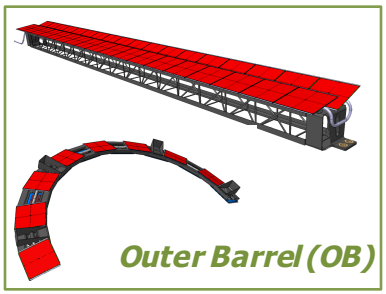
- Loaded local support structures (staves and petals) are end insertable including cooling and cabling.
- For barrel: carbon cylinders for each layer in which staves are inserted.
- For endcaps: carbon wheels with blades for each disk mounted in endcap structure.

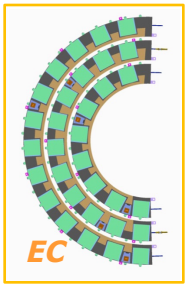
ATLAS ITk

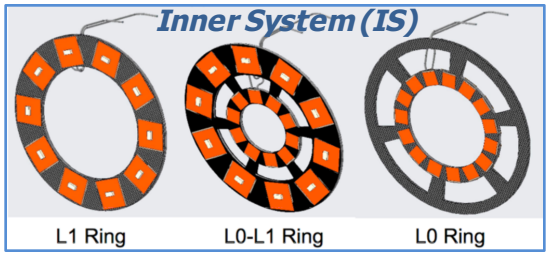
ITk Pixel Overview



Local supports in ...

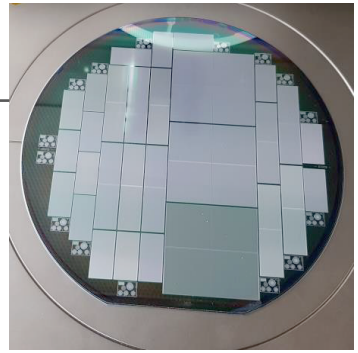






Layer	Sensor Type	Thickn. [µm]	Sensor Size [µm²]	Module Type	Module installed	Replace-ment	Fluence w/ SF [1e15 n_{eq}/cm²]
L0 barrel	3D n-in-p	150	25x100 1E	Triplet	288	Yes	18
L0 rings	3D n-in-p	150	50x50 1E	Triplet	900	Yes	18
L1	Planar n-in-p	100	50x50	Quad	1160	Yes	4
L2-4	Planar n-in-p	150	50x50	Quad	6816	No	4-1

Pixel Planars sensors

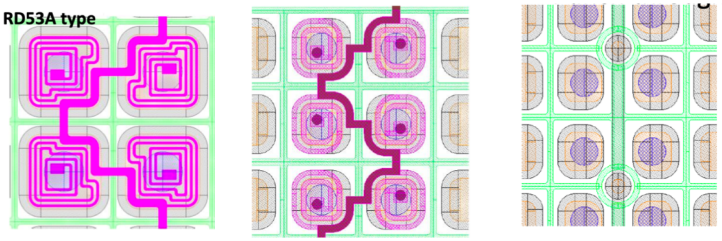


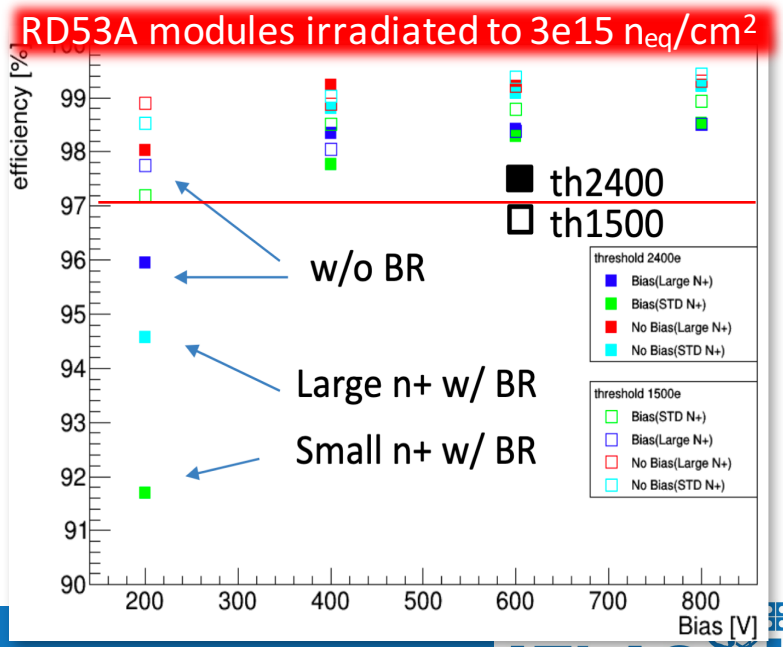
- Thin n-in-p planar sensors: **IBL** is presently using 200 µm n-in-n planar sensors with 50x250 µm² pixel cells. **ITk** will use n-in-p technology (single side process) with 50x50 µm² pixel cells:
  - 150 µm for the outer layers; 100 µm for the inner Layer-1

✓ Required performance
- First results show clear operating
- Hit efficiency >97%
- Bias voltage at end of life up to:
  - 600 V for 150 µm active thickness
  - 400 V for 100 µm active thickness

✓ Market Survey almost finalized
- Tender issued by the end of the year

✓ Vendors are optimizing the final design
- Different biasing solution allowed
  - Punch through (PT)
  - Bias Rail (BR) and bias resistor
  - Temporary Metal (TM)
- Dimension of the n⁺ implant





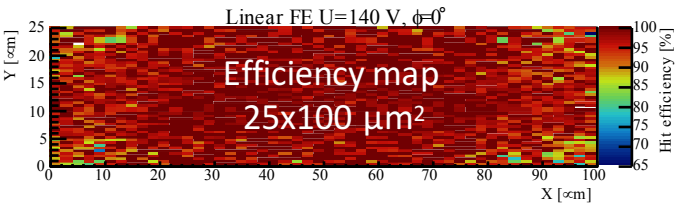
See TREDI2020 for more results

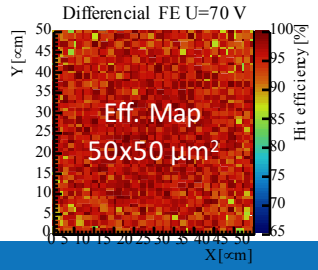
ATLAS ITk

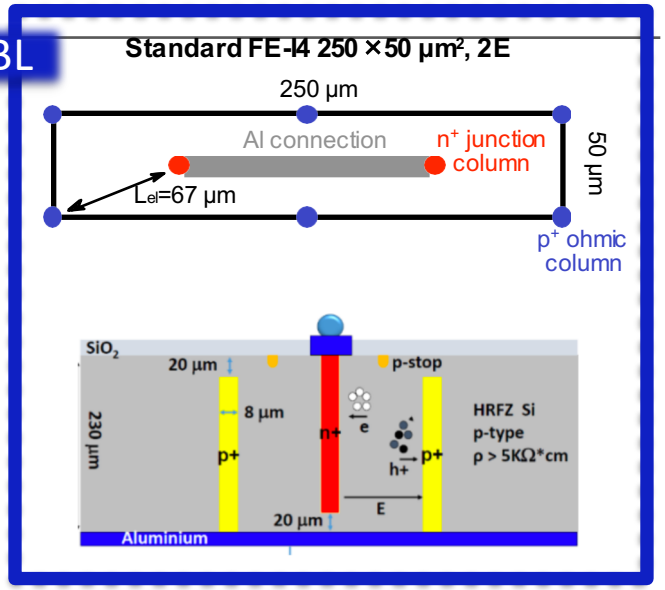
Pixel 3D sensors

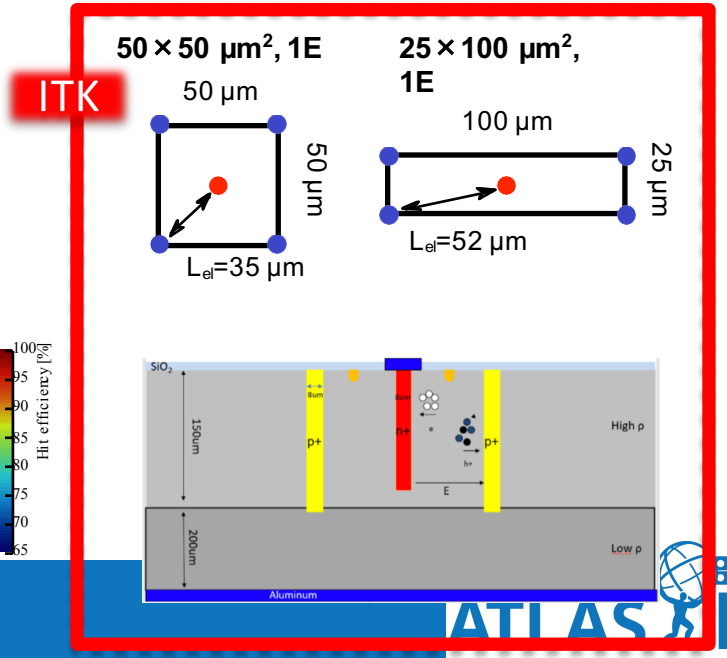
- New single-side technology: conductive support wafer (Si-Si), both electrodes etched from the same side
- 150 µm thin active substrate to reduce cluster size and data rates

- Small pixels (high occupancy + resolution)
  - Rings: 50x50 µm²
  - Flat barrel: 25x100 µm²
- Superior radiation hardness (@1e16 n_{eq}/cm^2)
  - High efficiency: >97%
  - Low operational bias voltage: 80-140 V
  - Low power dissipation < 10 mW/cm² (@-25°C)
- Preproduction already started for FBK, CNM and Sintef!





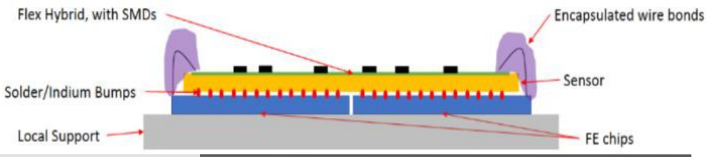




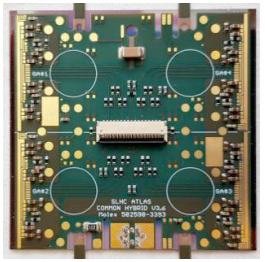
See TREDI2020 for more results

Pixel Modules

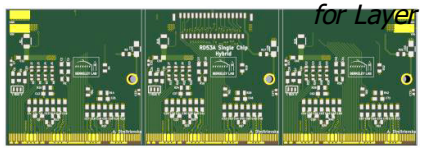
Readout Chip: in Timon Heim's talk



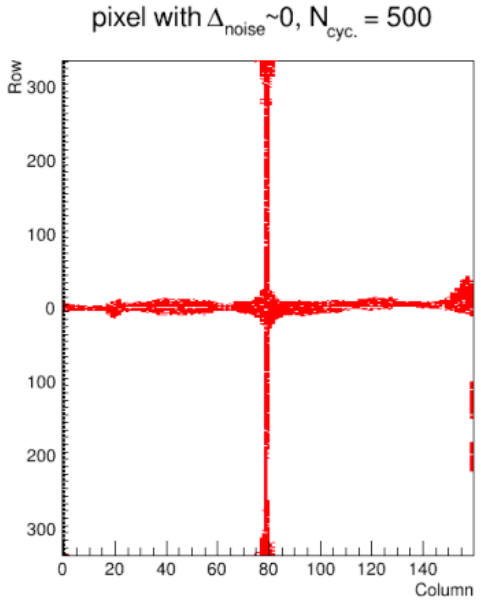
- ✓ Several module prototype stages have helped to reach maturity in several aspects:
  - General module design explored on FEI4 prototypes
  - Extensive studies with ~ 250 RD53A module prototypes: thermal cycling, serial powering, new demonstrator to explore system aspects, …
  - ITkPixV1 modules coming soon



RD53A Quad Dummy



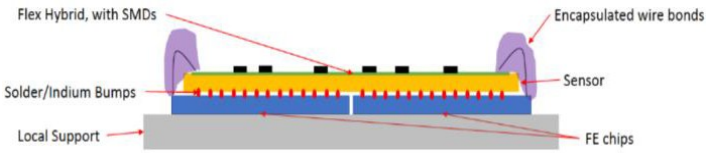
RD53A Triplet Flex for Layer 0



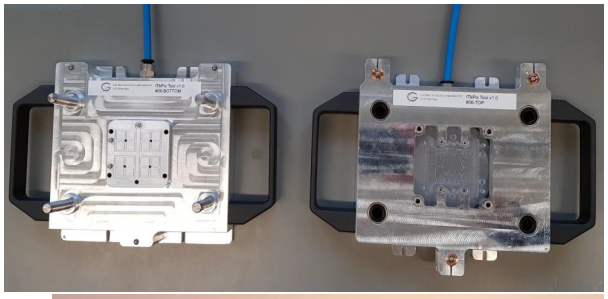
Disconnected bumps in FEI4 modules

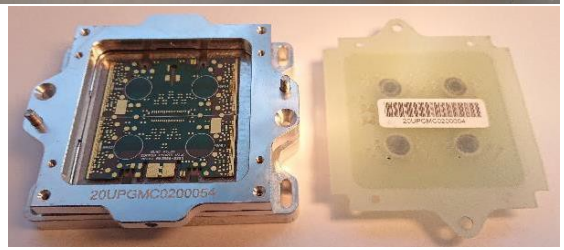
- ✓ Hybridization
  - Demonstration of fine-pitch bump-bonding on RD53A successful.
  - Market survey of vendors running for different process steps: bump deposition, UBM, flip-chip.
  - Concern: Thermal cycling causes bump stress, in case of large CTE mismatch between flex (Cu) and Si. Observed in inter-chip regions of FEI4 quads.
    - Improves with parylene coating of the assembled modules and mitigations in interfaces and flex design. Expected more results by the end of the year.
- ✓ Flex-Hybrid
  - Designs for common flex hybrids finished (RD53A)/ongoing (ITkPixV1).
  - Reduced Cu content to mitigate CTE mismatch with Si

Pixel Modules

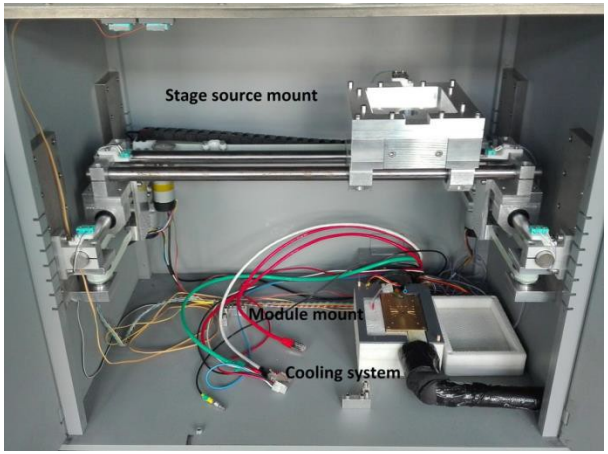


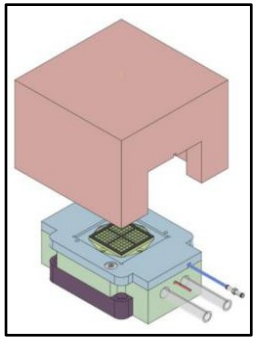
- ✓ Module Assembly
  - Developed common method for flex-to-bare-module attachment
  - In total ~20 module building institutes:
    - **4 institutes already** "qualified"

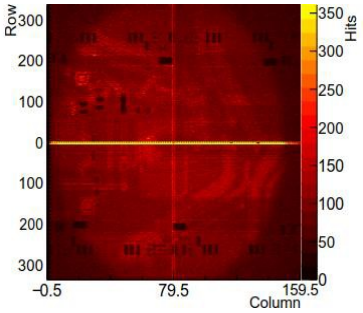




- ✓ Module Testing
  - Design validation (DV) during prototyping and pre-production → very detailed testing beyond design specifications
  - Quality control (QC) on each module built during production → assure installation of good modules



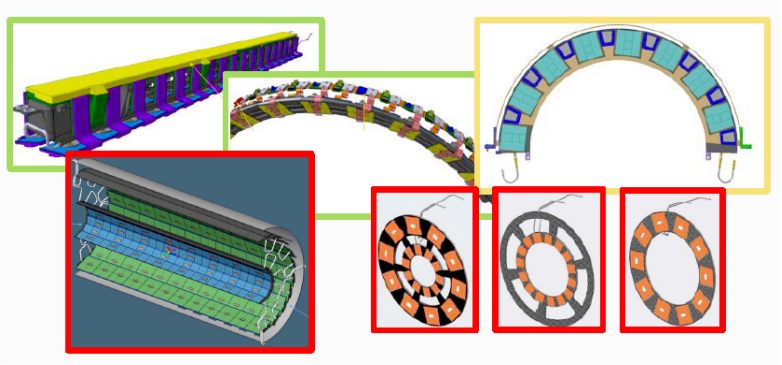


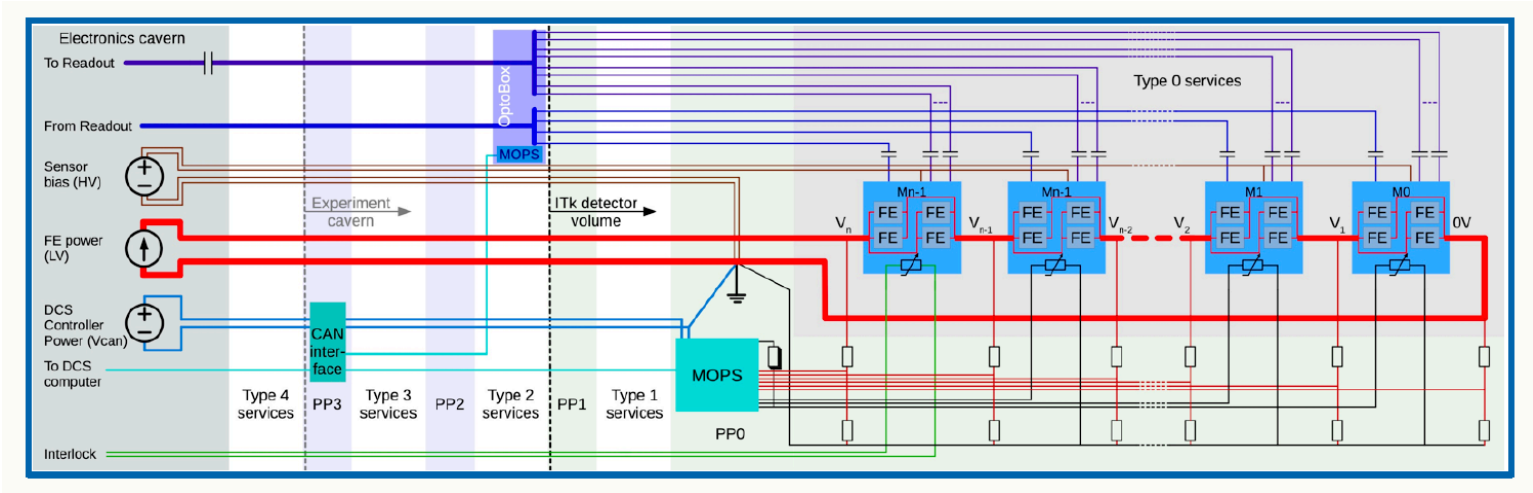


ATLAS ITk

Pixel Serial Powering

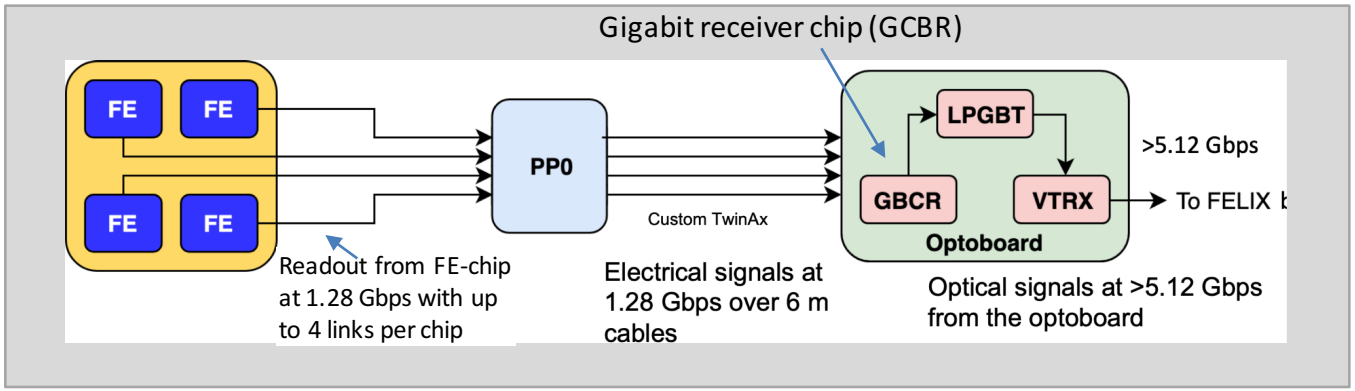
- ✓ **Modules are** connected in series and powered by a constant current source**. Overall** 912 serial powering chains with **3 to 14** modules per chain; length dictated by Layout.
  - All FES on a module powered in parallel. Two Shunt LDO regulators on each FE chip to generate constant operating voltage for digital and analog parts.
  - Dedicated DCS chip (MOPS) for monitoring.
  - Full system level tests available only with FE-I4 prototypes so far. Next stage of testing in ATLAS uses RD53A chips.





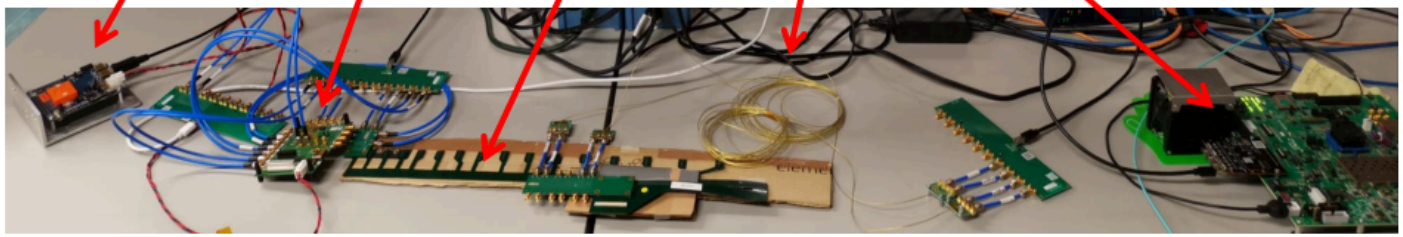
See TWEPP2020 for more details

Pixel Data Transmission



RD53a + Rd53b_cdr + Flex + 6m Twinax+ DAQ

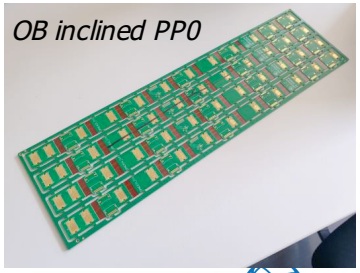
FPGA used to simulate GBCR, LPGBTx and readout



- Results are encouraging (BER < 0.2e-12, spec is 1e-12) and studies continue as components become available
  - Included over summer GBCR v2
  - Use ITkPixV1, will improve on RD53A+RD53B CDR
  - Include final connectors and terminated cable
- System test will evolve but current system is already a realistic test

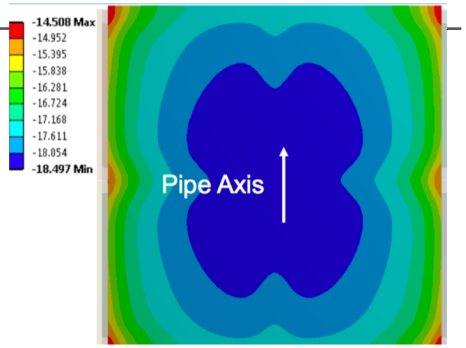
Optoboard

OB inclined PP0

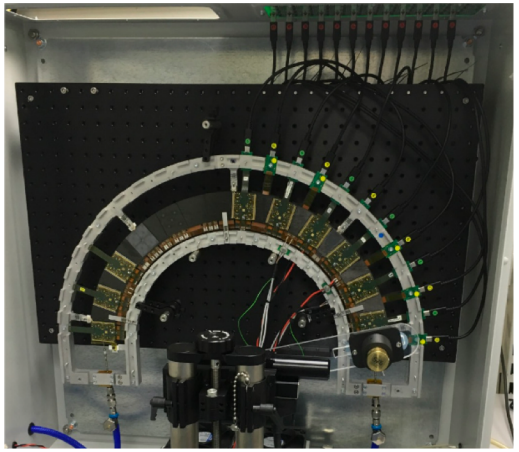


Pixel Demonstrator Program

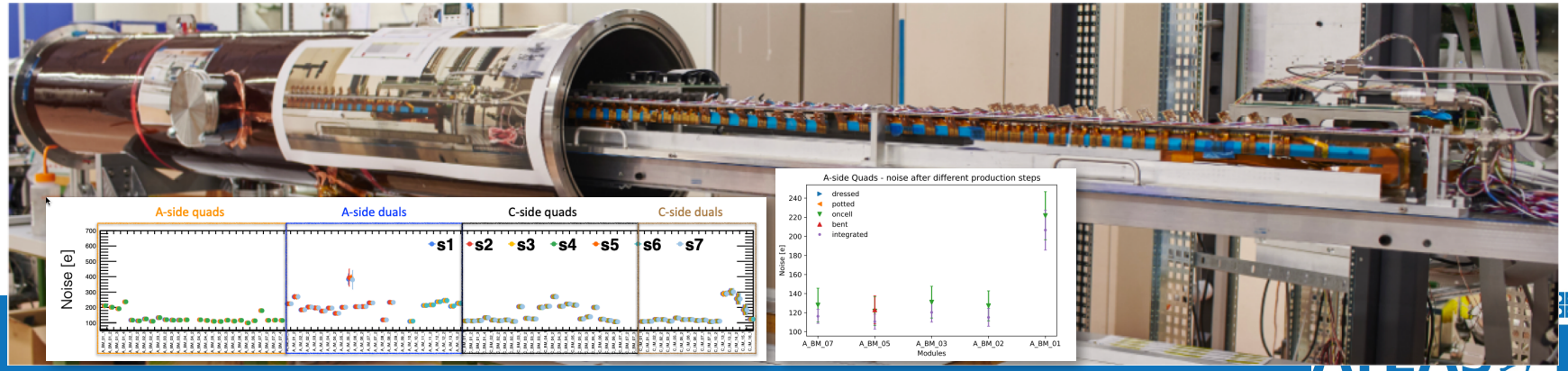
- **Thermo-mechanical studies**
  - Evaluation of thermal performance and manufacturing variability ongoing
  - Simulation results are within thermal specifications
  - Test with Baby Demo CO_2 facility at CERN



- **Endcap system tests with FE-I4-based prototypes**
  - **Ring-0**: 12 module ring structure (2 SP chains)

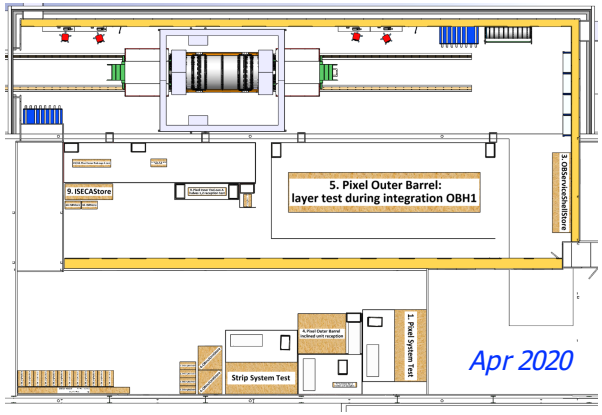


- **Outer barrel demonstrator programme**
  - Thermal and electrical prototypes
  - Full size prototype (1.6 m) with 7 quads and 13 duals
    - 6 serial powering chains with electrical modules

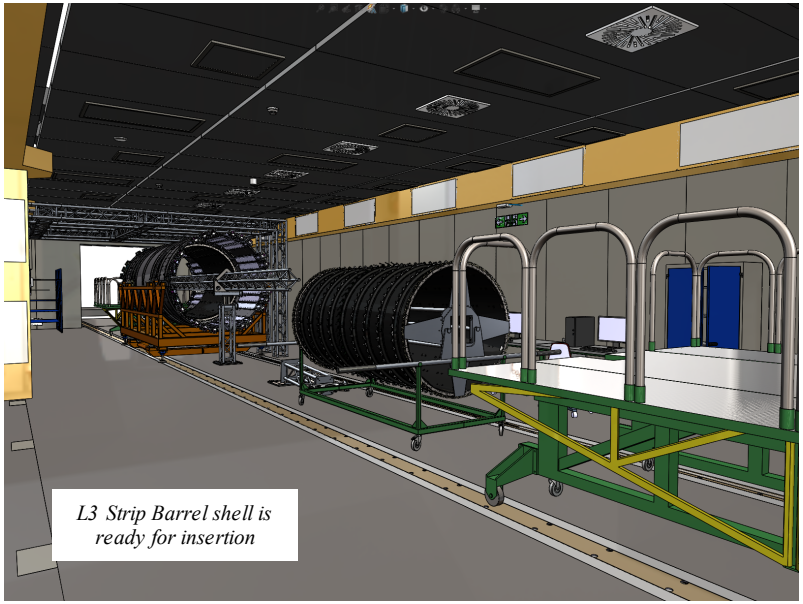


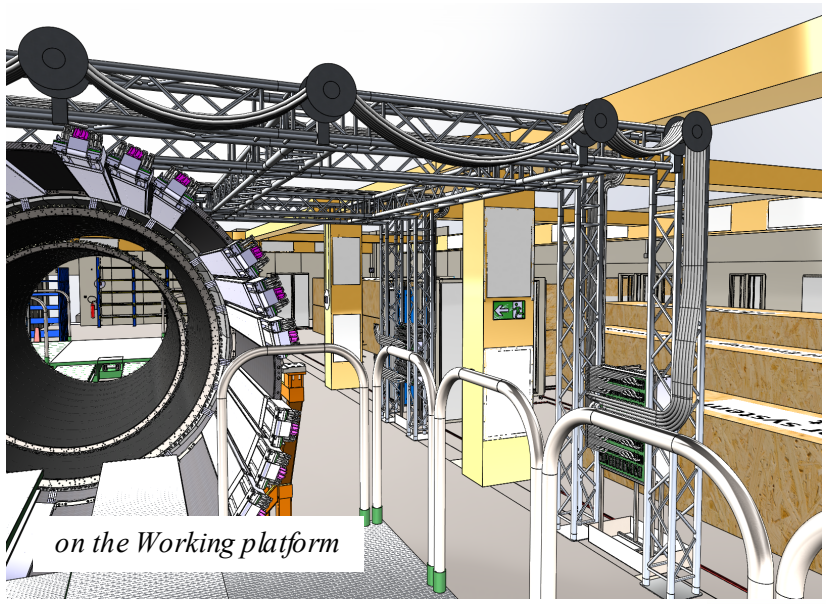
Preparation for ITk integration

- ✓ ITk integration will happen in the surface at P1 in our assembly building (SR1).
  - Outer Cylinder arrives in SR1 at the end of 2021.
  - Strip Barrel integrated in SR1. Endcaps arrive from DESY and NIKHEF.
  - Pixel Outer Barrel integrated in SR1, Outer Endcaps arrive from UK/Italy, Inner System in quarters from US.



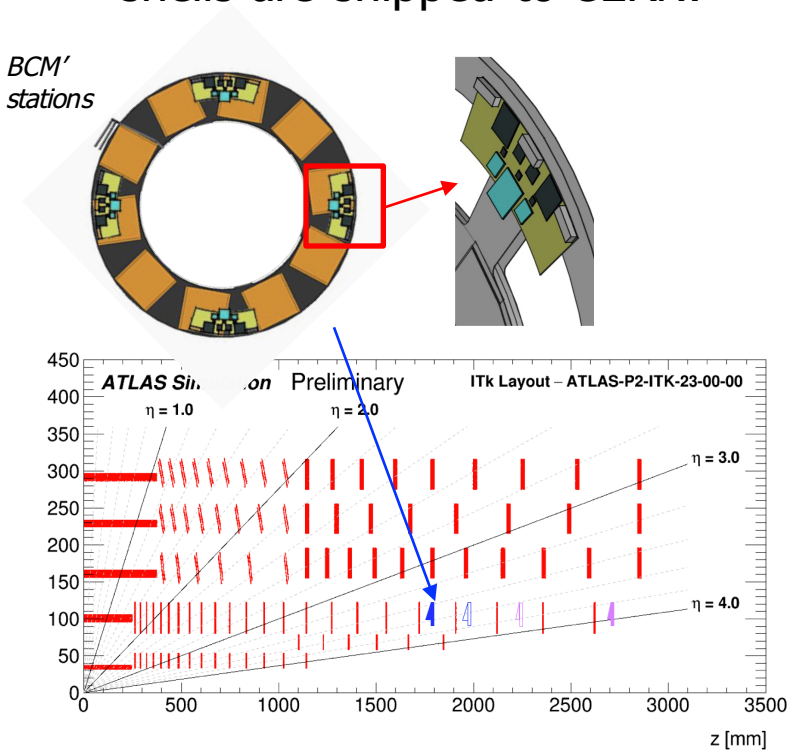
- ✓ 3D precise modeling allows for detail planning of space and services.



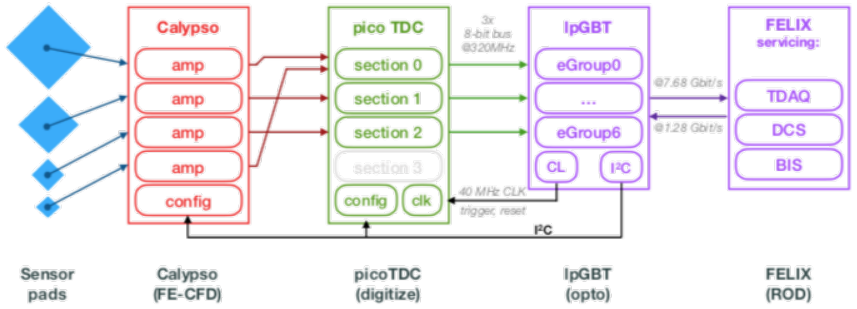


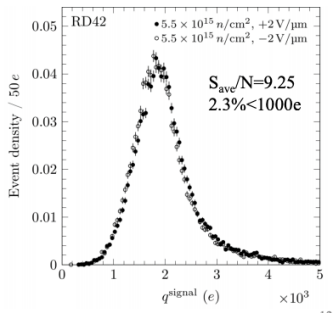
Beam Condition Monitor'

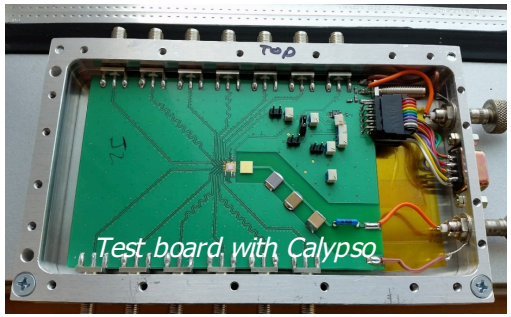
- ✓ BCM' stays within the Pixel IS, provides Fast (bunch-by-bunch) safety system for ATLAS, Luminosity measurement and Background monitoring
  - Separate out functionalities of abort and lumi measurement for HL-LHC
- ✓ BCM' occupies a separate ring; 4 *stations* per side with abort, lumi BCM' and BLM. It has to be delivered for integration at SLAC, before IS quarter shells are shipped to CERN.



Service baseline: Complete readout with optical fibre in/out





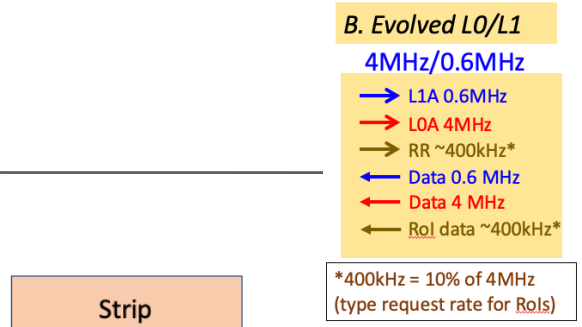


Conclusions

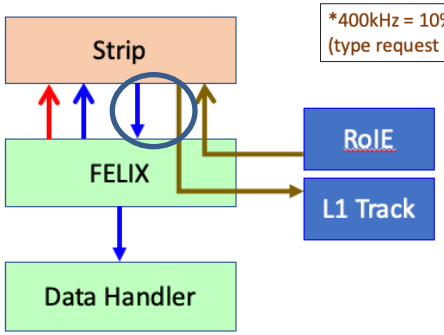
- No time to discuss several other ingredients to the ITk project that are substantial to the construction:
  - The production database - ramping up with first preproduction
  - The CO2 system, partially developed with CMS for the primary systems and plants and while distributions lines are up to ATLAS to be developed and qualified
  - The environmental monitoring, the interlock systems …
- Moving from prototypes to construction!
  - The Strip system is starting the preproduction for several parts of the system
    - Several issues solved between the readiness for preproduction and the actual start. And learning lots from the important system tests on large structures → Important take-awayis to have System Tests as earlier as possible in the project.
  - Pixel is just starting the first preproduction (3D, planar sensors soon).
    - Since the last year fixed the last choices on the L0 radius and pitch; data transmission services inventory.
- The project has accumulated some delay with respect the original plan.
  - COVID is of course impacting the production seriously and in a not very uniform way the different institutes and deliverables.

Additional

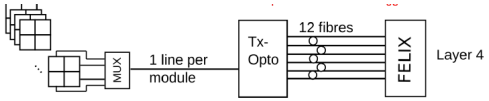
Trigger and ITk: TDR plans



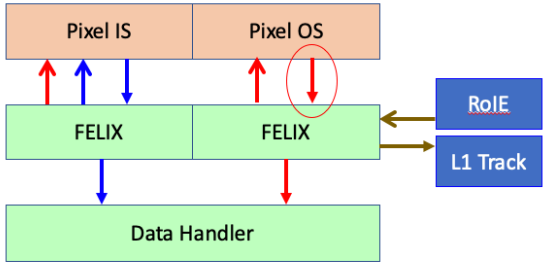
- ✓ **Strips**: data are buffered in the FE electronics at the 4 MHz L0A rate. Regional Readout Requests (RRRs) are issued at a rate of 4 MHz targetting no more than 10% of the detector to request the transmission of RoIs to FELIX.
  - Upon receipt of an L1A, all of the data are read out at a rate of 600 kHz. Data are therefore transmitted after an RRR or L1A at a total combined rate of up to 1 MHz.



- ✓ **Pixel**: all data from those layers (the Outer System) contributing to the L1A decision are read out at the L0A rate of 4 MHz; sufficient data fibres and cables need to be installed
  - Pixel Outer was the target in the TDR, using active cables with an aggregator chip on detector and equalizer on the optoboard side. The aggregator should have multiplexed **four 1.28 Gbps** differential lanes from one or multiple Front-Ends in the same module into **one 5.12 Gbps** output.



  - The selection of data for the L1 hardware-based trigger system will be done off-detector, in the Readout System, based on RRRs received from the Global Trigger.



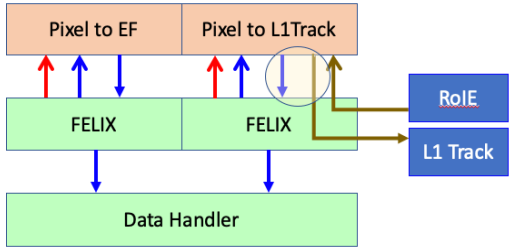
ITk contributes to L1 decision:

RRR for Strip, full events for Pixel

Trigger and ITk: post-TDR

- ✓ After the TDR, several complications emerged:
  - RD53 decision to drop support for 5.12 Gbps output drivers
  - →Passive Twinax cables driving directly FE ASICs e-links (@ 1.28 Gbps) to the opto-box. No aggregator ASIC → significant increase of no. of cables in the ITk-Pixel volume
  - An updated estimate of the data rates with the more accurate description of the services material, together with an improved knowledge of the envelopes and new limits on the bandwidth occupancy (50%) for modules read at Level-0) made clear that the requested 4 MHz maximum trigger rate was impossible to reach in several detector parts
- ✓ → ATLAS decision in June 2020 that Pixel implements the services for an **effective maximum readout rate of 1 MHz**.

- ✓ Either Pixels DO NOT contribute to L1Track or a RR mode, ~similar to the Strip one, is implemented in the FE ASICs.
- ✓ **To be decided by ATLAS in mid-October if to pursue this option further.**



Strip Services