R&D Status of Monolithic SOI Pixel Sensor for Vertex Detector

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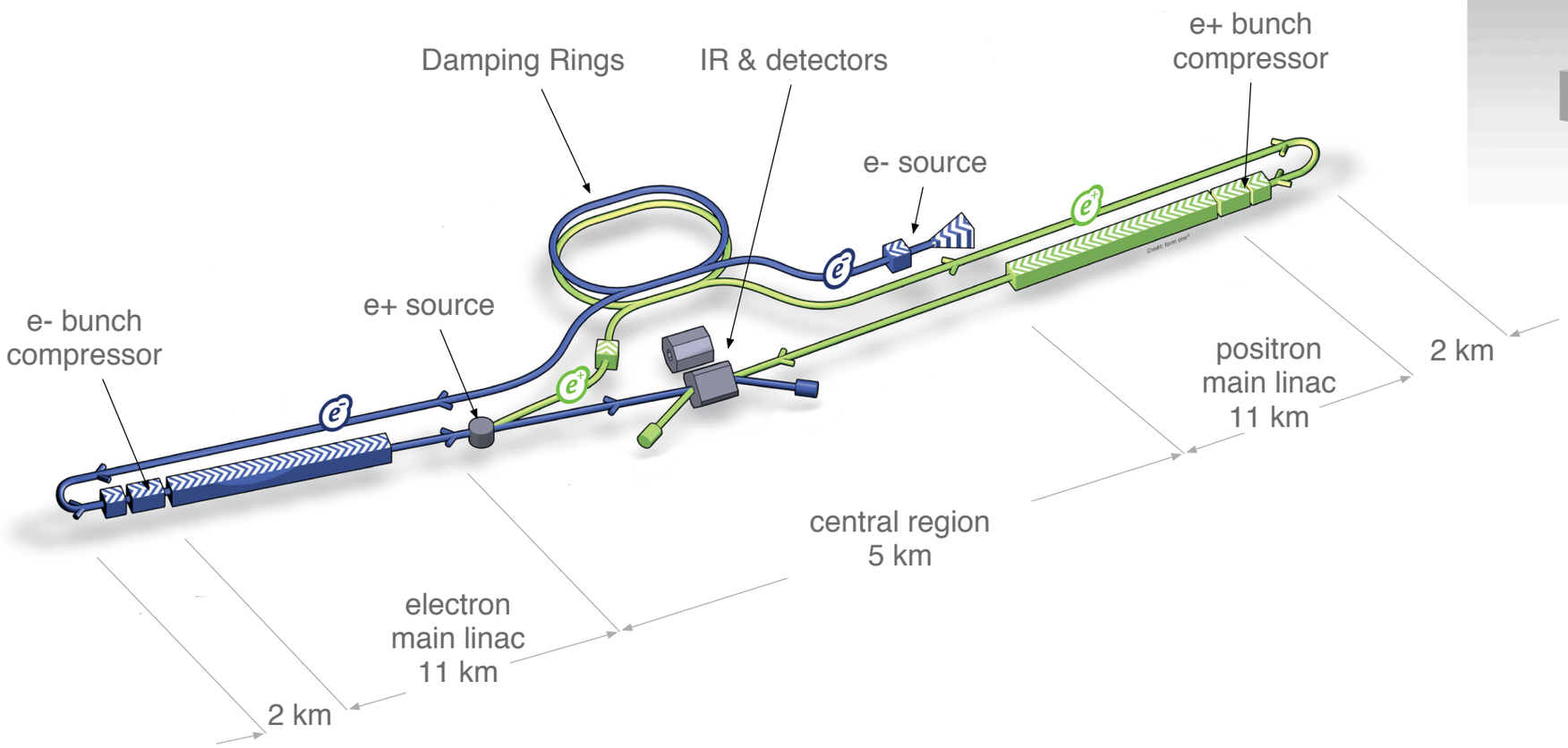
and SOI PIXEL R&D Group

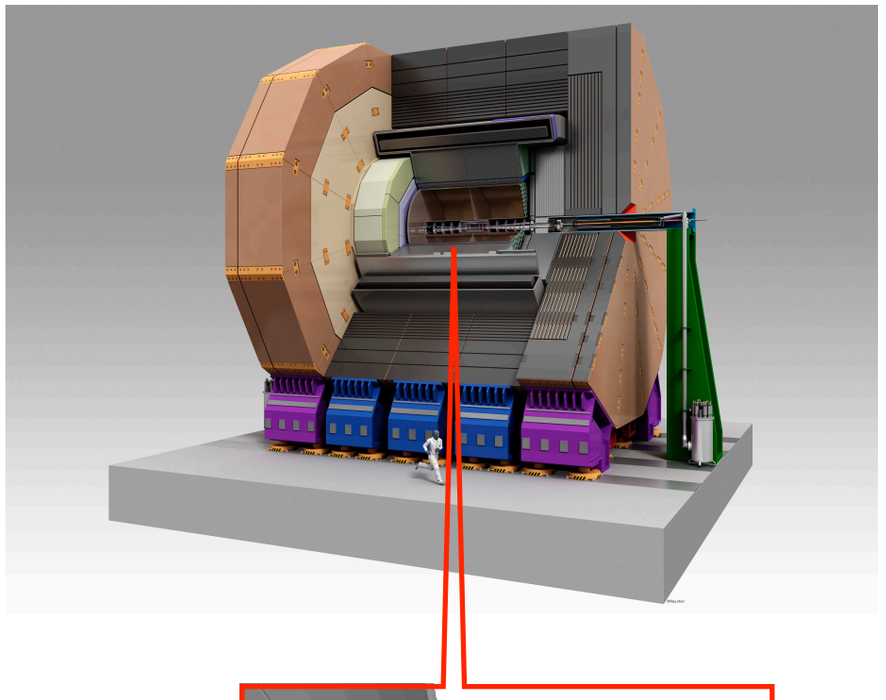
ILC Experiment

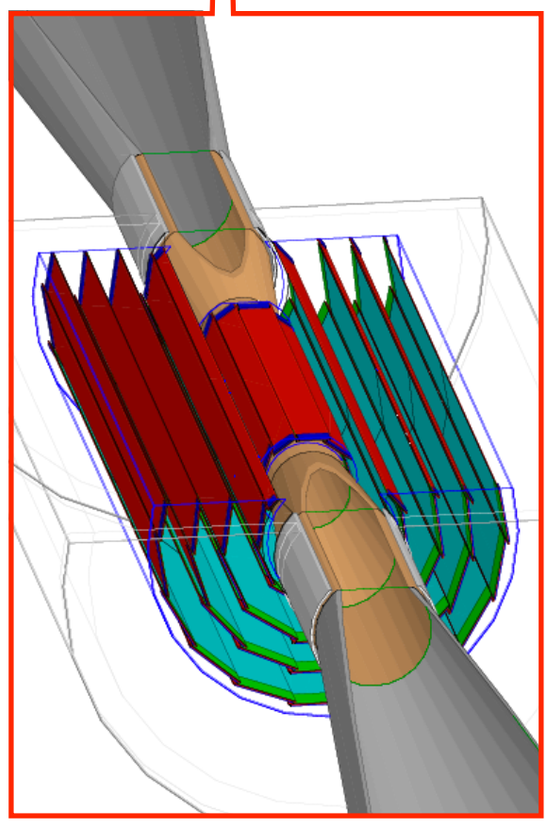
ILC Experiment

- e^+e^- linear collider
- Center of mass energy: 250 - 500 GeV (extendable to 1 TeV)
- Precise measurement of the Higgs boson
- Search for beyond the Standard Model



ILC detector concept (ILD)





Vertex detector geometry (VTX-SL)

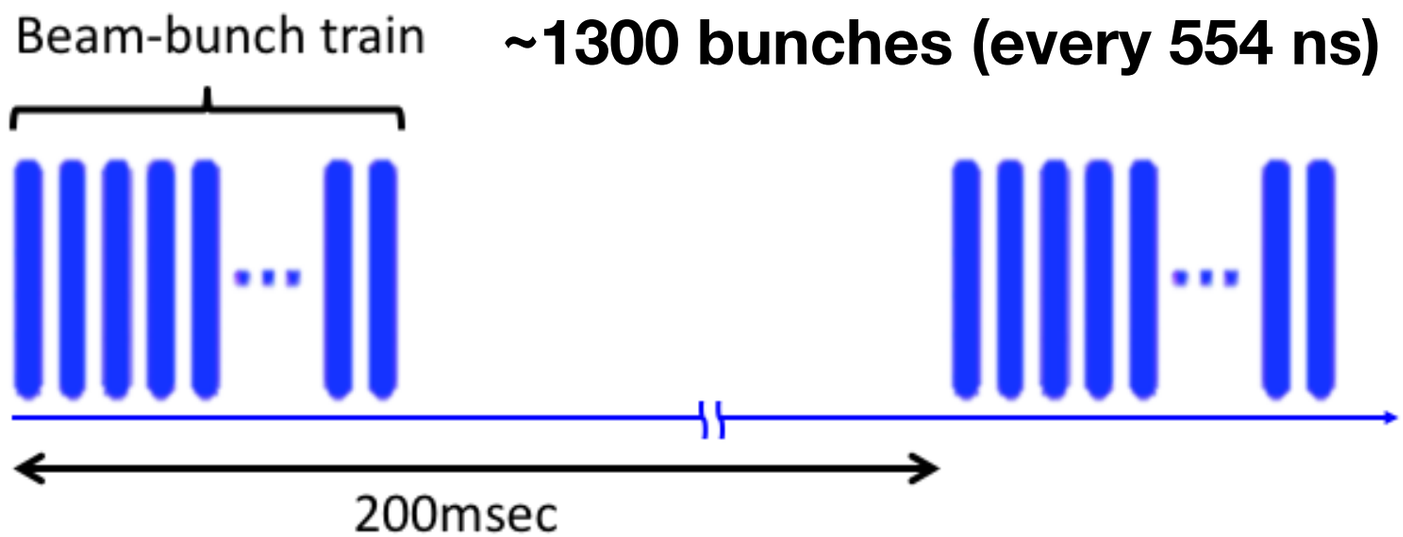
ILC TDR vol.4: Detectors
ILD Concept Group, T. Abe et al., arXiv:1006.3396 [hep-ex].

ILC Vertex detector

Requirements:

1) Single point resolution: better than 3 μm
   Pixel size: ~20 × 20 μm^2
2) Time resolution: single-crossing (554 ns interval) time resolution
3) Detector occupancy: < 2 %
4) Low material budget: $X \leq 0.1 - 0.2$ % X_0 / Layer
   corresponds to ~ 100 - 200 μm Si, including supports, cables and cooling
   low-power ASICs (~ 50 mW/cm^2) + gas-flow cooling
5) Radiation hardness:
   TID : < 1 kGy / year
   NIEL: < 10^{11} 1MeV n_{eq} / cm^2 / year

We are designing and evaluating prototype pixel sensor with SOI technology to fulfill the requirements.



ILC TDR v4 Detector
LC Vertex / Tracking R&D 2nd Nov. 2015

SOI Pixel Detector

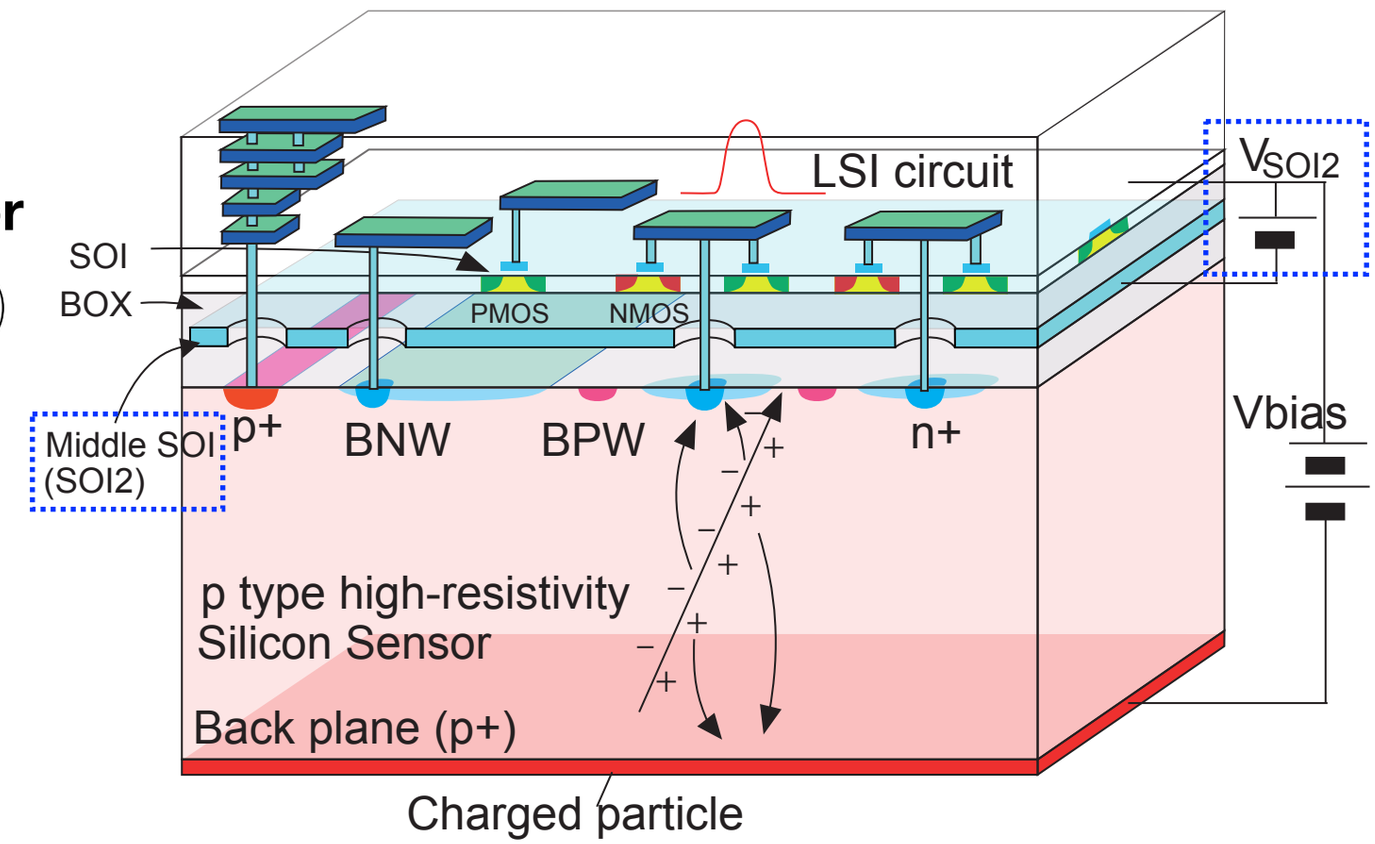
SOI: Silicon-on-Insulator technology

Utilize 0.2 μm FD-SOI CMOS process by
Lapis Semiconductor Co. Ltd.

SOI Pixel Detector: Monolithic type detector

- LSI is processed on Buried Oxide layer (BOX)
- Smaller pixel size, complex circuit in pixel
- Low material budget
- High speed, low power
- Less single event effects (SEE) probability
- Low cost

Double SOI Pixel Detector



Double SOI Pixel Detector

Middle Si layer suppresses

- Back gate effect
- Sensor-Circuit cross talk
  - Middle Si layer shields coupling between sensor and circuit.
  - It is useful for analog and digital mixed circuit in pixel.
- Radiation damage (TID)
  - It is able to compensate electric field generated by trapped holes in the BOX.
  - It can be used in high radiation environment (~1MGy).
  - (K. Hara et. al., TIPP2017, May 22-27, 2017, Beijing)

Sensor thickness: 50 - 500 μm
Sensor Resistivity: > 1 kΩ·cm
SOI2 thickness: 150 μm (*n*-type)
SOI2 Resistivity: < 10 Ω·cm

Functions for ILC Vertex Detector

Necessary functions for the ILC vertex detector:

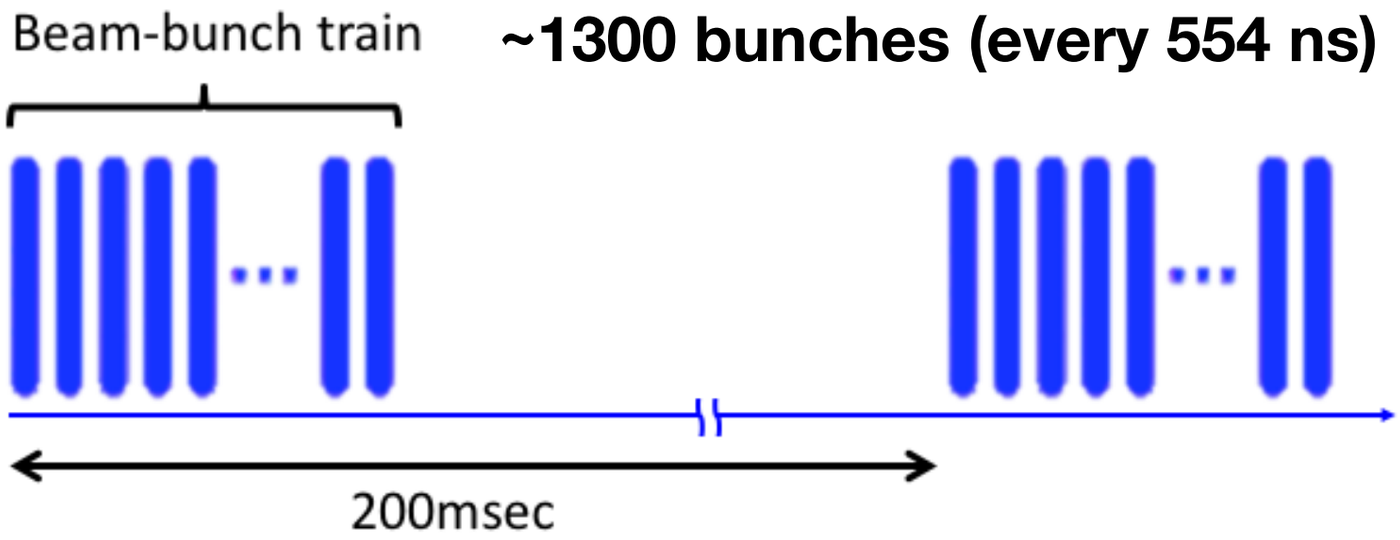
- Single point resolution
  Pixel size: less than 20 μm
  Calculate weighted center of charges (Charges are spread among multi pixels).
  → Record an analog signal of a hit.

- Timing resolution
  Bunch crossing occurs every 554 ns in 1-msec-long bunch train with an interval 200 ms.
  Identify a collision bunch of a hit to reconstruct a event.
  → Record a time stamp of a hit.

- Detector occupancy
  Hit information have to hold during 1 beam-bunch train.
  Increase detector occupancy.
  → Need multiple memories

- High speed data transfer
  Data have to be send to backend before next bunch train injection.
  → Reduce a data to transfer.

We designed a prototype pixel detector SOFIST.



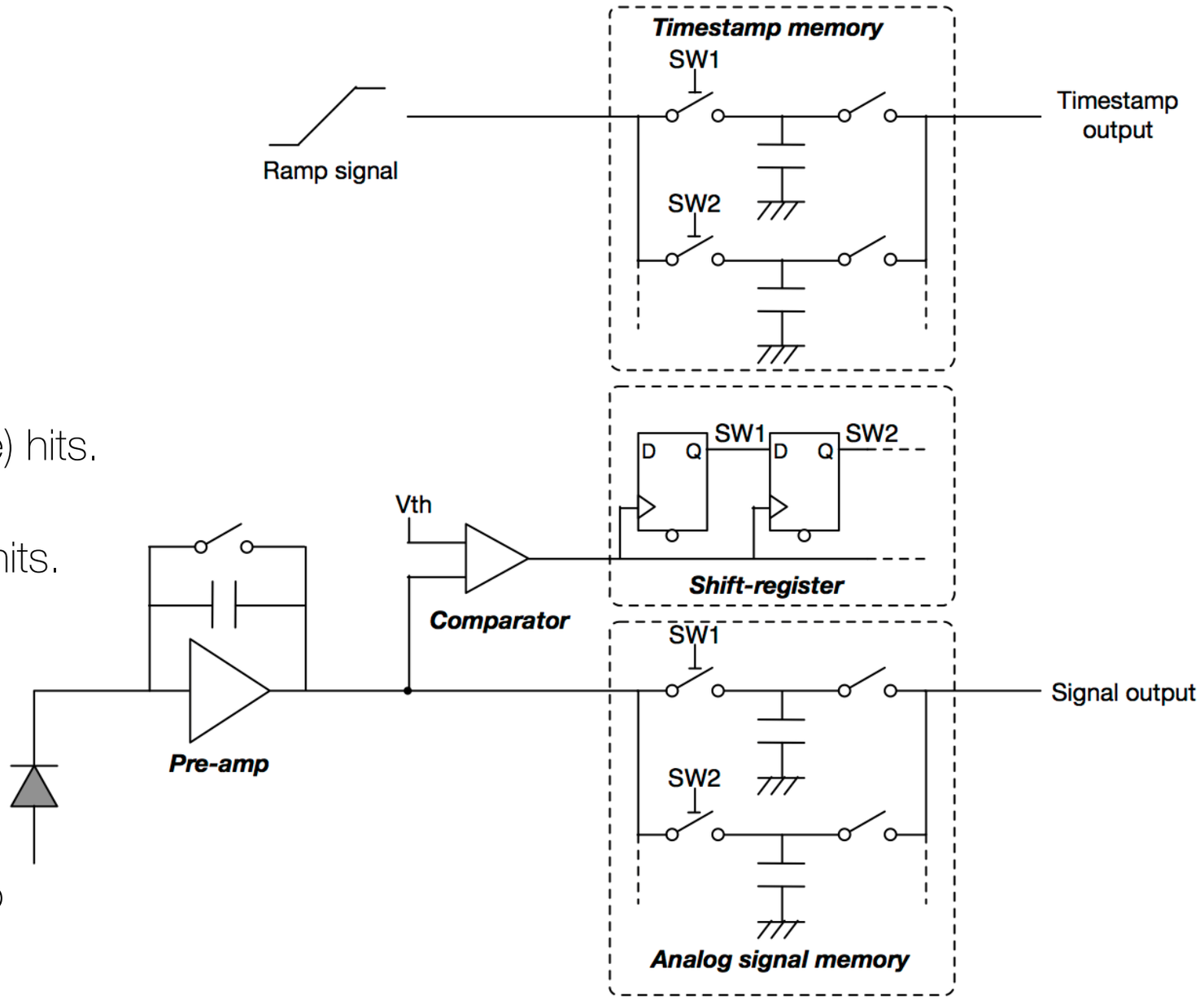
Architecture of SOFIST

In a Pixel

- Pre-amplifier
- Comparator
  Keep the analog signal and time stamp
  if a signal exceeds a threshold V_{th}.
- Shift register
  Latch for multiple memories.
- Analog signal memory
  Store signal charges up to two (or more) hits.
- Time stamp circuit
  Store time stamps up to two (or more) hits.

On Chip

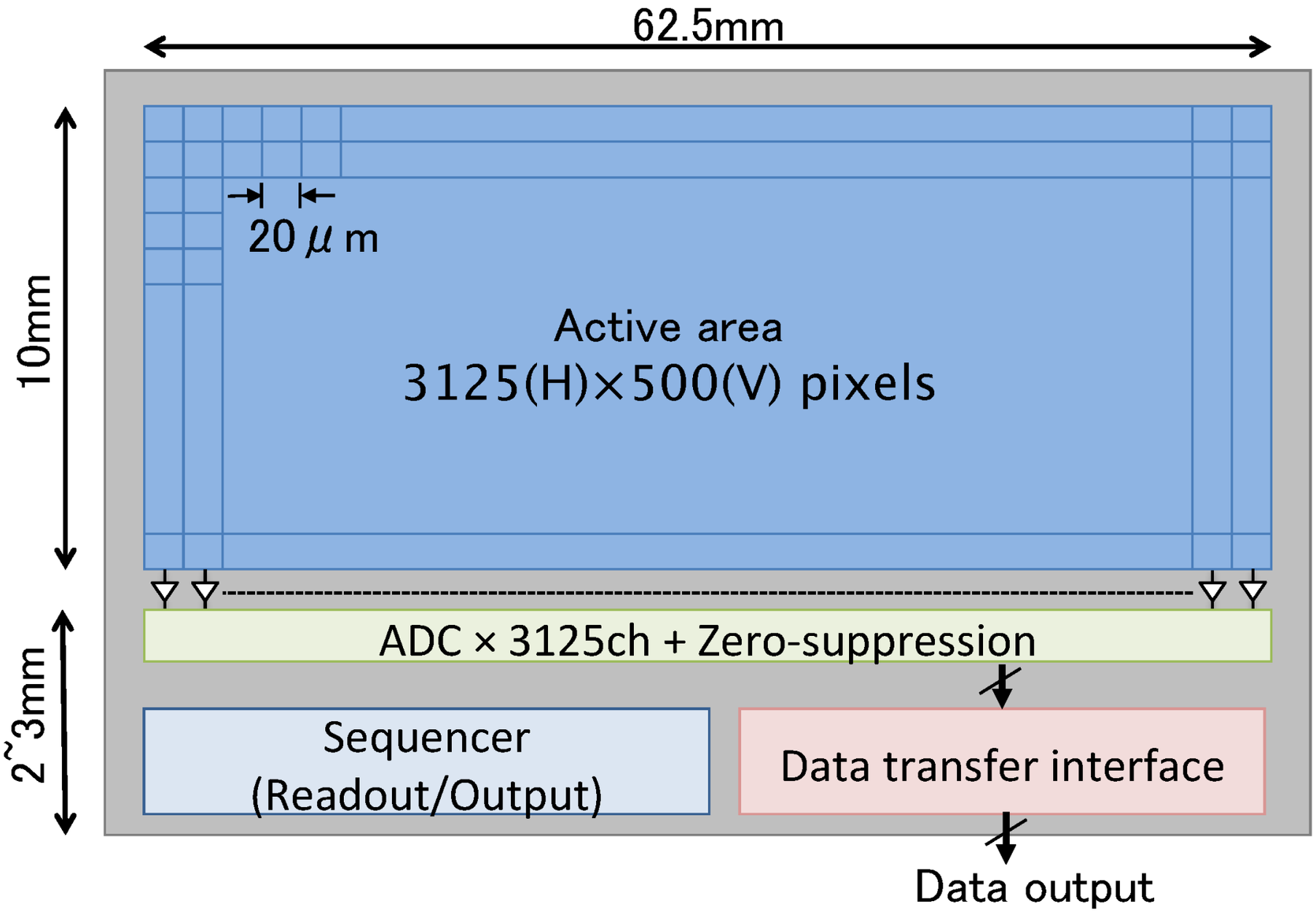
- Column ADC
  Digitize analog signal and time stamp.
- Zero-Suppression logic
  Extract hit pixels and reduce the data to
  transfer to backend.



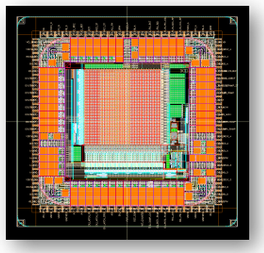
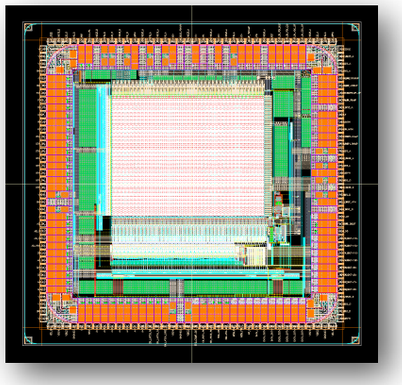
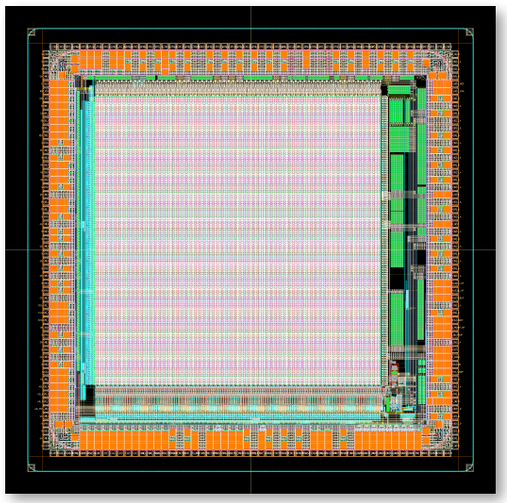
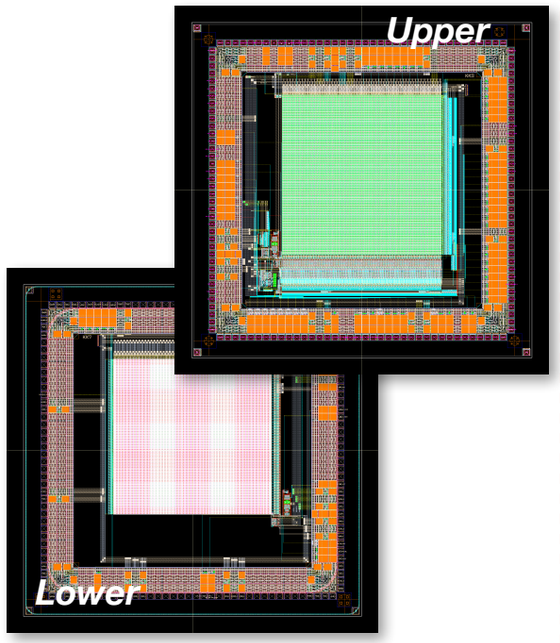
SOI sensor for ILC: SOFIST

SOFIST: SOi sensor for Fine measurement of Space and Time

Conceptual SOI pixel sensor for the ILC (inner most layer of the vertex detector).



SOFIST

SOFIST	ver.1	ver.2	ver.3	ver.4 (3D)
	Beam test at FNAL in Jan. 2017 Analog signal	**Beam test at FNAL in Feb. 2018 Analog signal or Timestamp**	**Beam test at FNAL in Feb. 2019 Analog signal and Timestamp**	**Beam test at FNAL in Feb. 2020**
				
Chip Size (mm^2)	2.9 × 2.9	4.45 × 4.45	6 × 6	4.45 × 4.45
Pixel Size (μm^2)	20 × 20	25 × 25	30 × 30	20 × 20
Pixel Array	50 × 50 (Analog Signal)	64 × 64 (Time Stamp) 16 × 64 (Analog Signal)	128 × 128 (Analog signal and Time stamp)	104 × 104 (Analog signal and Time stamp)
Functions (Pixel)	Pre. Amplifier (CSA) Analog signal memory (2 hits)	Pre. Amplifier (CSA) Comparator (Chopper inverter) Shift register (DFF × 2) Analog signal memory (2 hits) or Time stamp memory (2 hits)	Pre. Amplifier (CSA) Comparator (Chopper inverter) Shift register (DFF × 3) Analog signal memory (3 hits) Time stamp memory (3 hits)	Pre. Amplifier (CSA) Comparator (Chopper inverter) Shift register (DFF × 3) Analog signal memory (3 hits) Time stamp memory (3 hits)
Functions (On Chip)	Column ADC (8 bit)	Column ADC (8 bit) Zero-suppression logic	Column ADC (8 bit)	Column ADC (8 bit)
Wafer	FZ *n*-type (Single SOI)	Cz *p*-type (Double SOI)	FZ *p*-type (Double SOI)	FZ *p*-type (Double SOI)
Wafer Resistivity (kΩ·cm)	2 ≤	1 ≤	3 - 10	3 - 10
Status	Delivered (Dec. 2015) Position resolution ~1.4 μm	Delivered (Jan. 2017) Time resolution ~1.55 μs	Delivered (May. 2018) Time resolution ~1.92 μs	Delivered (Jan. 2019 ~) Under evaluation

SOFIST3

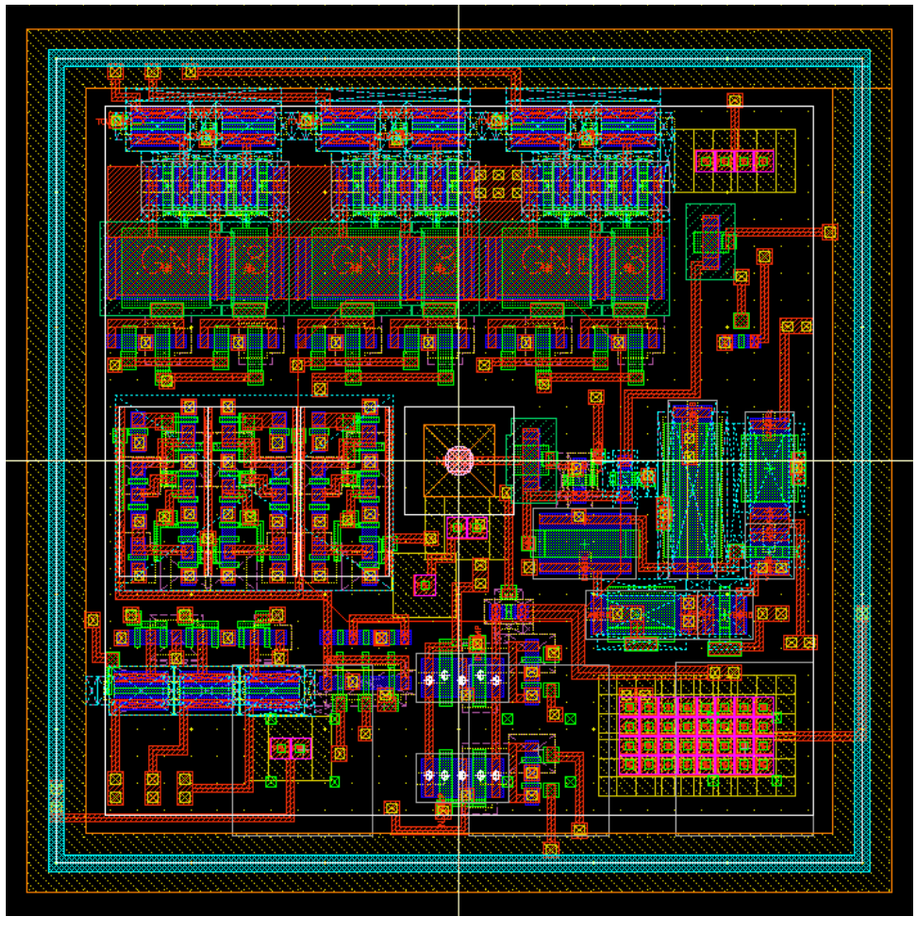
Pixel

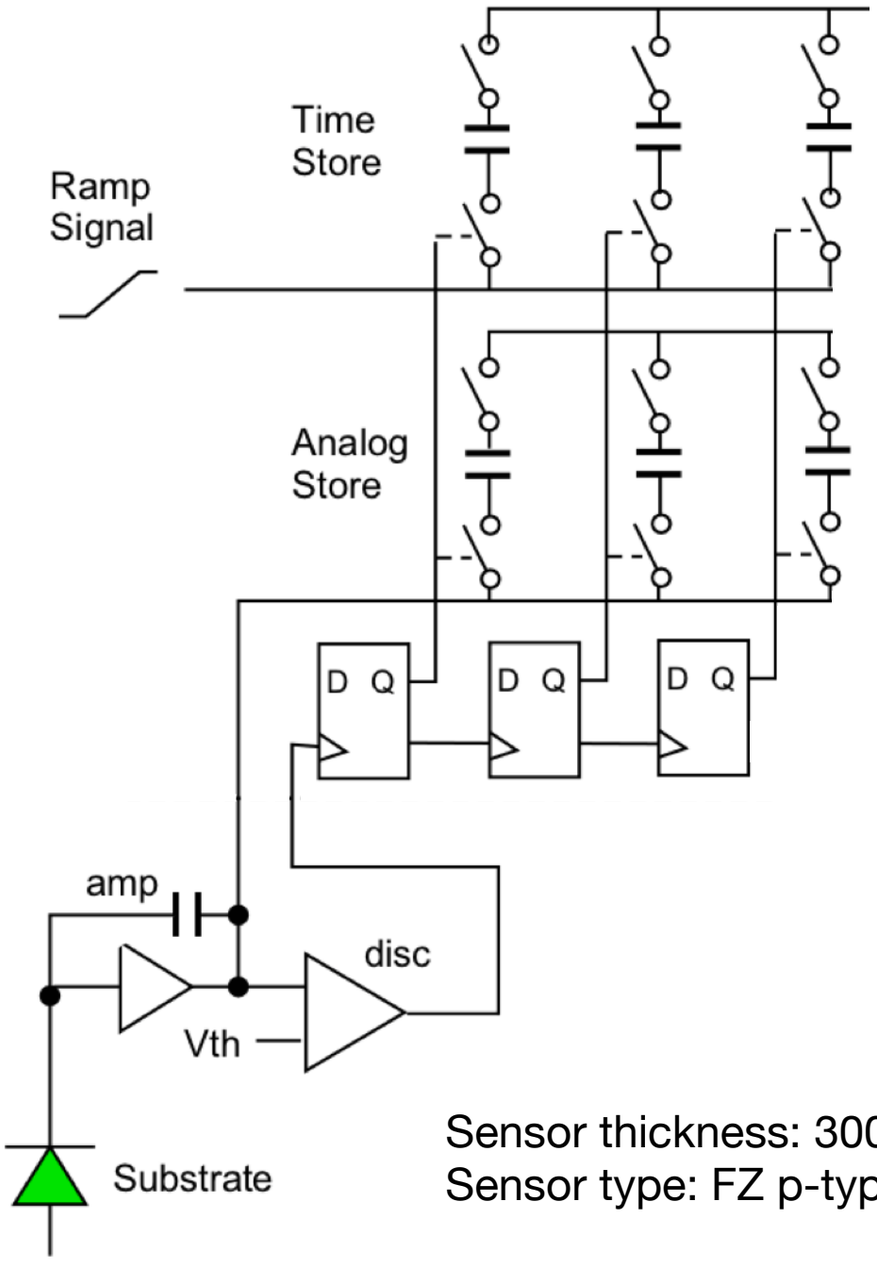
- Pre. amplifier (Charge sensitive amplifier)
- Comparator (Chopper inverter)
- Shift register (three hits)
- Analog signal memories (three hits)
- Time stamp memories (three hits)

On chip

8 bit column ADC

Pixel size: 30 × 30 μm^2





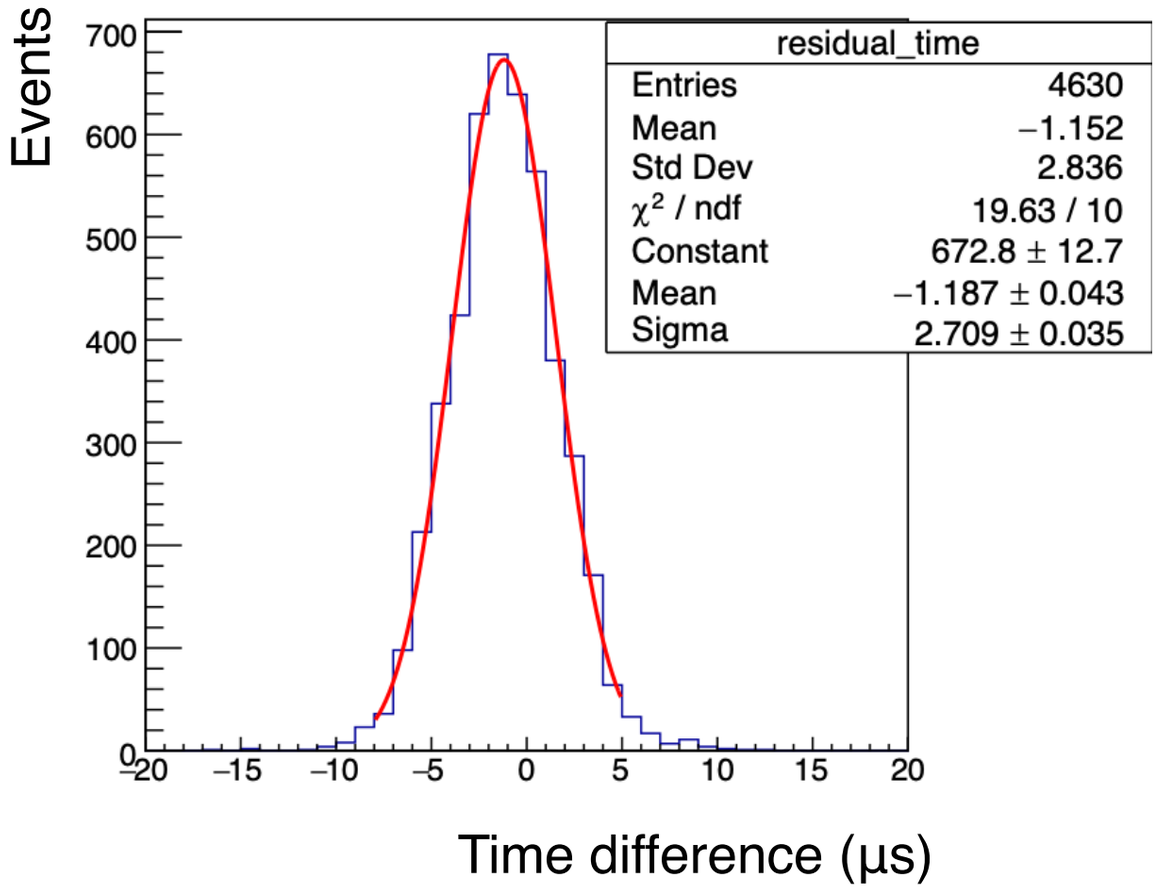
Sensor thickness: 300 or 65 μm
Sensor type: FZ p-type, DSOI

All necessary functions which are the same as SOFIST4 are implemented into a pixel.
Evaluation of pixel circuit is the main purpose of SOFIST3 due to large size pixel (30 × 30 μm^2)

SOFIST3

Timestamp residual

Timestamp difference between #1 and #4.

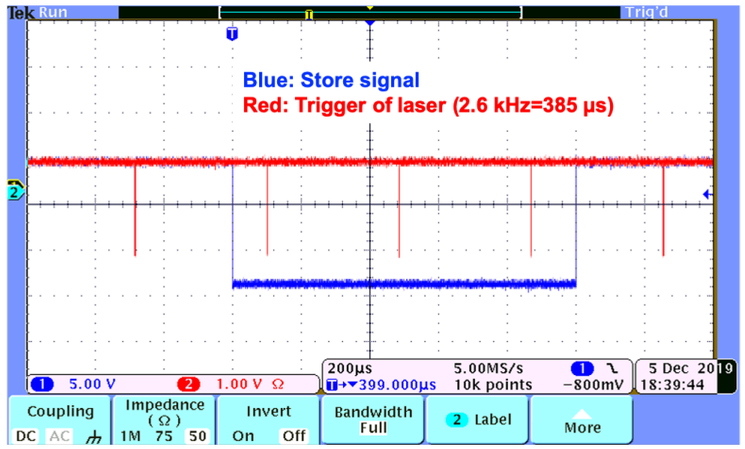


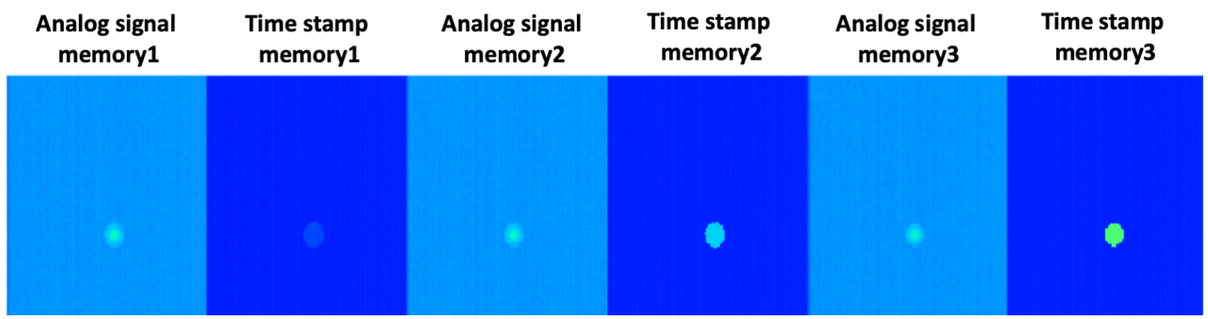
Intrinsic resolution: 2.71/√2 ~ 1.92 *μs*

Sensor Thickness: 300 μm

Multi-memory readout test

SOFIST3 has three hit, analog signal and timestamp memories.
Multi-memory readout scheme was tested by injecting a IR laser three times in a 1 ms period.





Analog signal

Represent stable laser pulses (~180 ADC).

Timestamp

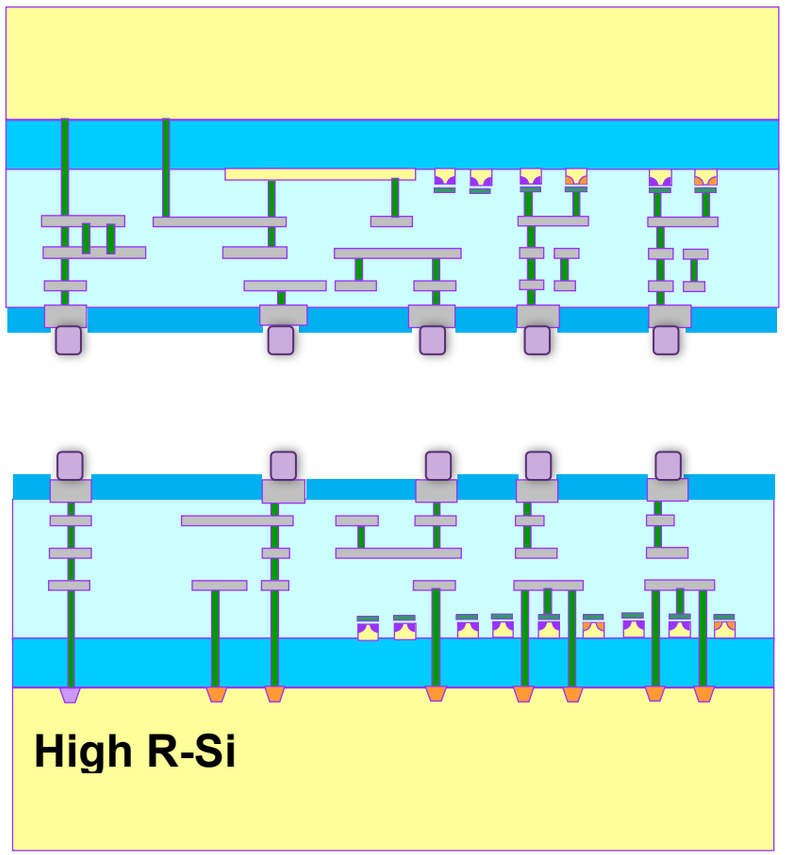
Show different timing of the laser injection (110, 490, 880 ADC).

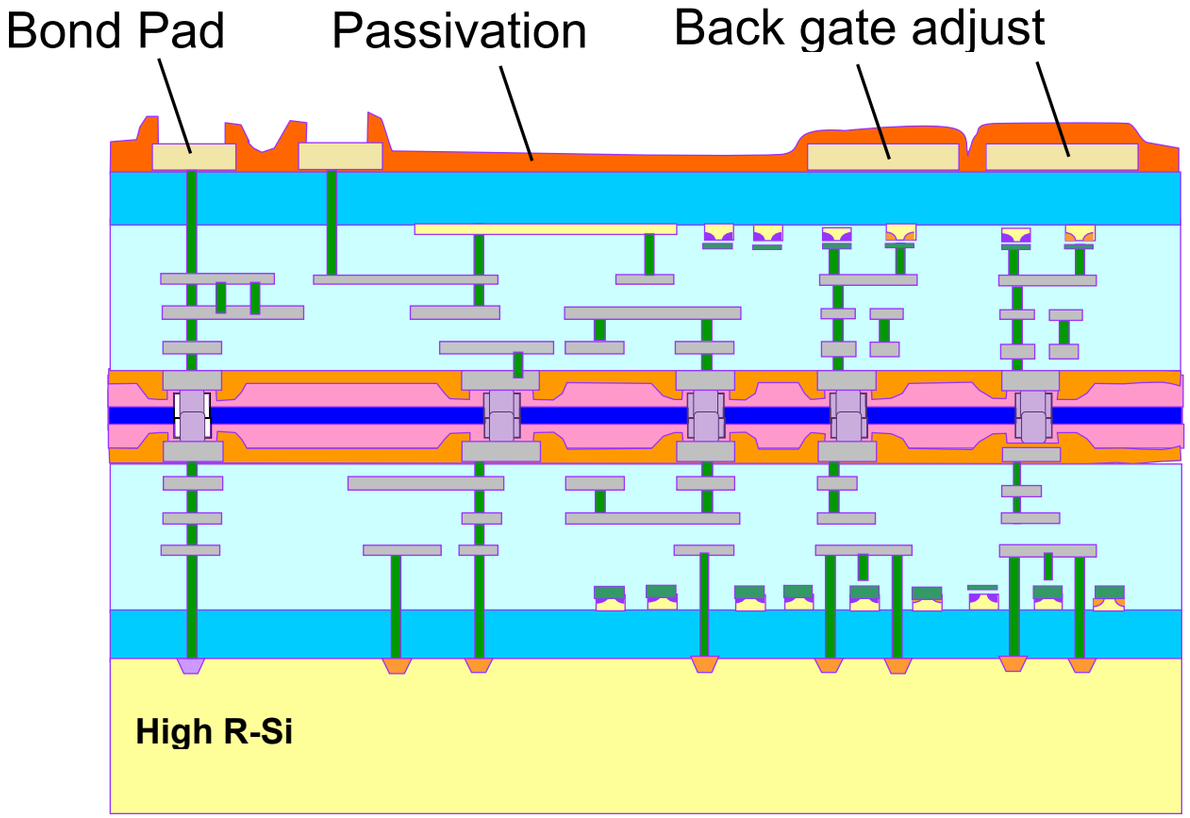
SOI Based 3D Stacking

Two SOI chips are connected by micro bump (3 μm diameter) pixel by pixel.
→ Keep pixel size small and implement complex circuit three dimensionally.

Detail of technology is shown by I. Kurachi (KEK) today [C06].

Upper





Lower

Lower Chip (Pixel): used as sensor and implement analog circuit in a pixel.
Upper Chip (Pixel): sensor layer is removed by wet etching and then formed Al pad for wire bonding on the BOX.
digital circuits/memories are implemented in a pixel.

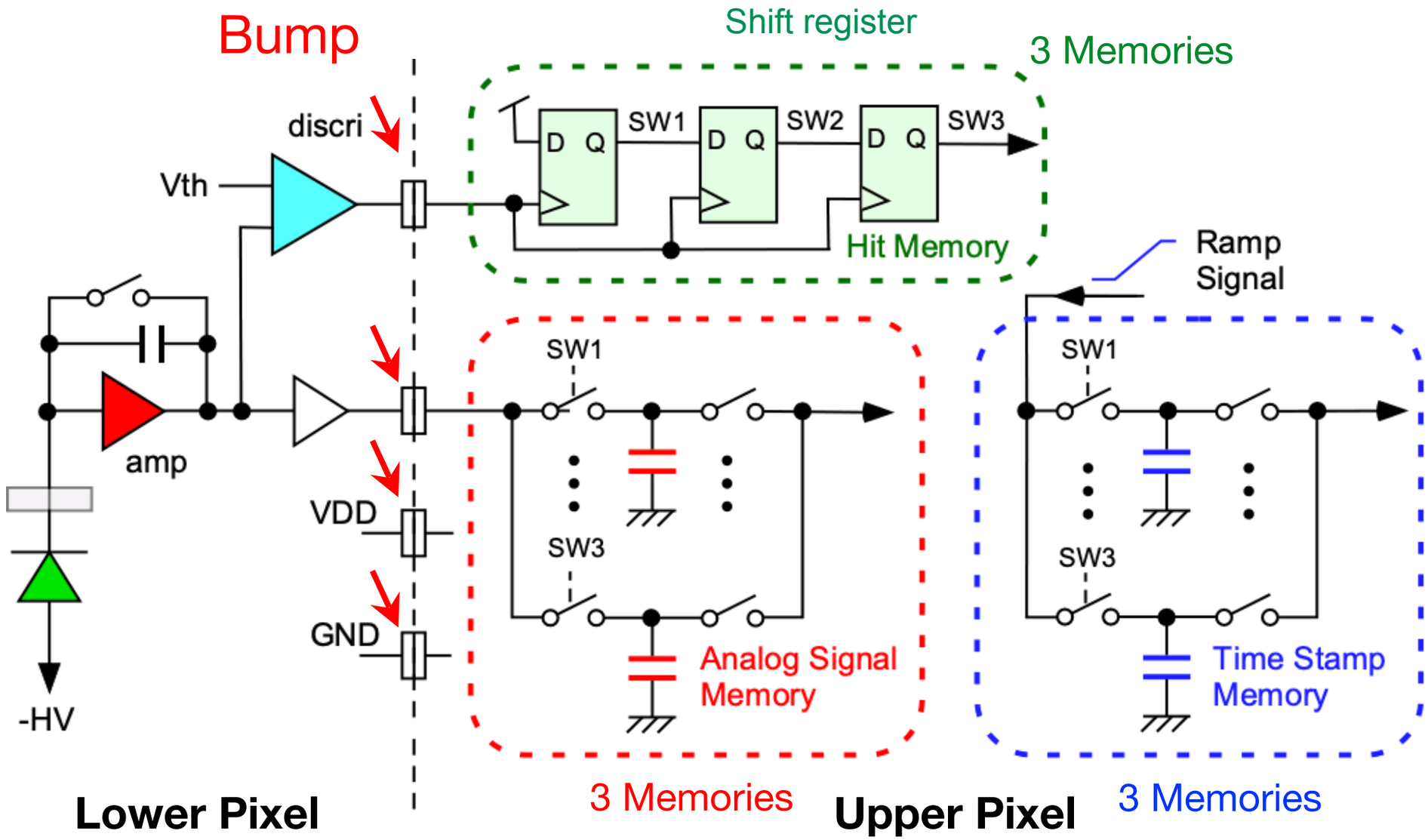
SOFIST4 Pixel

All necessary functions are implemented in a pixel.

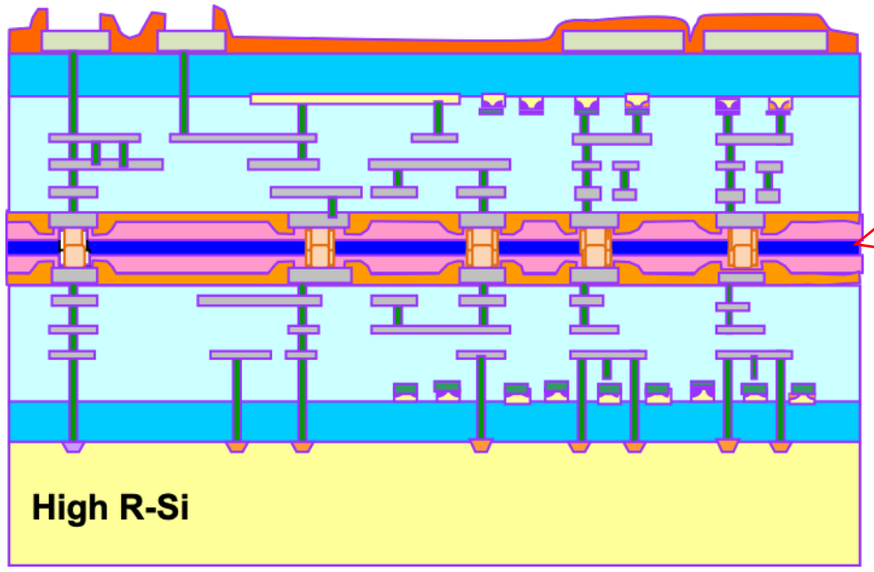
Lower pixel: Pre. amplifier and comparator

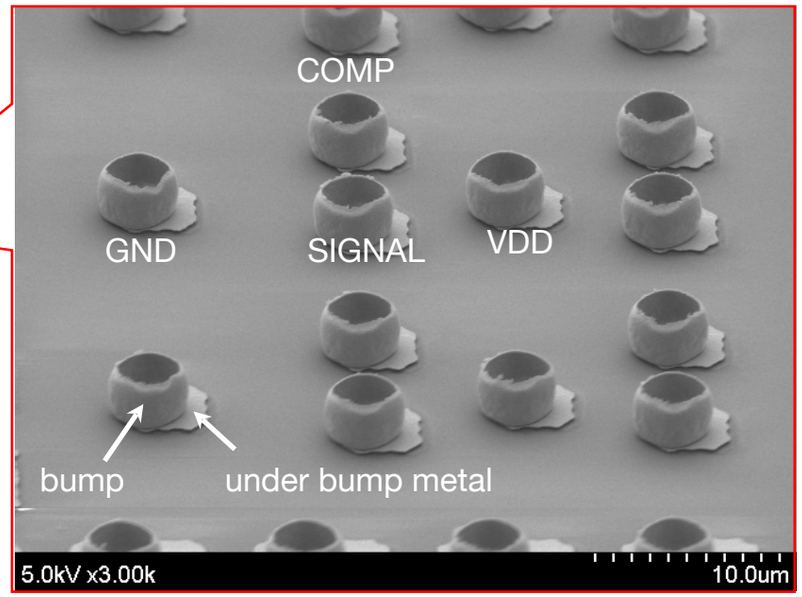
Upper pixel: Hit, Analog signal and Timestamp memories (up to 3 hits)

Output of pre. amplifier and comparator are sent to upper pixel via micro bump.



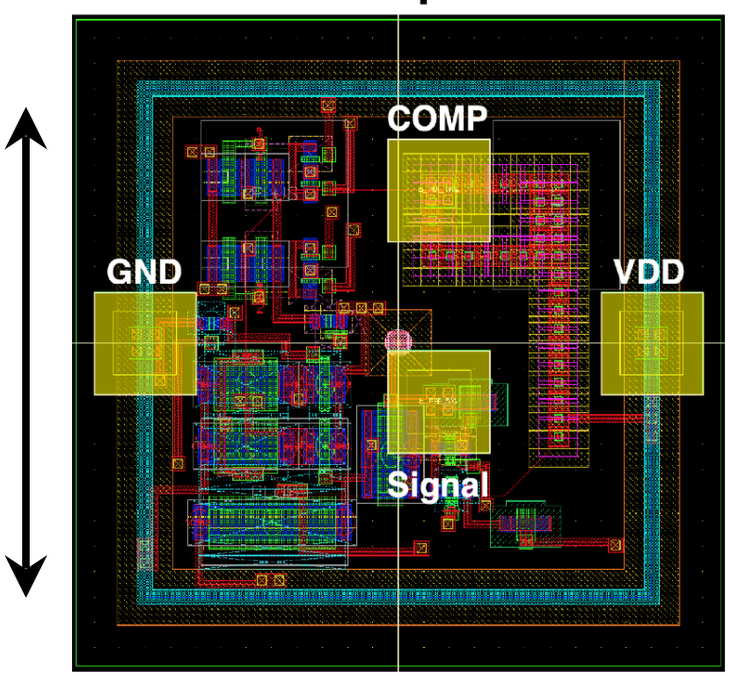
Au Micro Cylinder Bump





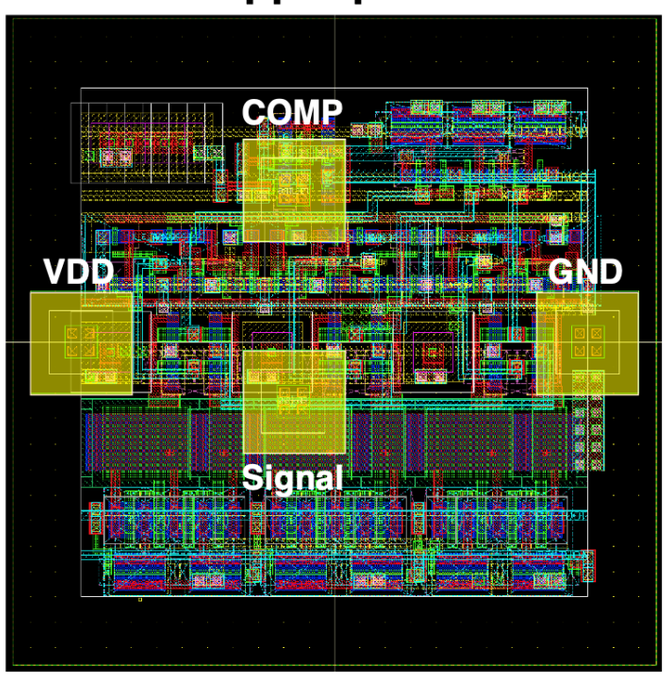
Au cylinder bump
Diameter: 3μm
（by T-Micro）

Lower pixel

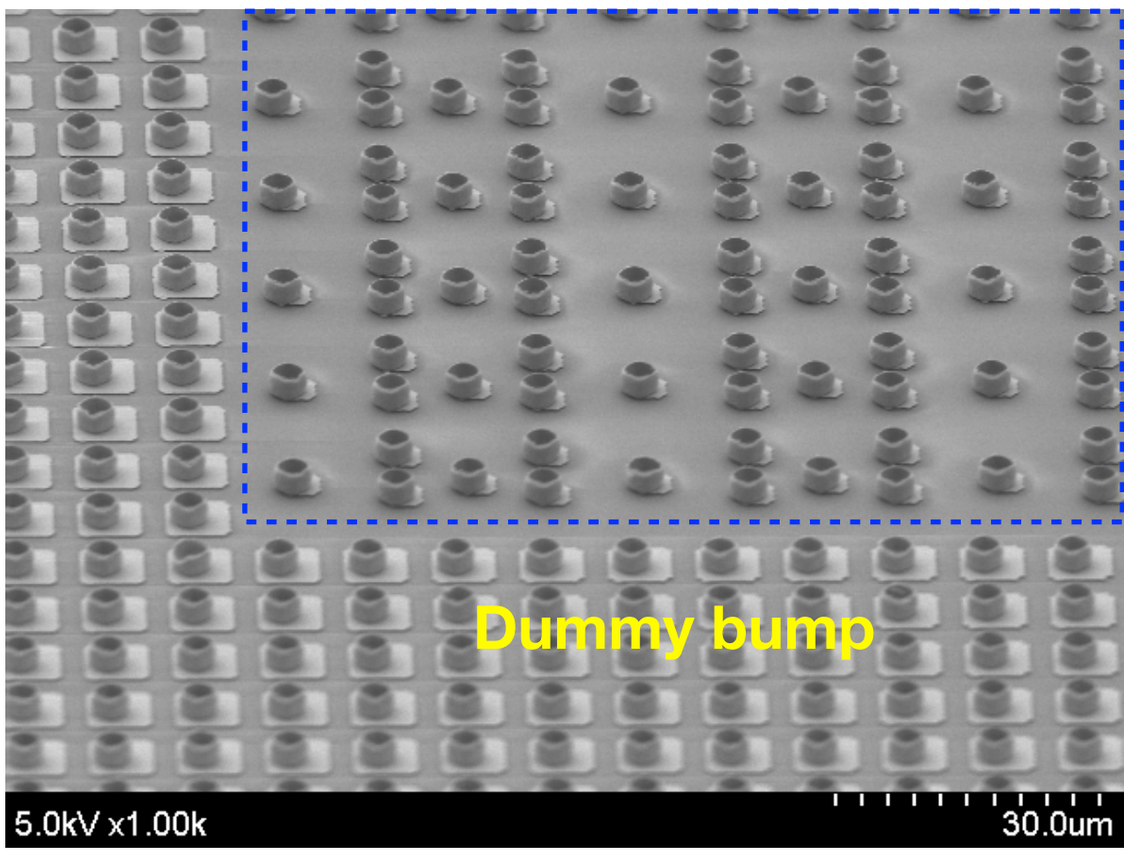


$20 \times 20\ \mu m^2$

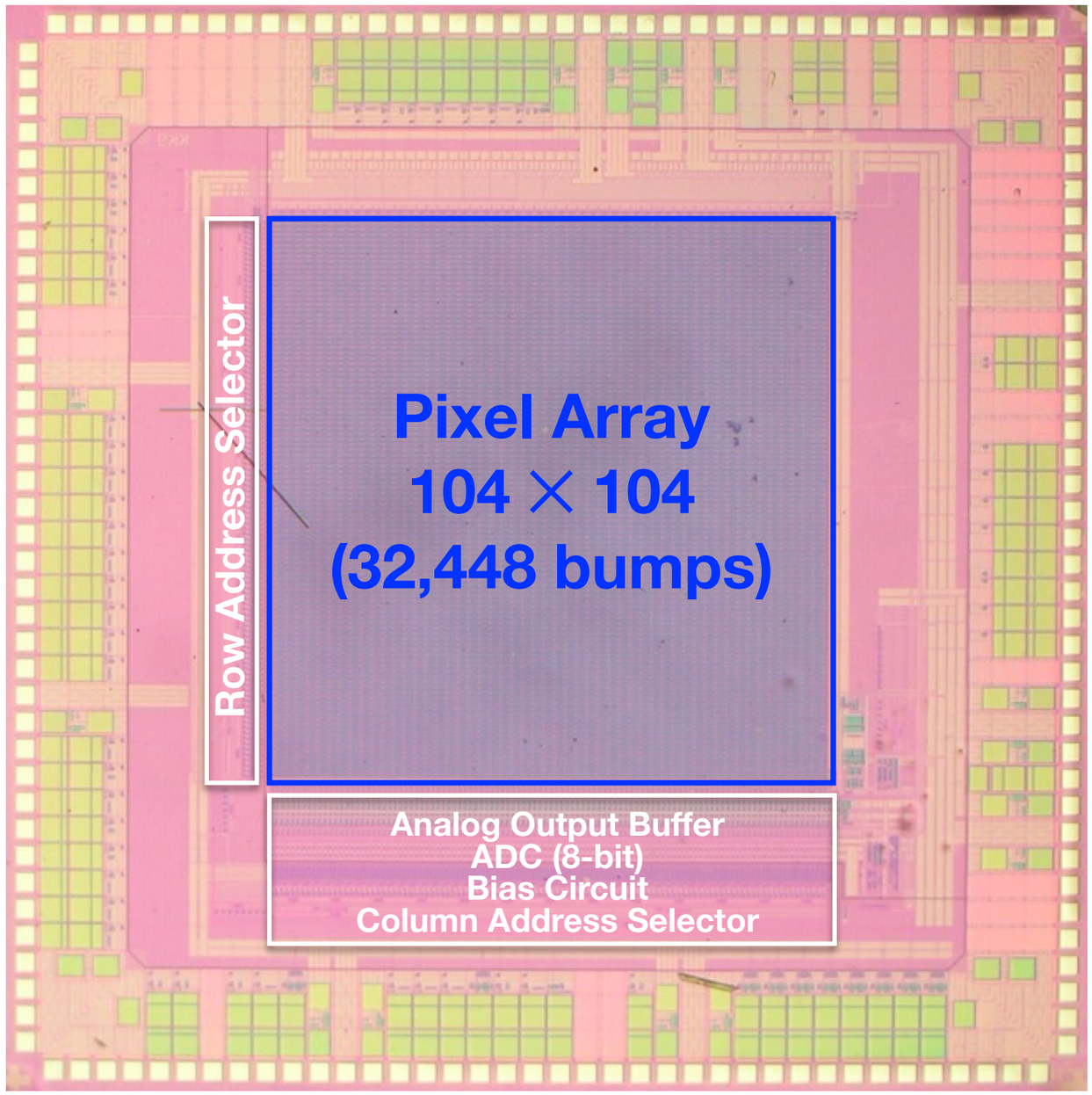
Upper pixel



Pixel array



SOFIST4 Chip



4.45 × 4.45 mm²

Design:

Chip size: 4.45 × 4.45 mm²

Pixel size: 20 × 20 μm²

Active area: 2.08 × 2.08 mm²

Sensor type: Double SOI, FZ *p*-type

Sensor thickness: 300 μm

Sensor resistivity: 3 – 10 kΩ · cm

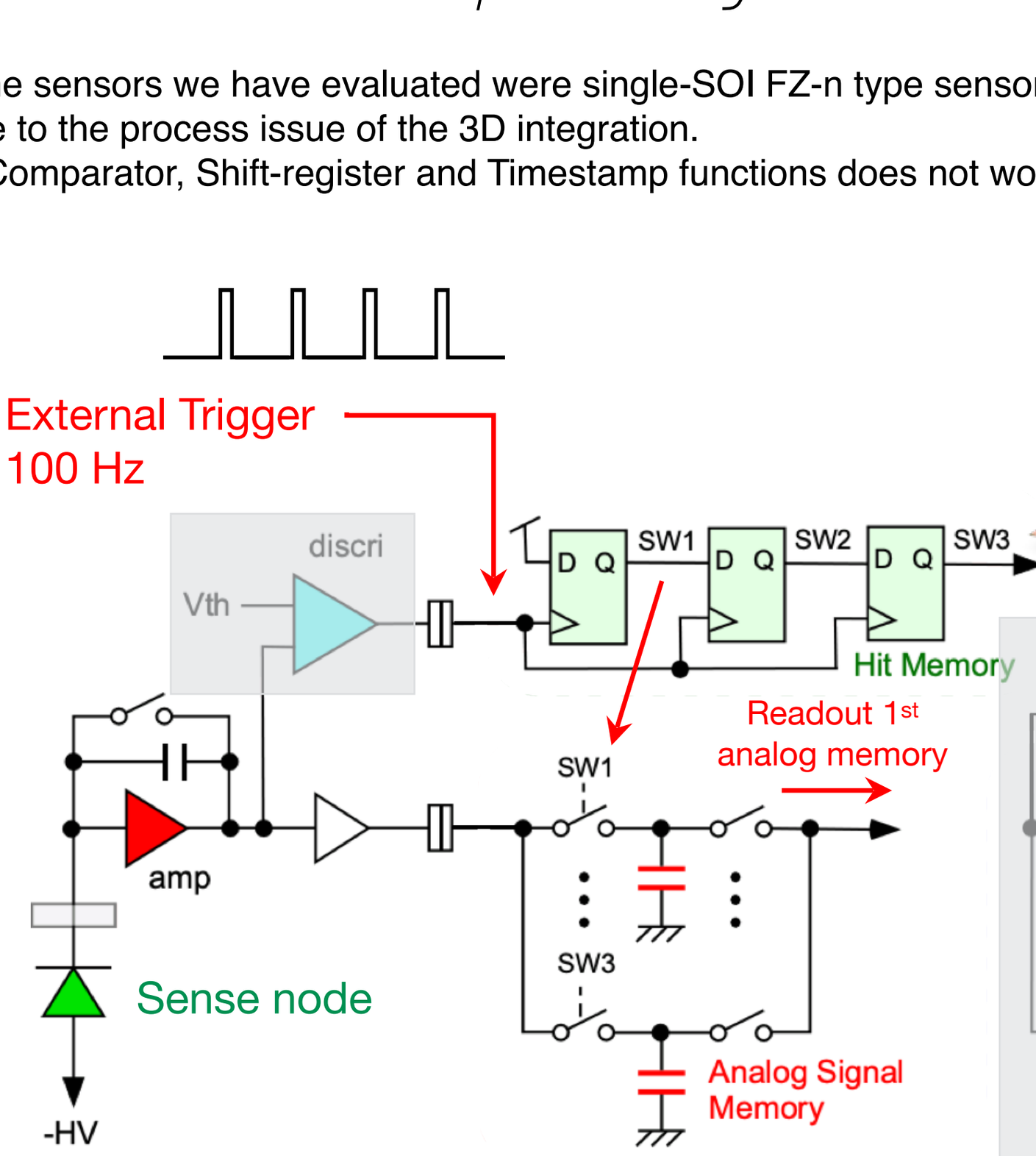
Memory: Analog 3 hits
Timestamp 3 hits
Hit 3 hits

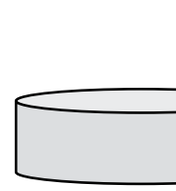
On-Chip: 8-bit Column ADC

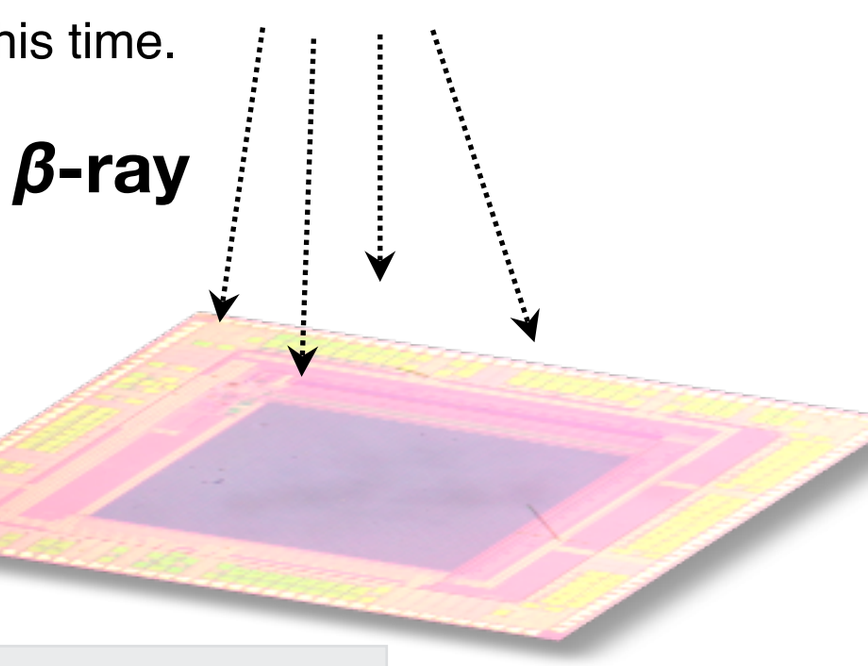
Total bumps: 32,448 for pixel array
3,520 for I/O cell

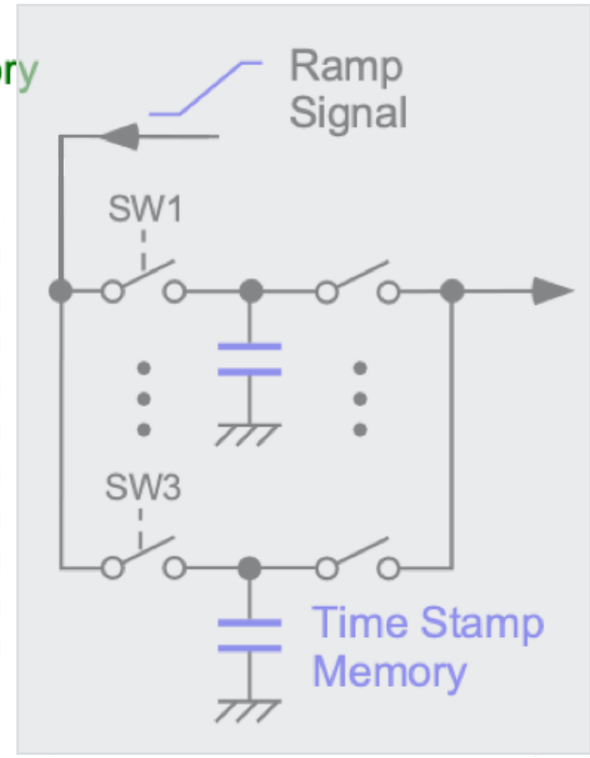
β-ray tracks

*The sensors we have evaluated were single-SOI FZ-n type sensor
due to the process issue of the 3D integration.
→Comparator, Shift-register and Timestamp functions does not work at this time.



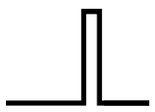




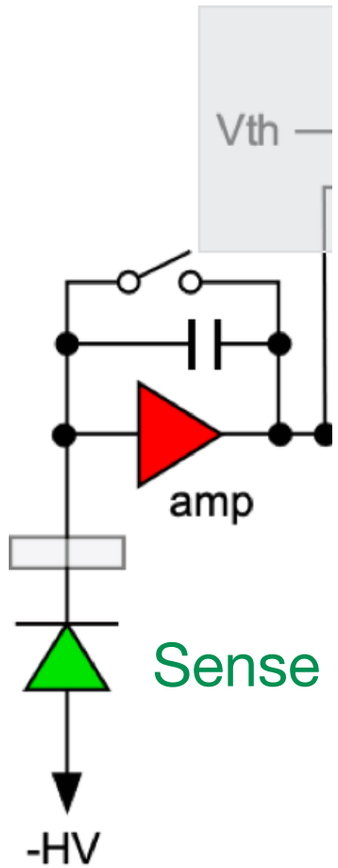


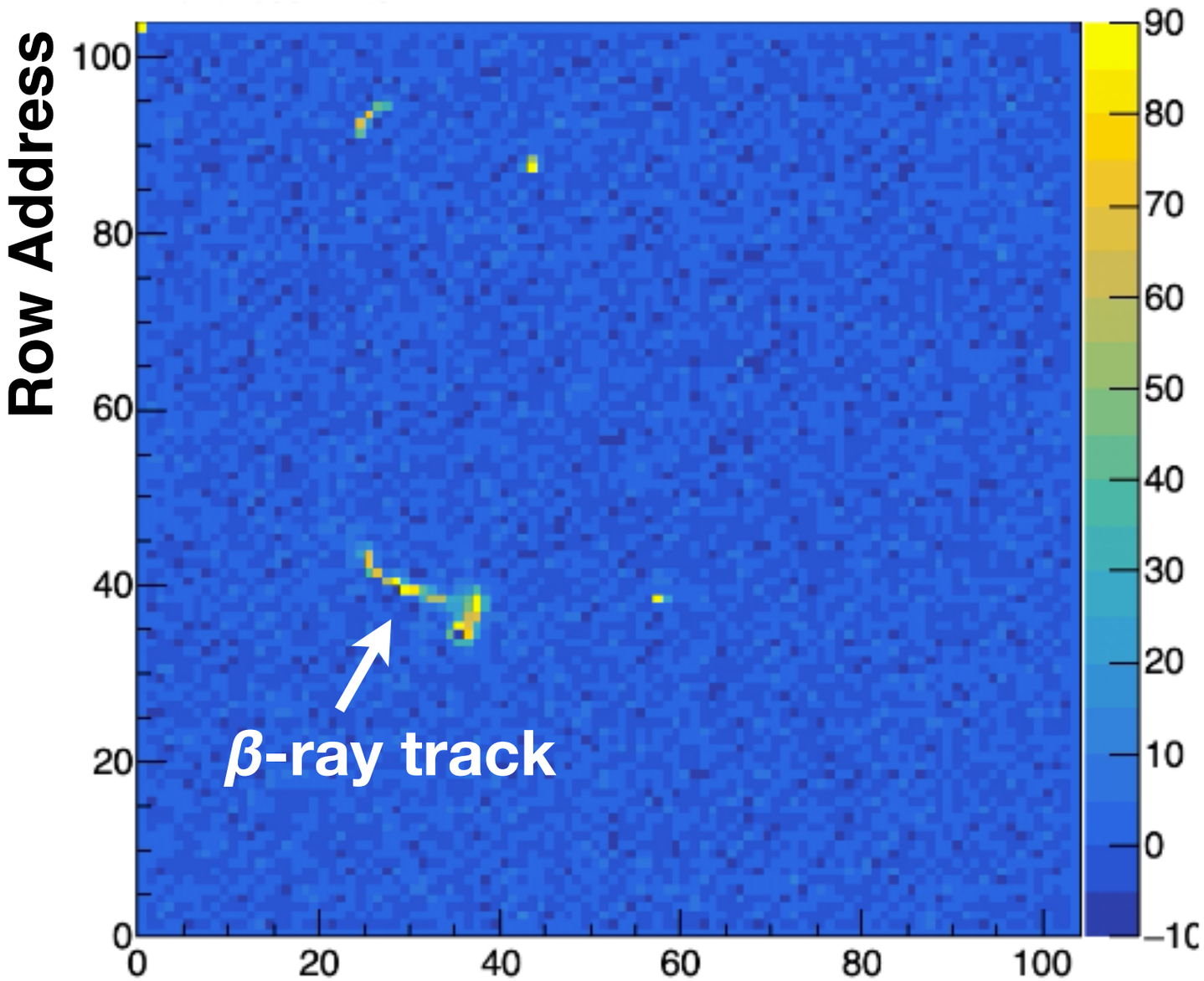
β-ray tracks

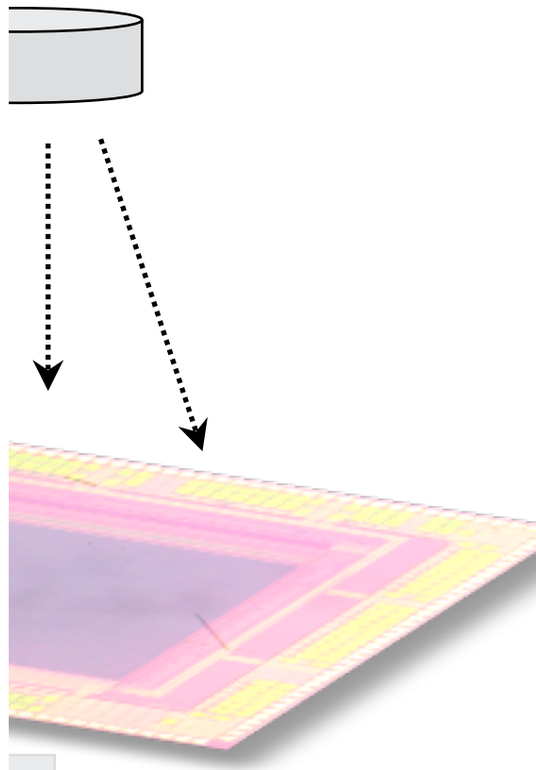
*The sensors we ha
due to the process i
→Comparator, Shift



External Trigg
100 Hz

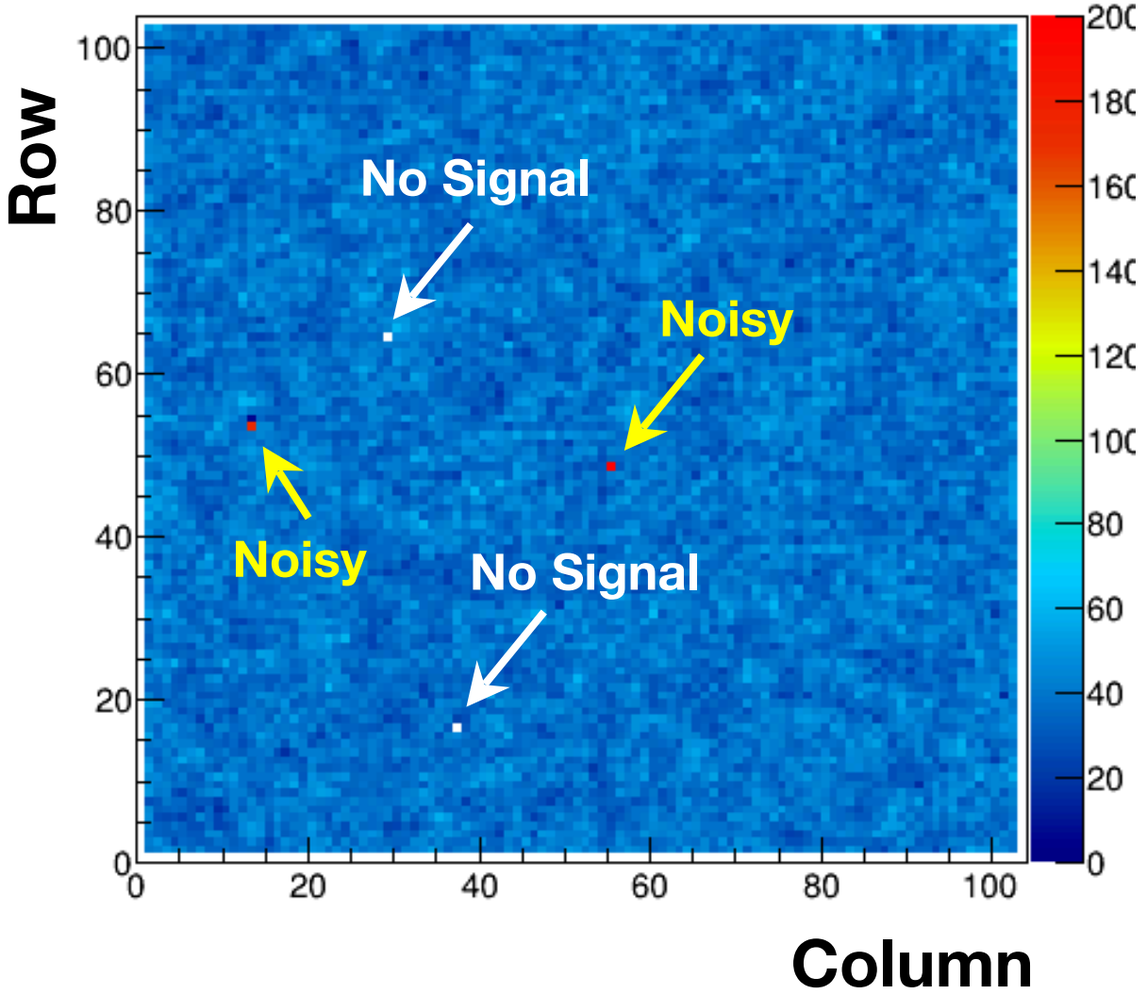


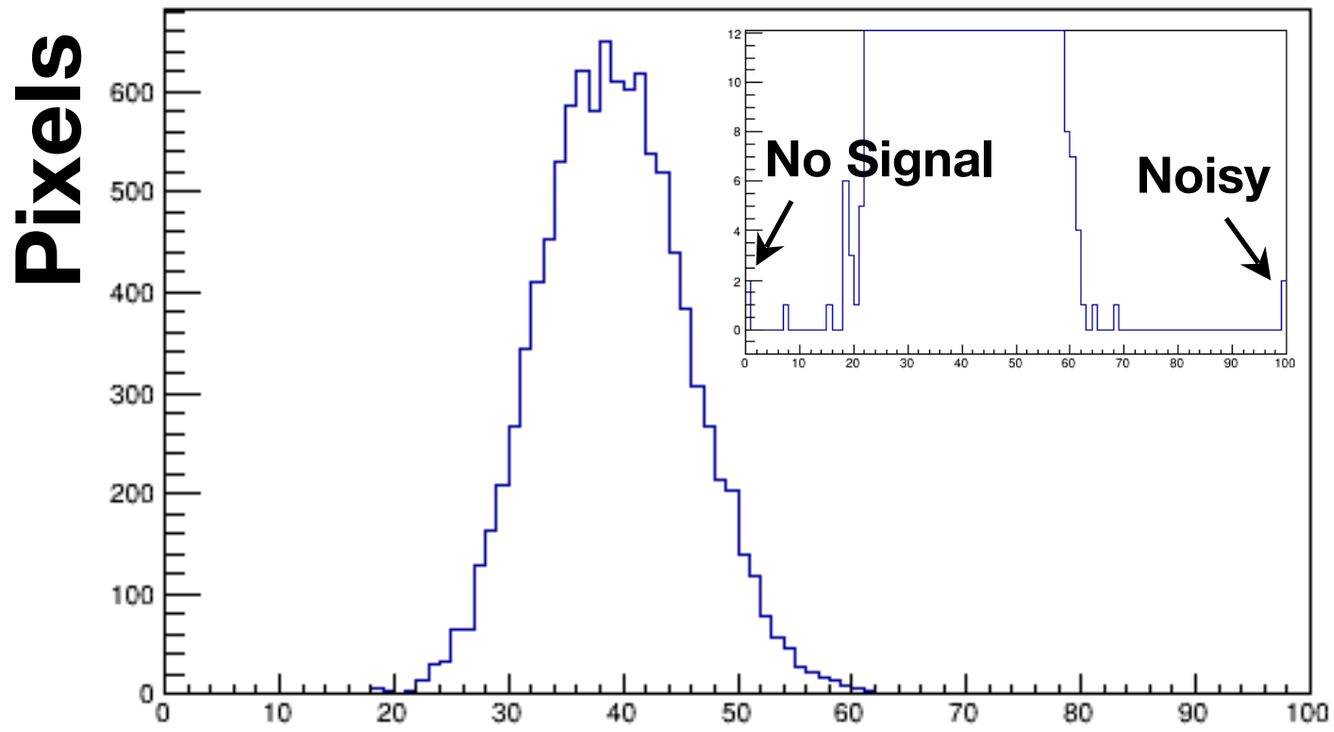




Bump Connection Yield

Hit Map (50 kEvents)



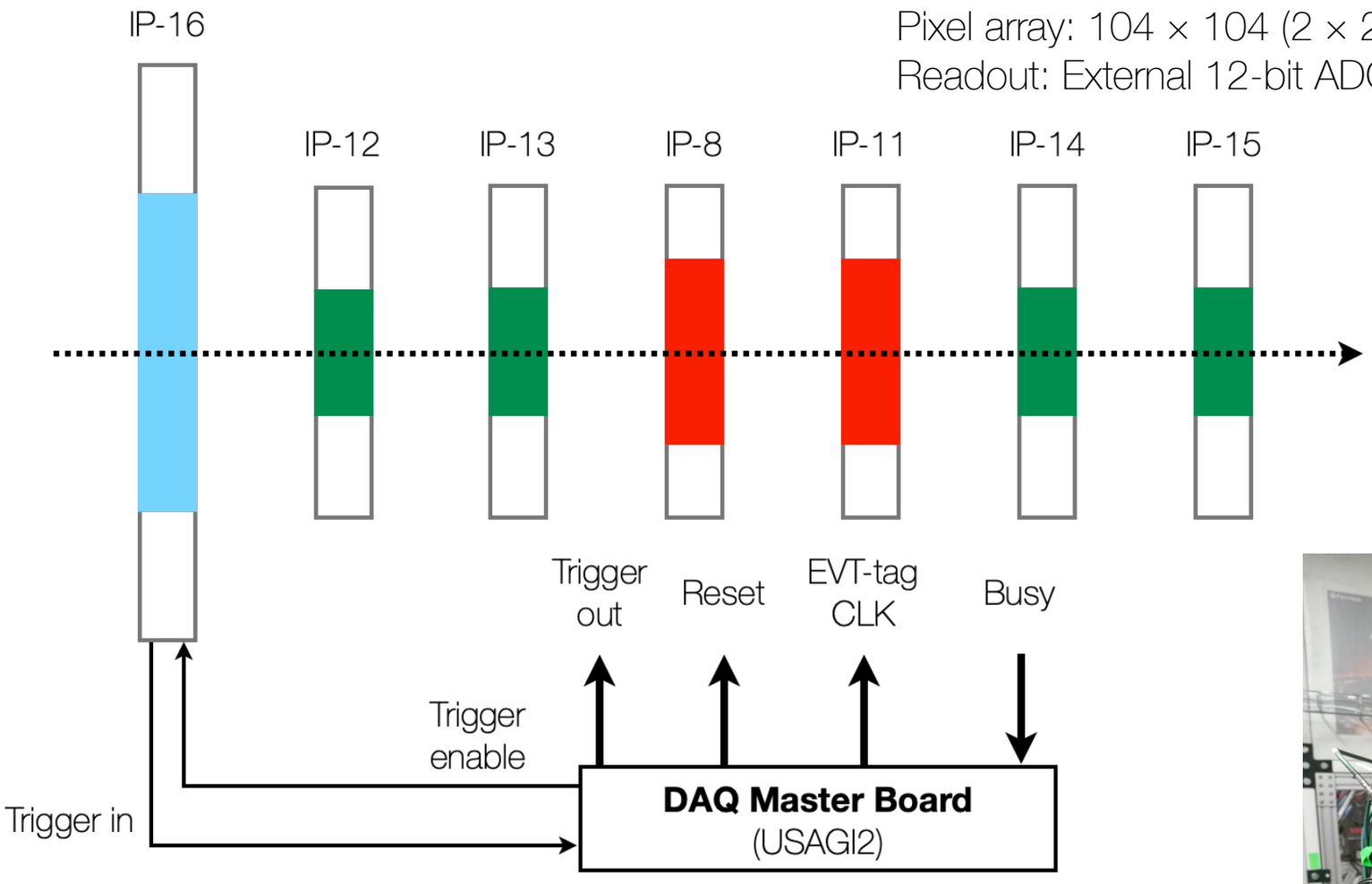


Connection Yield:
(102 × 102 – 2) / 102 × 102 ~ 99.98 %

Reject the outermost pixels for the calculation.

Beam Test

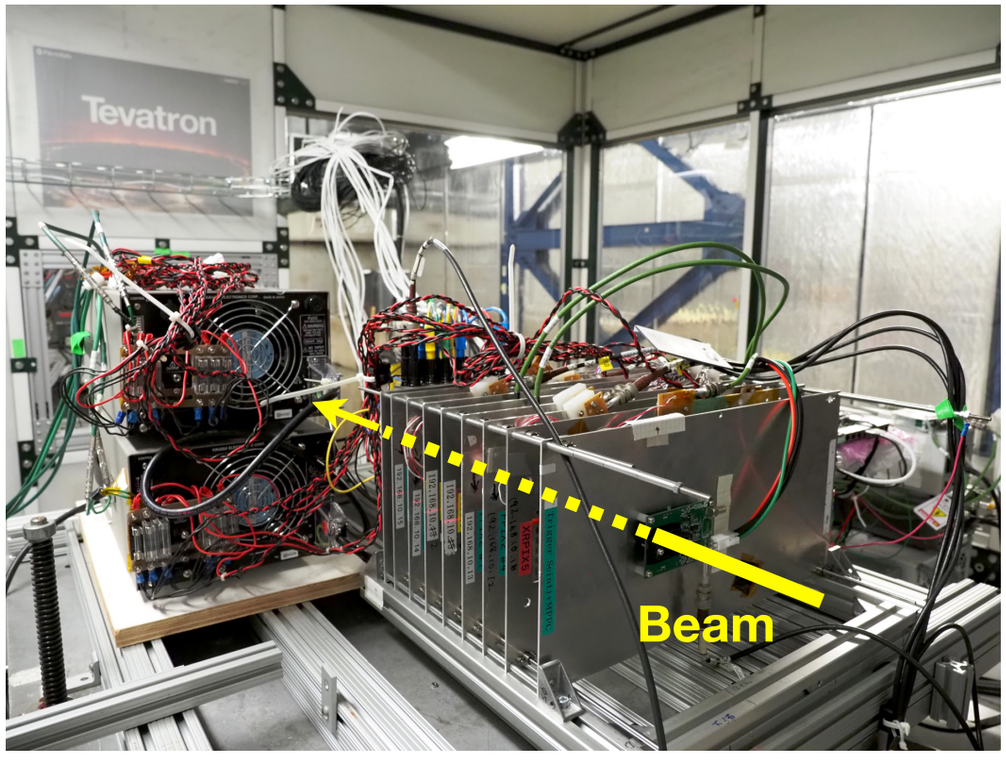
Beam: 120 GeV proton (Fermilab Beam Test Facility)
DAQ rate: ~120 events/s



SOFIST4
Pixel size: 20 × 20 μm²
Pixel array: 104 × 104 (2 × 2 mm²)
Readout: External 12-bit ADC

FPIX2 (SOIPIX)
Telescope for SOFIST
σ ~0.7 μm
Pixel size: 8 × 8 μm²
Pixel array: 128 × 128 (1 × 1 mm²)
Readout: External 12-bit ADC

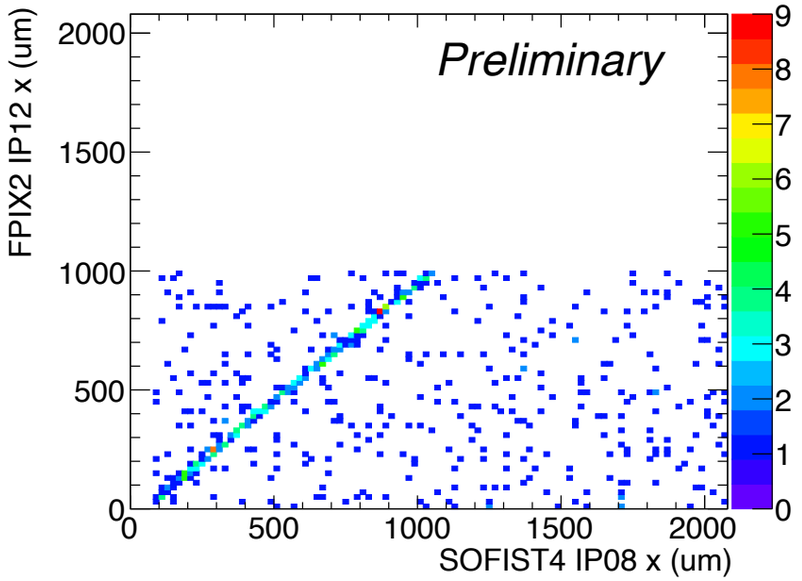
XRPIX5 (SOIPIX)
Trigger counter
Pixel size: 36 × 36 μm²
Pixel array: 608 × 384 (24.6 × 13.8 mm²)
Region of Interest function
Readout: External 12-bit ADC

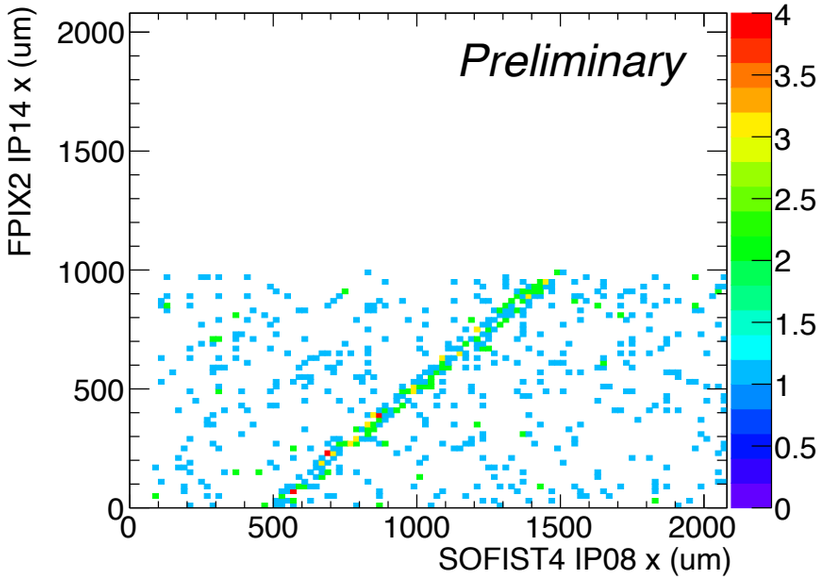


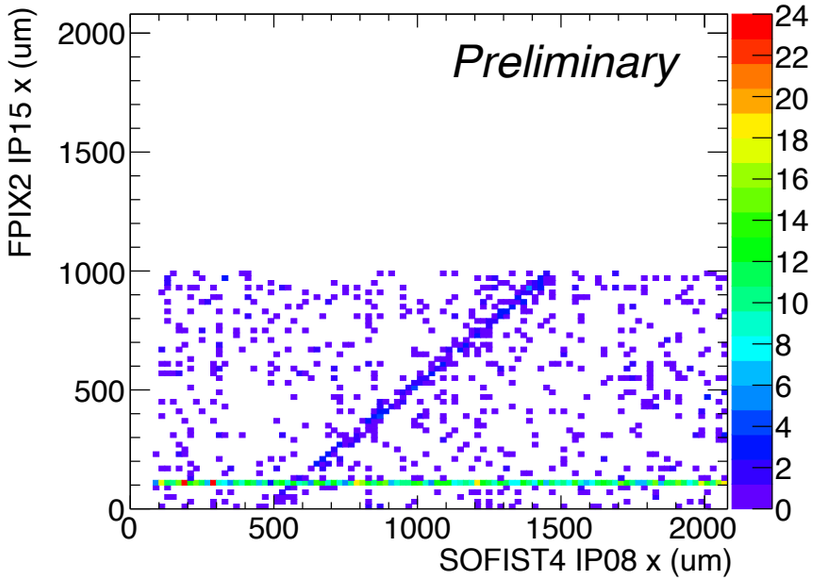
Hit Correlation

Hit position correction between **telescope (FPIX2) and SOFIST4 IP-8** in *x* and *y*-direction.

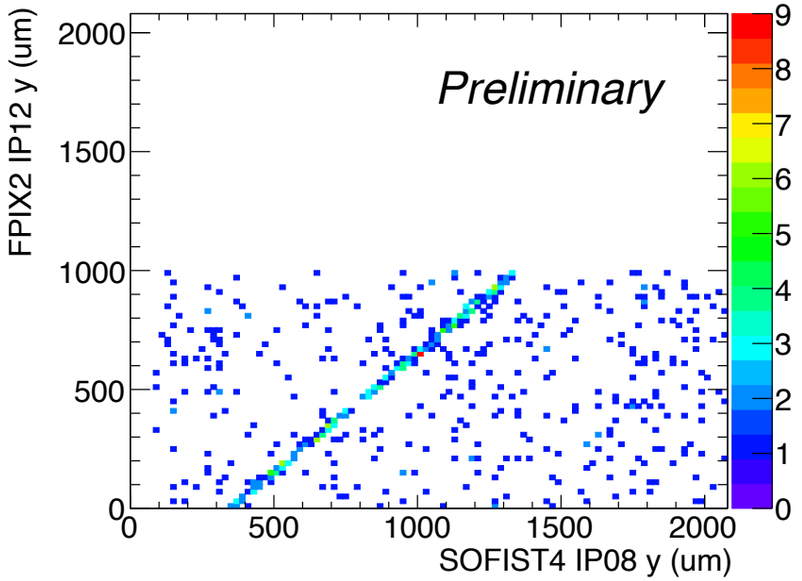
x-direction

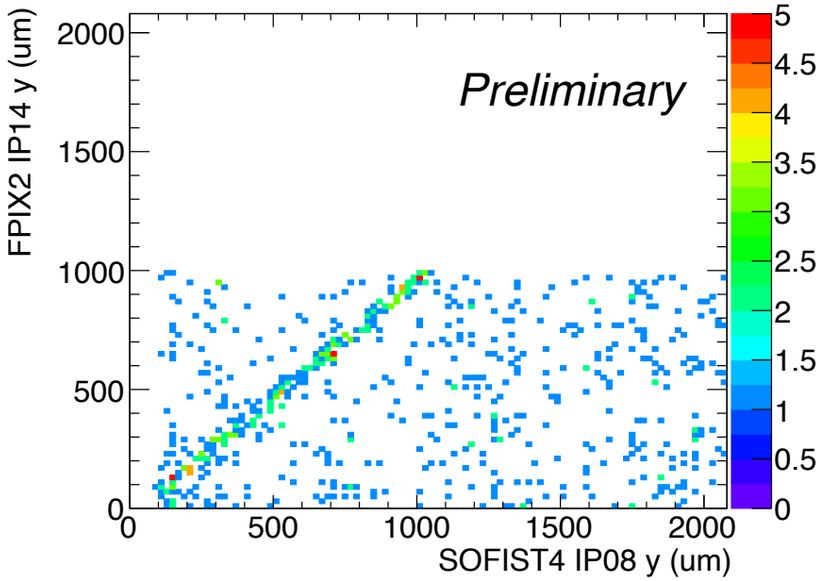


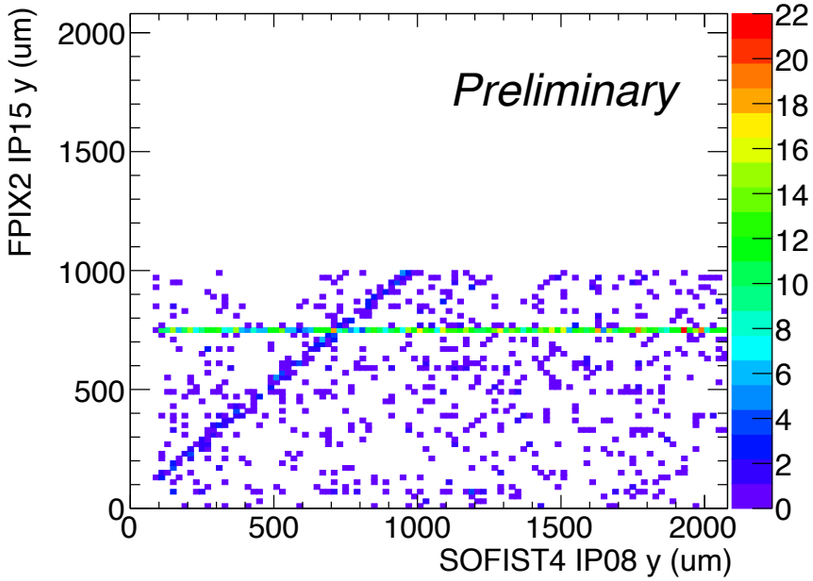




y-direction





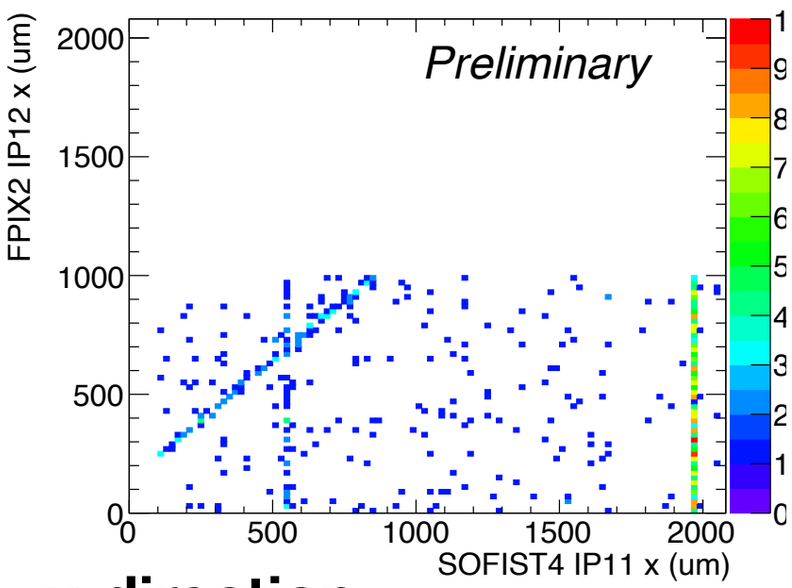


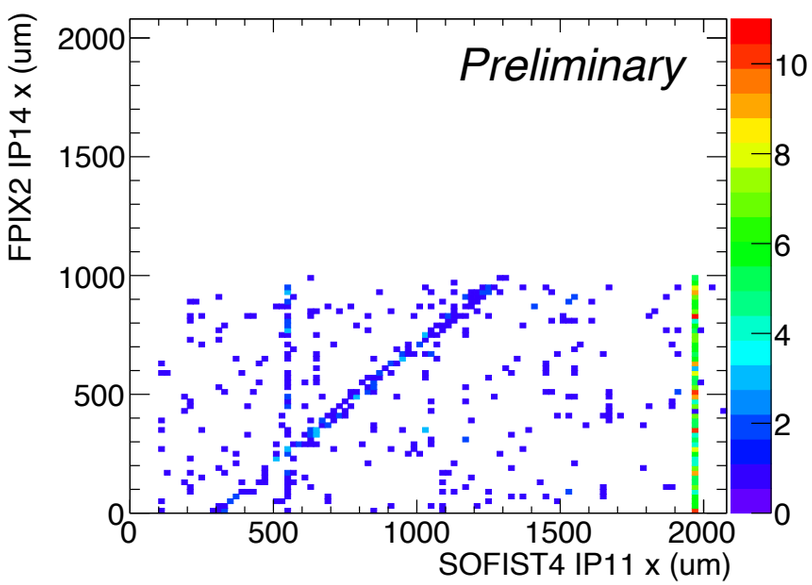
* **Active area:** FPIX2: 1 × 1 mm², SOFIST4: 2 × 2 mm²

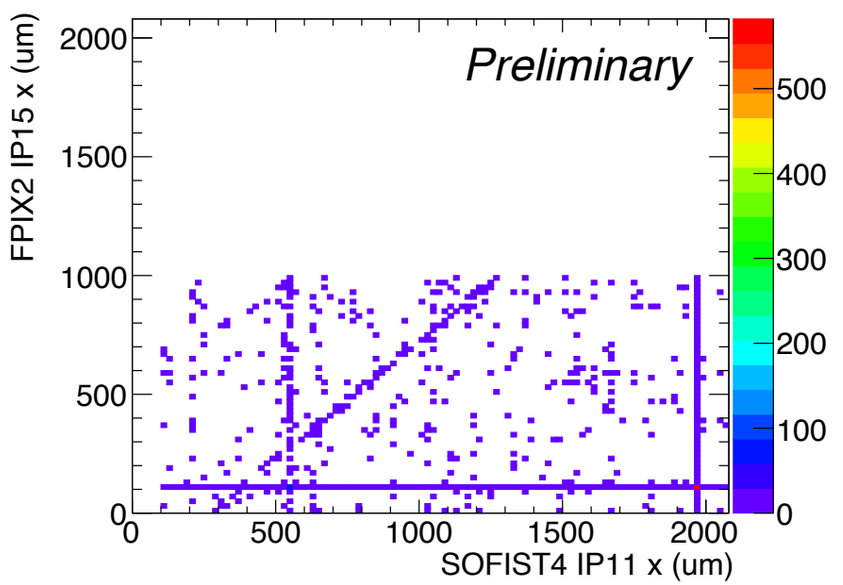
Hit Correlation

Hit position correction between **telescope (FPIX2) and SOFIST4 IP-11** in *x* and *y*-direction.

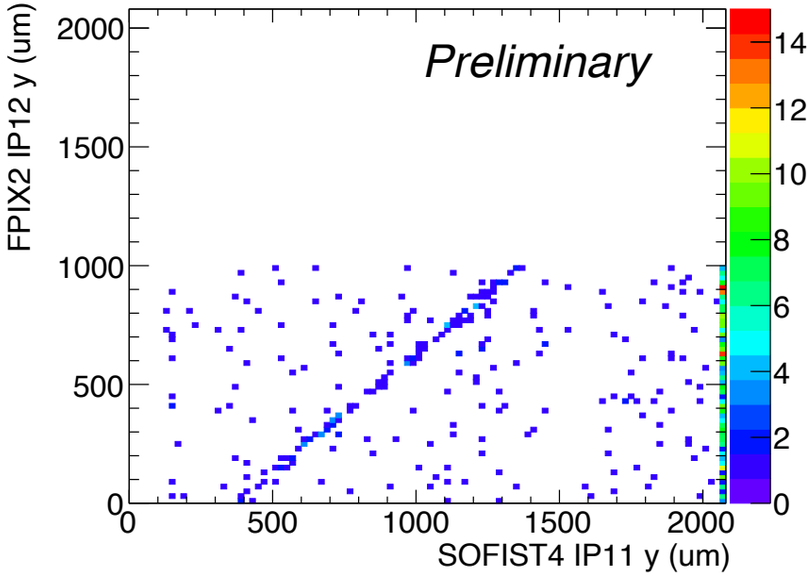
x-direction

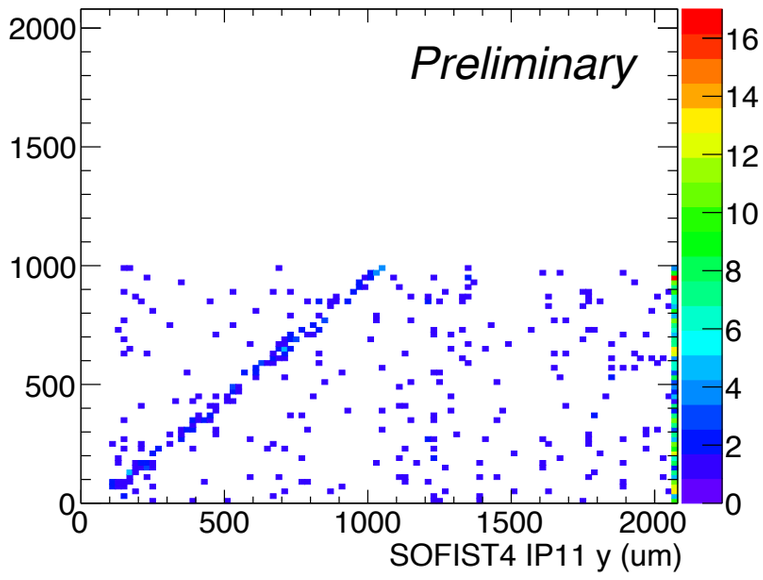


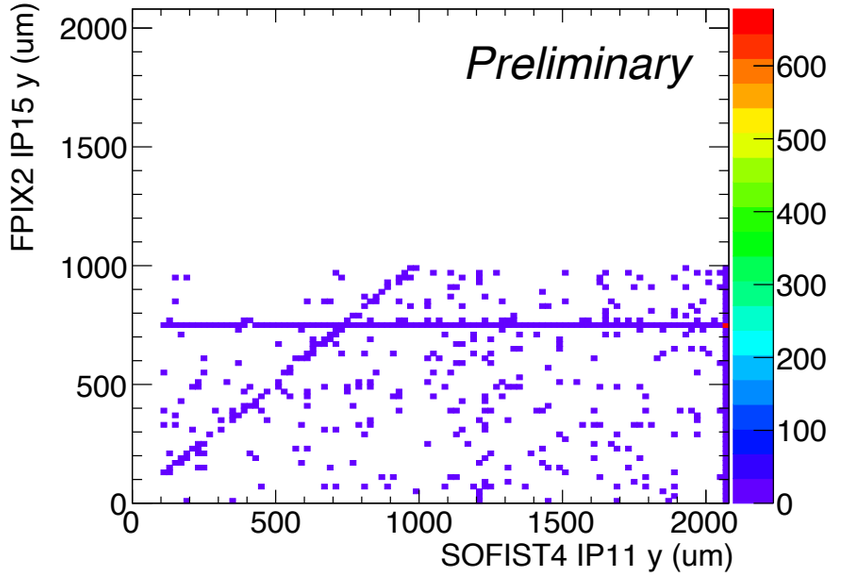




y-direction





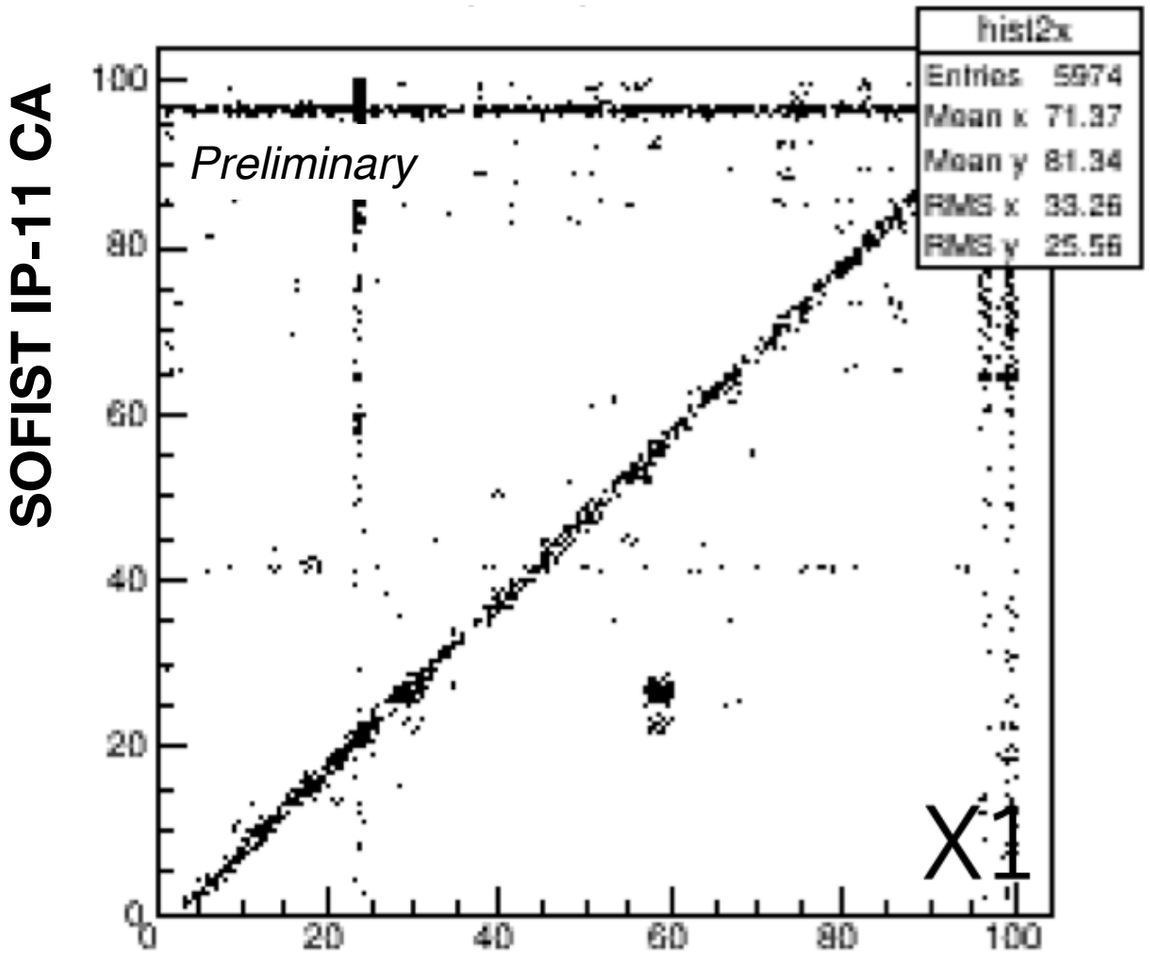


* **Active area:** FPIX2: 1 × 1 mm^2, SOFIST4: 2 × 2 mm^2

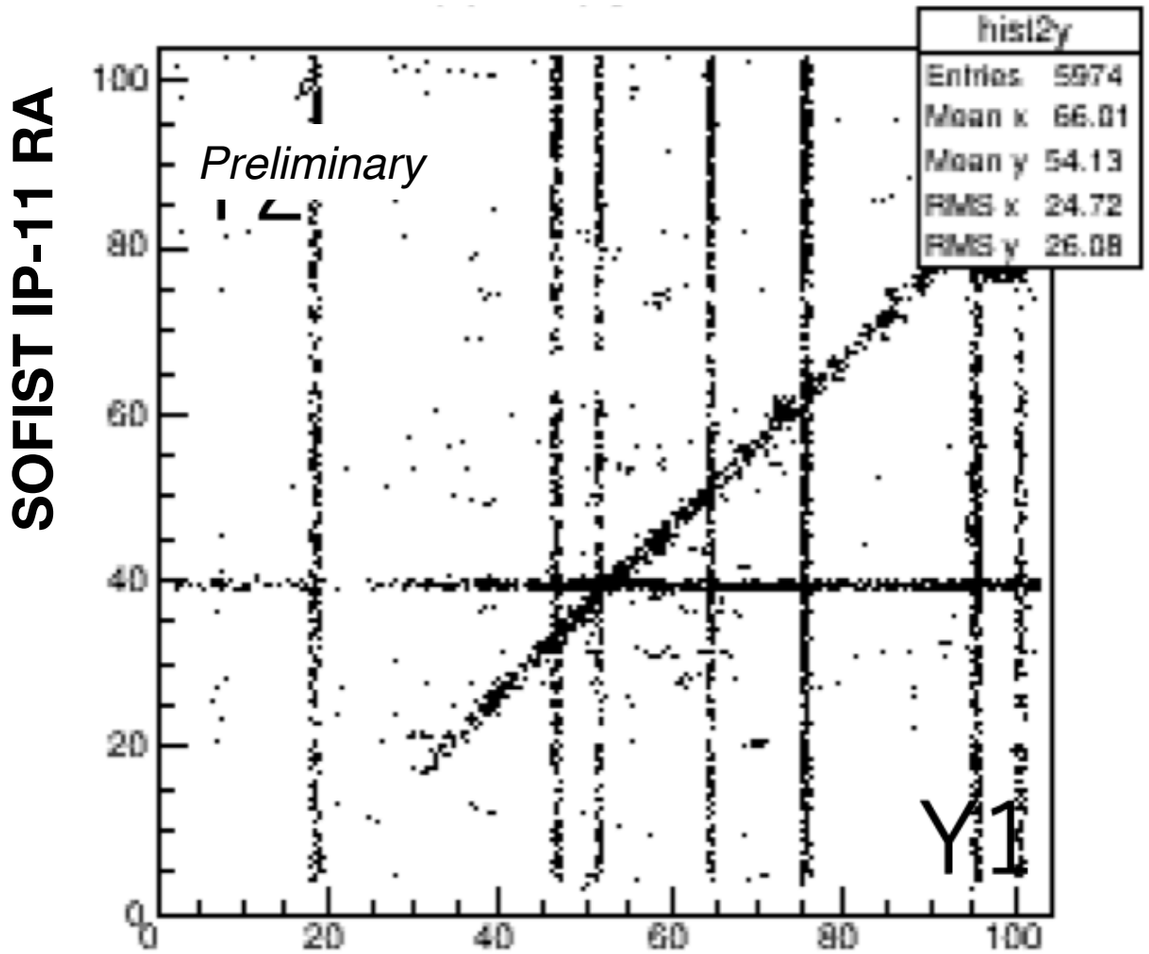
Hit Correlation

Hit position correction between **SOFIST4 IP-08 and SOFIST4 IP-11** in *x* and *y*-direction.

x-direction



y-direction



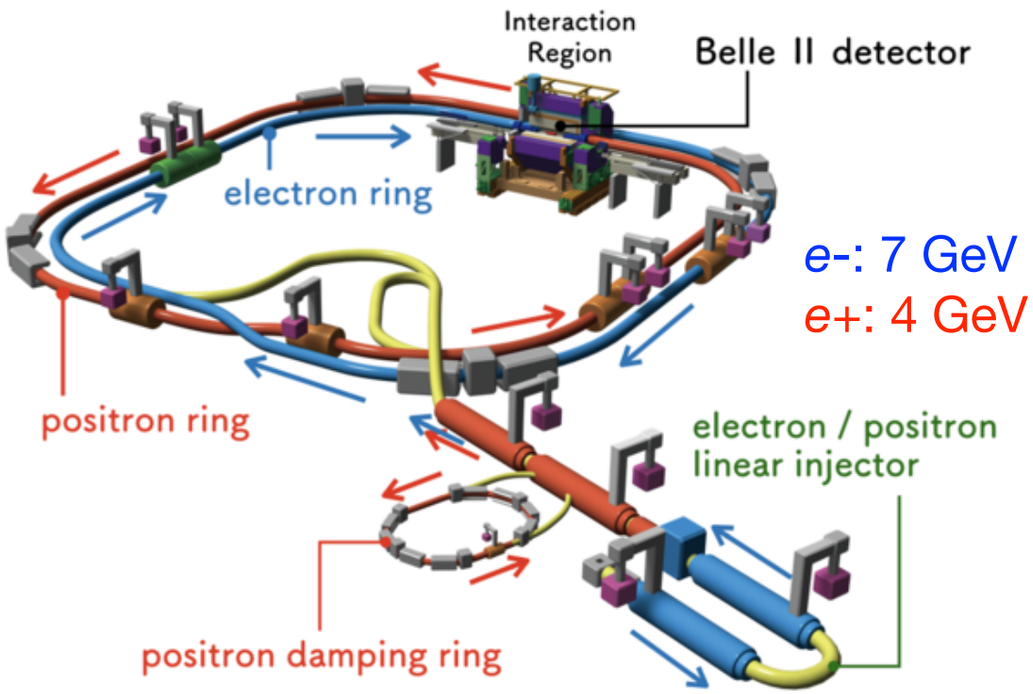
Both SOFIST4 have successfully detected hit of proton beam and shown hit correlation between telescopes and SOFIST4 themselves.

SuperKEKB Upgrade

SuperKEKB: Target luminosity 8×10^{35} cm^{-2}s^{-1}
SuperKEKB upgrade: 5 times higher luminosity (integrated luminosity: 250 ab^{-1})
→ 5 times higher beam background level (hit rate: 113 MHz/cm^2 at layer 1)

We propose new pixel detector for upgraded SuperKEKB

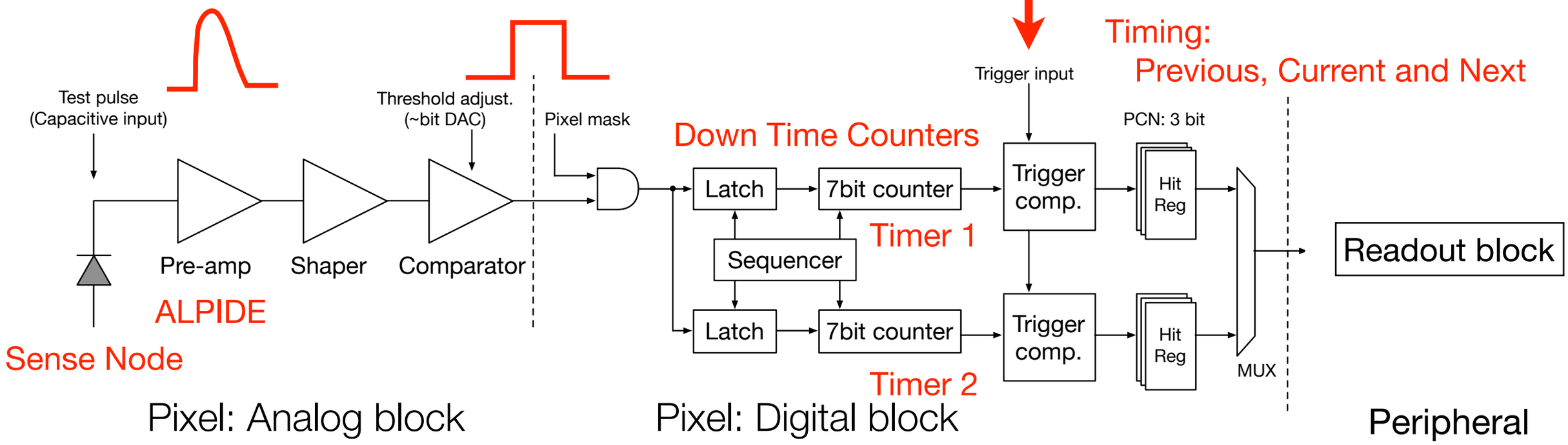
- much faster readout (trigger latency is 8 μs)
- trigger based global shutter
- low occupancy < *O*(0.1) %
- position resolution ~10 μm (B mesons decay position inside beam pipe)
- low material budget (sensor thickness ~50 μm)
- radiation tolerance ~100 Mrad, 5×10^{14} n_{eq}/cm^2



DuTiP Pixel Concept

DuTiP (Dual Timer Pixel)

Two down time counters for hits in a pixel



1) Analog block: usual configuration for the binary detector
2) Binary hit signal is sent from analog block (output of comparator) to digital block
3) Timer 1 starts counting down (7, 6, 5 … μs)
4) Hit timing is readout as current timing if the timer 1 = 1 when pixel received trigger decision
5) Timer 1 is reset if the trigger decision is not received at PCN timing
6) Timer 2 is used for second hit during trigger latency

Occupancy

Layer 1 hit rate = 113 MHz/cm^2, Trigger latency = 8 μs: 0.012 %

DuTiP1 Pixel Design

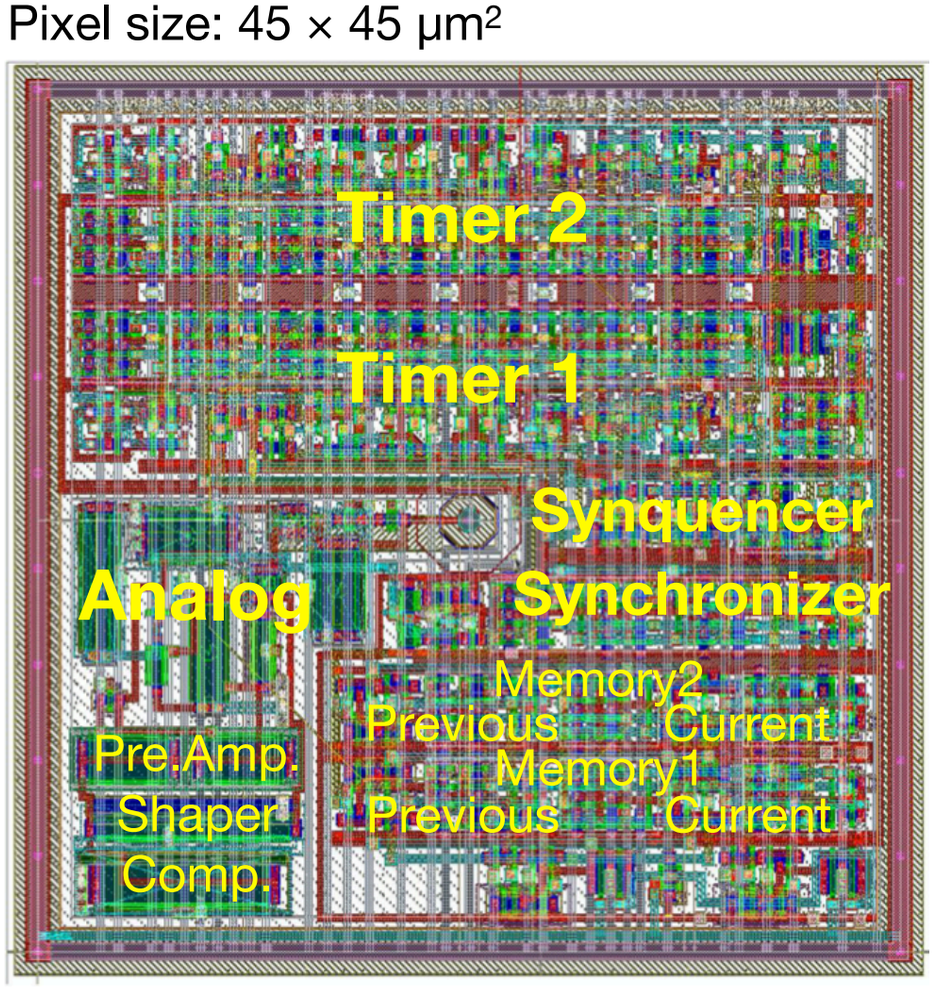
Pixel

- Pre. amplifier (ALPIDE type)
- Shaper
- Comparator
- Dual down time counters (7 bit)
- Timing memory (Previous/Current)

Readout

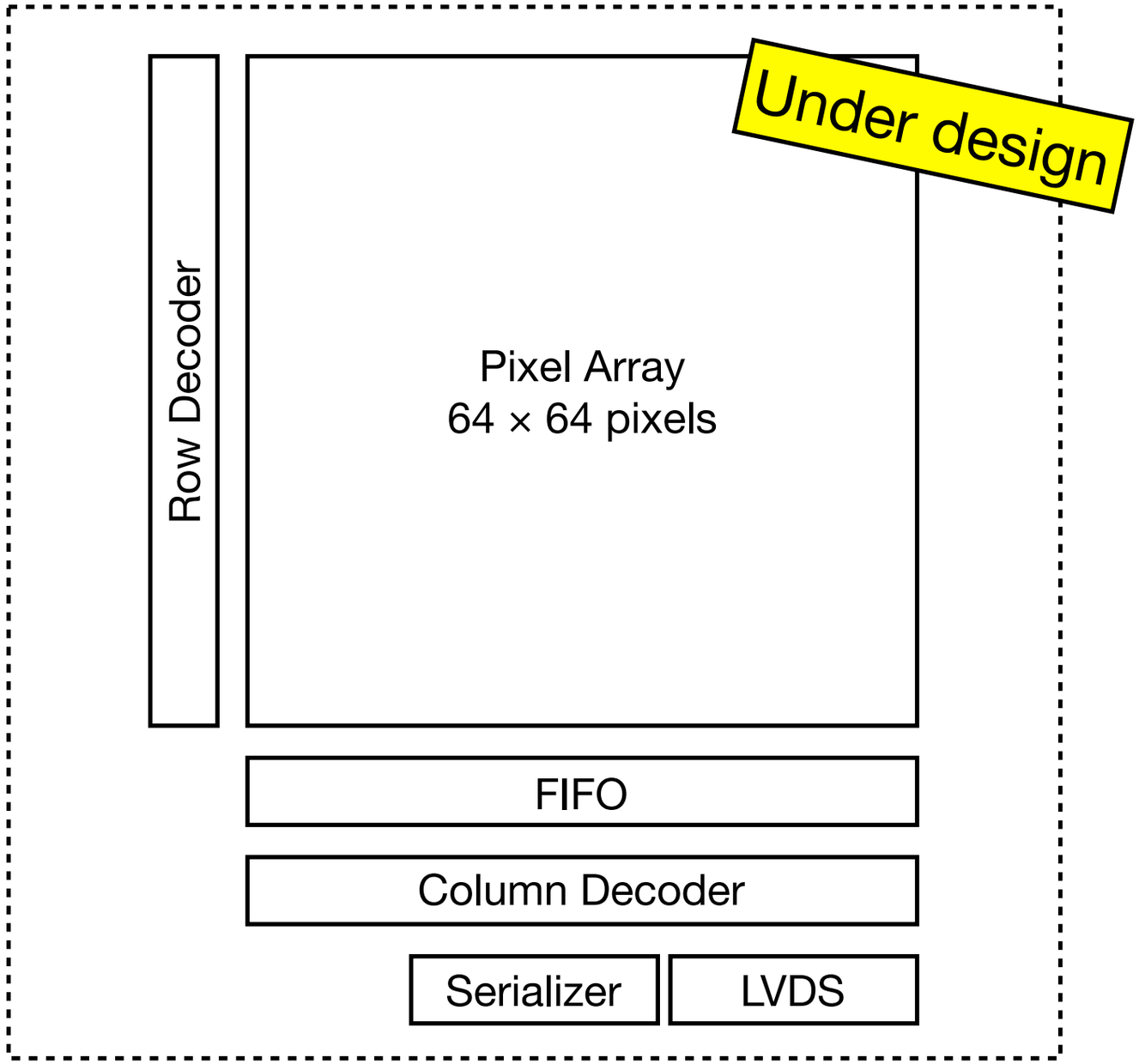
- Row address (5 bit), column address (5 bit)
- 2 bit hit (Previous/Current)
  → Single 241 Mbps LVDS line

Pixel size: 45 × 45 μm²



Chip Floor Plan

Chip size: 6 × 6 mm² (Active are: 2.88 × 2.88 mm²)



We will submit DuTiP1 end of November in 2020.
Sensor will be thinned to ~50 μm in 2021.

Summary

We are designing and developing a monolithic type pixel detector with SOI technology for the ILC vertex detector (SOFIST) and Belle II upgrade pixel detector (DuTiP).

SOFIST 3

Hit, analog signal and timestamp functions worked (infrared laser test).
Time resolution is ~1.92 μs (120 GeV proton beam test).

SOFIST 4 (3D stacking sensor)

3D stacking bump connection yield ~99.9 %
Successfully detected hits by 120 GeV proton beam.
Confirmed hit correlation between telescopes.
→ Still working on the beam test data analysis (alignment, tracking and position resolution).

DuTiP

Developing new pixel detector for Belle II upgrade.
First prototype DuTiP1 will be submitted in November 2020 (deliver: ~Spring in 2021).