Contribution ID: **21** Type: **Talk (invited speaker only)**

[C01] R&D status of monolithic SOI pixel sensor for vertex detector

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SOI wafer consists of high-resistive handle wafer and CMOS LSI circuit layer, and these two layers are isolated by Silicon oxide layer. The handle wafer corresponds to radiation sensor.
Produced charges in the sensor are readout through a tungsten via to the circuit. Sensor thickness can be changed from 500 to 50 um according to application. It satisfy both of a complex circuit implementation in a small size pixel since there is no mechanical bonding like hybrid type silicon detector. Recent high-luminosity collider experiments propose to reconstruct vertices with a few micrometer resolution in high background environment. 3D stacking SOI pixel detector offers high spatial resolution and high functional signal processing circuit by extending circuit area three dimensionally. Prototype pixel sensor for the ILC vertex detector, SOFIST4, has 20x20 um pixel and it expect to perform 3 um of position resolution. We have already obtained 90Sr beta-ray tracks image and hits of 120 GeV proton beam by SOFIST4. Recent results of beam test with 120 GeV proton beam at Fermilab will be shown in this presentation. Conceptual design of pixel detector, DuTip (Dual Timer pixel), for the Belle II upgrade vertex detector will be also presented. Feature of DuTip is that has dual timers (two down counters) in a pixel to store hits and wait for trigger decision during trigger latency. Signal is readout as collision of current (next/previous) timing if the counter is consistent with trigger signal timing.

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