Depleted Monolithic Active Pixel Sensors in LF 150nm and TJ 180 nm CMOS technologies: The Monopix developments

Vertex 2020 conference
October 7th, 2020

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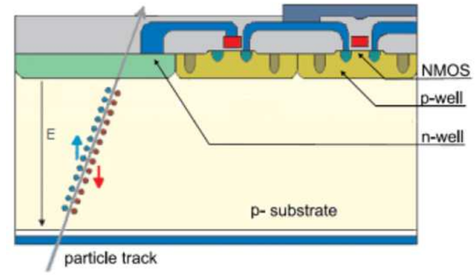
On behalf of

Introduction

Monolithic depleted CMOS

- In some context, could provide advantageous alternative to hybrid pixels.



Depleted active monolithic CMOS Pixels

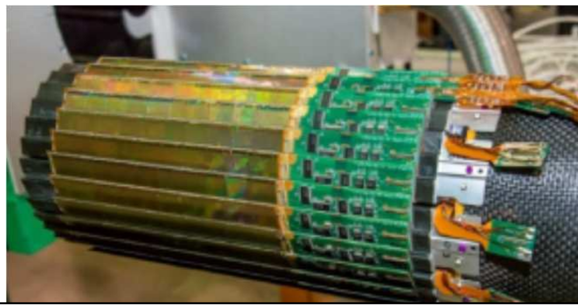
- Key ingredients:
  - Charges collected by drift.
    - to go above ~ 10^{13} $n_{eq}.cm^{-2}$, collecting charge by diffusion is problematic → drift (hence standard MAPS → Depleted MAPS).
  - Consequence → Fast signal response & radiation hardness.
  - Technology requirements → High Voltage process (apply 50-200 V), High Resistive wafers (>100Ωcm) and multiple nested wells (for full CMOS & shield)

(depleted layer: $d \sim \sqrt{\rho . V}$)

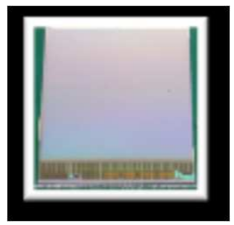
- Advantages:
  - Usage of commercial process: production capability, reliability, low cost…
  - Simple less expensive module (wrt hybrid): no hybridization and much easier production! Can be used for larger area applications
  - Small pixel size possible (in some process)
  - Less power, less material…

MAPS and DMAPS

- STAR experiment

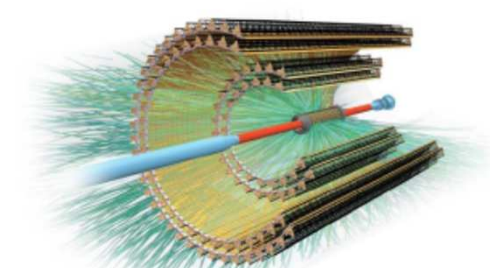


ULTIMATE IC



1st MAPS-based vertex detector for HEP

ALPIDE for ALICE upgrade



ALICE upgrade in LS2

ALPIDE - TJ180

Talk D. Colella, Oct. 5th

- DMAPS Monopix development based on original specs for ATLAS ITk outer pixel layer: NIEL > 10^{15} $n_{eq}.cm^{-2}$, TID >80 Mrad, Hit Rate > 100 $MHz.cm^{-2}$
- Higher radiation hardness & faster readout need:

→ Cope with NIEL / trapping:
  - Fast collection by drift

→ Have high time resolution:
  - Fast collection by drift
  - Fast analog FE
  - Time stamping on chip

→ Cope with high TID:
  - Process + design methodology

→ Cope with high hit rate:
  - Fast return to baseline in analog FE (<~ 1 µs, avoids pile-up)
  - High logic density
  - High output bandwidth

Specifications vs. environments

- In terms of radiation hardness and speed:

	STAR	ALICE	e.g. futur e+e-: ILC	ATLAS HL-LHC Outer layer	ATLAS HL-LHC Inner layer
Fluence [neq.cm-2]	10^{12}	2.10^{13}	10^{12}	**2.10^{15}**	2.10^{16}
TID [MRad]	0.2	<3	0.4	**100**	1000
Timing [ns]	~200000	20000	O(1000)	**25**	25
Hit rate [kHz.mm-2]	4	10	250	**1000**	10000

DMAPS CMOS Community

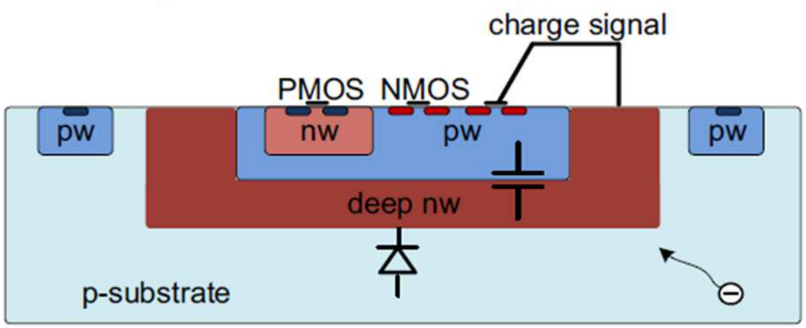
- Collaboration of ~25 institutes (european project STREAM)

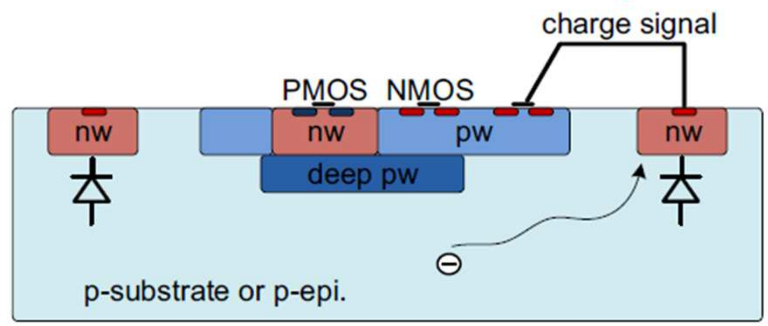
- Many technologies tried, but focus last ~3 years has been on: AMS/TSI 180 nm, LF 150 nm, and TJ 180nm

CMOS sensor development lines

Monolithic sensors with electronics all in one!

(a) large electrode design / (b) small electrode design





- LFoundry 150 process (or AMS/TSI 180)
- Pros:
  - Full CMOS
  - Uniform field, short drift distance → radiation hardness (TID & NIEL), 2.10^{15} $n_{eq}.cm^{-2}$ proven
  - HV rev. bias > 300V possible
  - BS thinning and processing possible
- Cons:
  - Deep nwell Q collection → big Capacitance (>200 fF) → noise, power & crosstalk

I. Peric, DOI: 10.1016/j.nima.2007.07.115
T. Kishishita, et al., DOI: 10.1088/1748-0221/10/03/C03047
P. Rymaszewski, et al., DOI: 10.1088/1748-0221/11/02/C02045
T. Hirono, et al., DOI: 10.1109/NSSMIC.2016.8069902

- TowerJazz 180 process
- Pros:
  - Full CMOS
  - Small capacitance (<10fF) → low noise, less crosstalk & low power.
  - Thin detector possible.
- Cons:
  - Limited depletion, long drift distance, low field region → radiation hardness TBD

R. Turchetta, et al., DOI: 10.1016/S0168-9002(00)00893-7
W. Dulinski, et al., DOI: 10.1109/TNS.2004.832947
A. Dorokhov , et al., DOI: 10.1016/j.nima.2010.12.112
M. Havránek, et al., DOI: 10.1088/1748-0221/10/02/P02013

TJ-Monopix development

1- Introduction

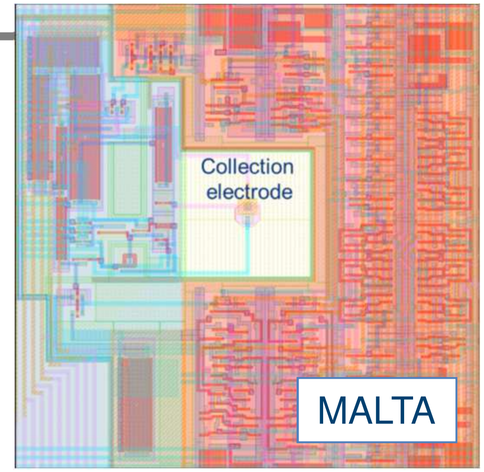
2- TJ 180 nm TJ-Monopix development

3- LF 150 nm LF-Monopix development

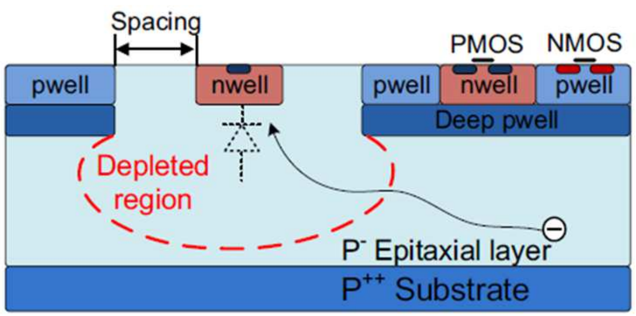
4- Conclusion

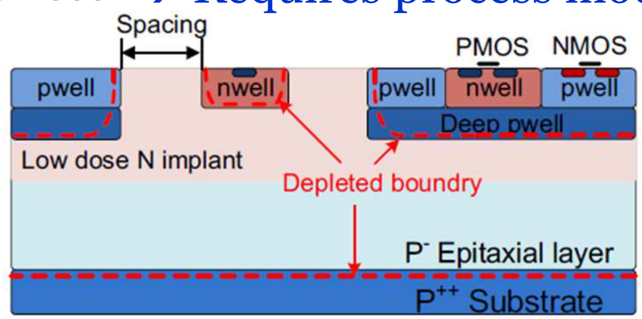
TJ 180nm: process modification

- A small electrode design:
  - Small pixel size (< 50 µm²)
  - Low capacitance (<3 fF)
  - Low power
  - Reduced digital-analog Xtalk



  …
  - … but suffers from limited radiation-hardness → Requires process modification!

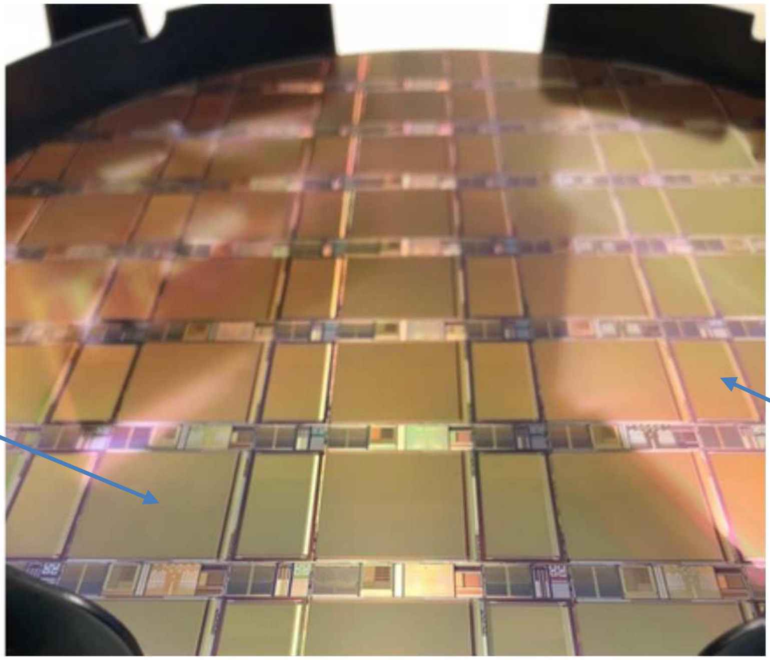




- Standard TJ 180 nm Process:
  - High resistivity p-type epi layer (> 1kΩ.cm)
  - Depleted region stays limited (in particular after irradiation)
  - ALPIDE-like
- Modified TJ 180 nm Process:
  - Additional n- implant → full depletion possible
  - Keeps small capacitance & no big changes to electronic layout
  - MALTA / MONOPIX

W. Snoeys et al. DOI: 10.1016/j.nima.2017.07.046

TJ: The Digital Architectures



TJ-MALTA1
2×2 cm² IC

TJ-Monopix1
1×2 cm² IC

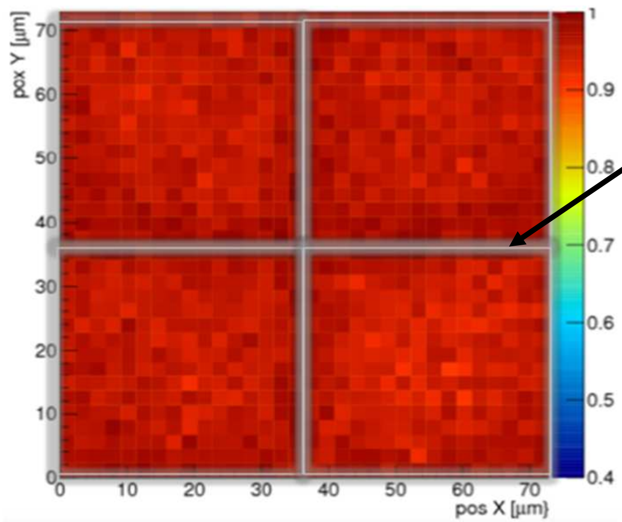
- 2 approaches have been followed:
  - **TJ-Malta1**:
    - Asynchronous readout: high hit rate, fast signal response, very low power
    - → Lead to TJ-Malta2 developments.

Talk I. Tortajada, Oct 7th

  - **TJ-Monopix1**:
    - Synchronous readout (a la FE-I3 IC): column drain architecture, ToT measurement

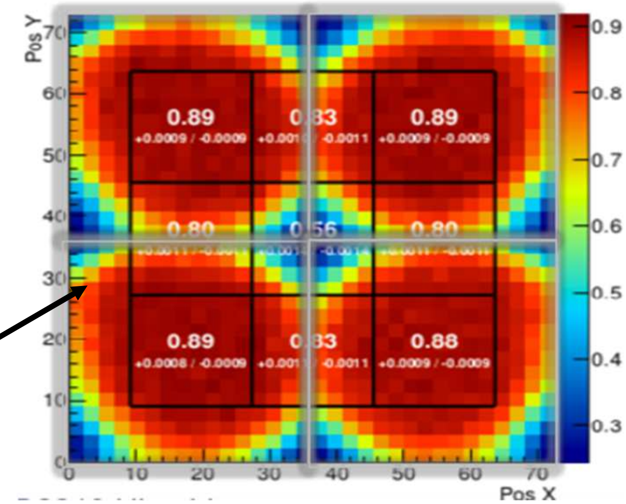
This talk

Loss of efficiency in corners



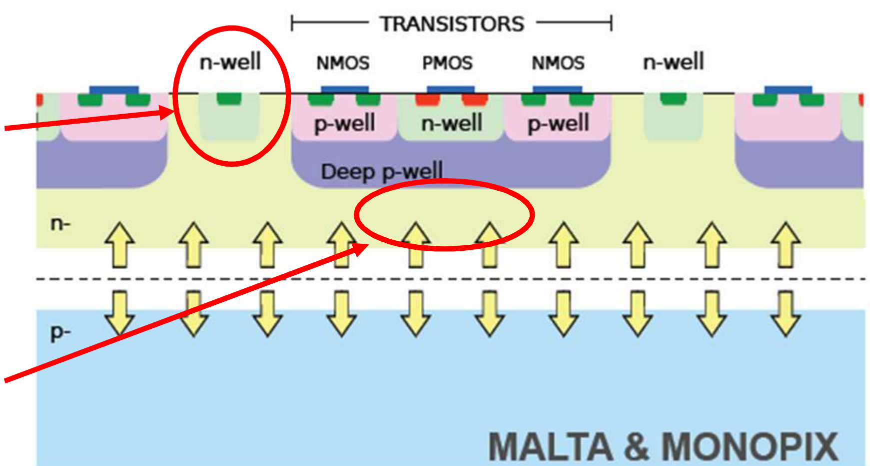
Malta: 2×2 pixels, 36 µm pitch, 250 e- threshold, **pre-irrad**

Malta: 2×2 pixels, 36 µm pitch, 350 e- threshold, **10^{15} n.cm^{-2}**



The field configuration under the DPWell far from the collection electrode is the issue:

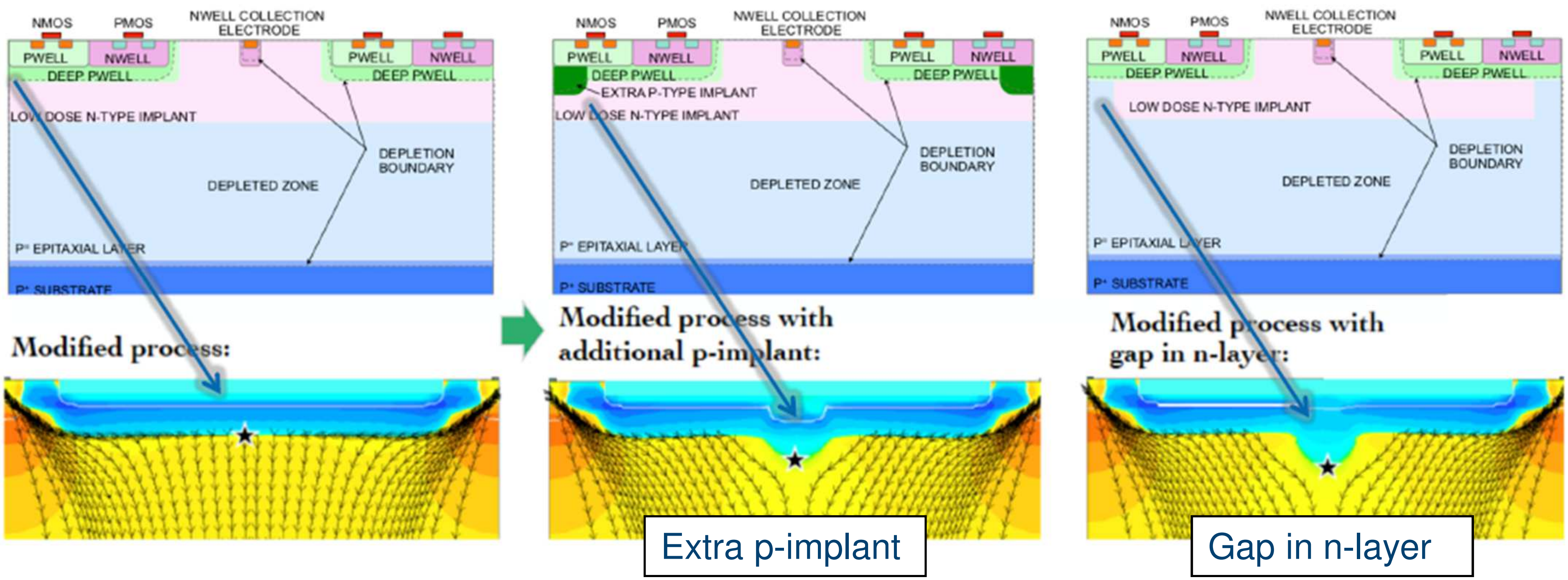
- Requires full depletion under DPW
- Need transversal field components in corners → proposition of extra process modification(s)
- Operation at low threshold essential



Process optimization for radiation hardness: MiniMALTA

- several possibilities found:
  - Deep p well extra implant.
  - Gap in n-type implant.

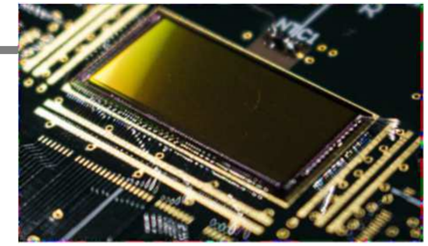
Change field configuration under DPW to "push" charges towards collection electrode



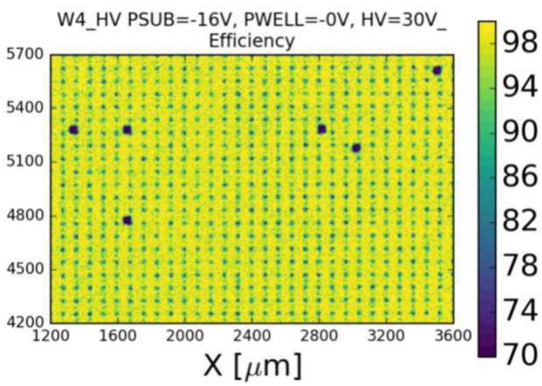
M. Munker PIXEL 2018 / 10.1088/1748-0221/14/05/C05013

Talk I. Tortajada, Oct 7th

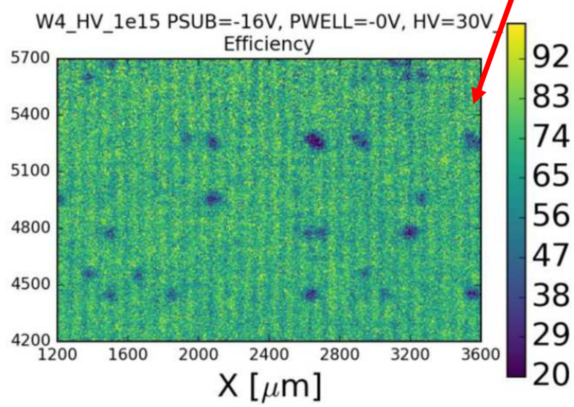
TJ-Monopix1 → TJ-Monopix2



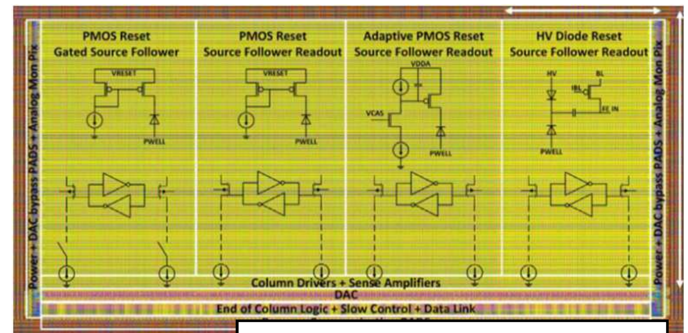
- TJ-Monopix1:
  - Fully functional, but efficiency drop after irradiation.



Efficiency unirradiated (17e- ENC / 350 e- threshold): 97%



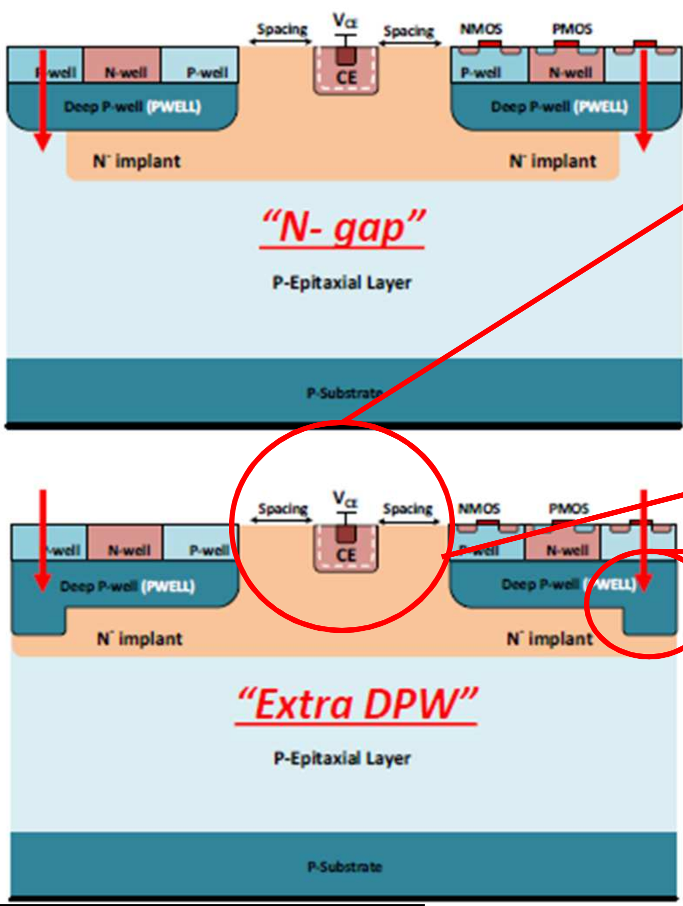
Efficiency 10^{15} n.cm^{-2}: 70% (23 e- ENC / 570 e- thresh.)

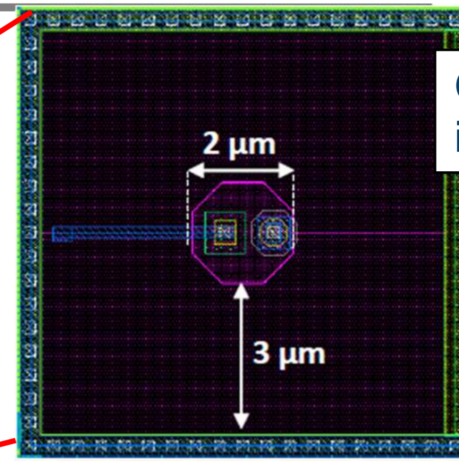


Monopix1: 112col×224row

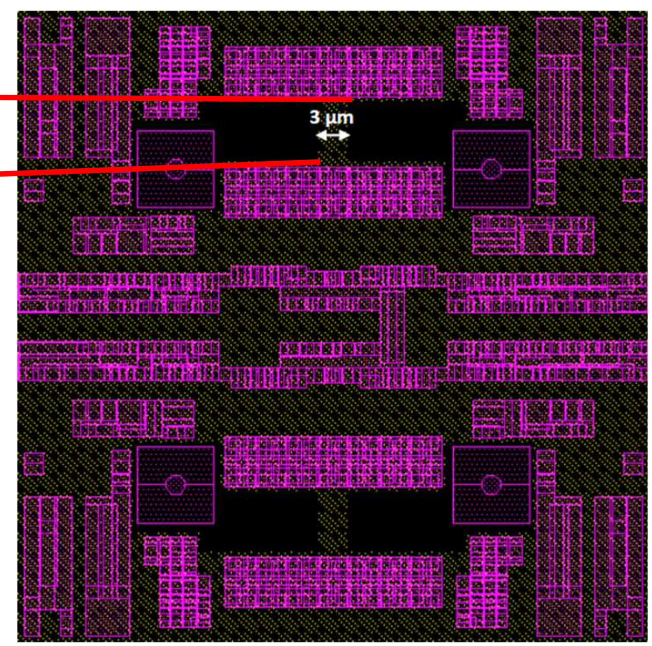
- TJ-Monopix2:
  - Full-scale small-collection diode with improved charge collection.
  - Decrease minimal threshold.
- Joint TJ-Malta + TJ-Monopix submission!
- Design on-going, final verification on-going (1st mock layout already sent to founder…).

TJ-Monopix2 sensor





Collection diode implementation



Implant modification

TJ-Monopix2 FE

- Low threshold operation crucial! → New FE design for higher gain and less noise.
- Threshold adjustment on pixel level.
- New implant designs, reset optimization

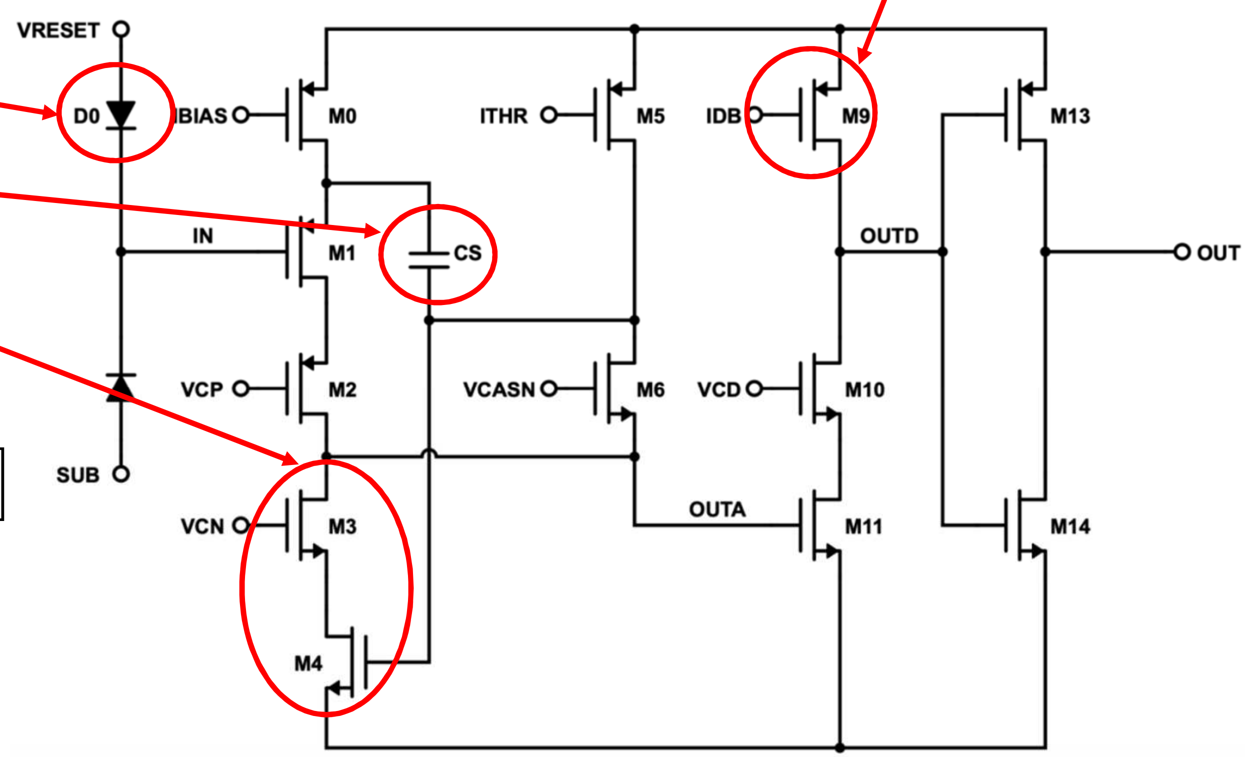
Diode reset → increased input signal, TID

↑C → gain↑, ↓ENC / ↓σ_{thr}

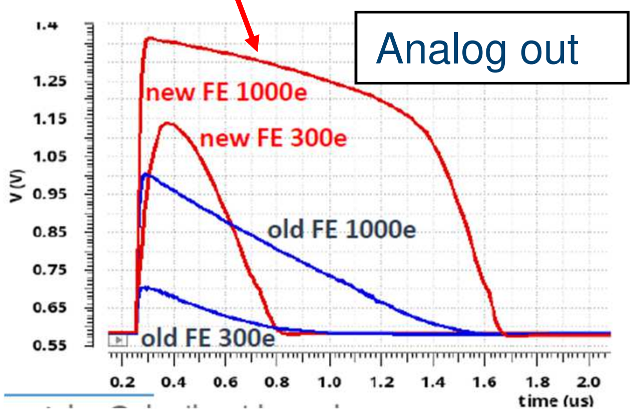
↑L → gain↑, ↓ RTS noise

3-5× gain increase!

3-bit threshold tuning



Analog out

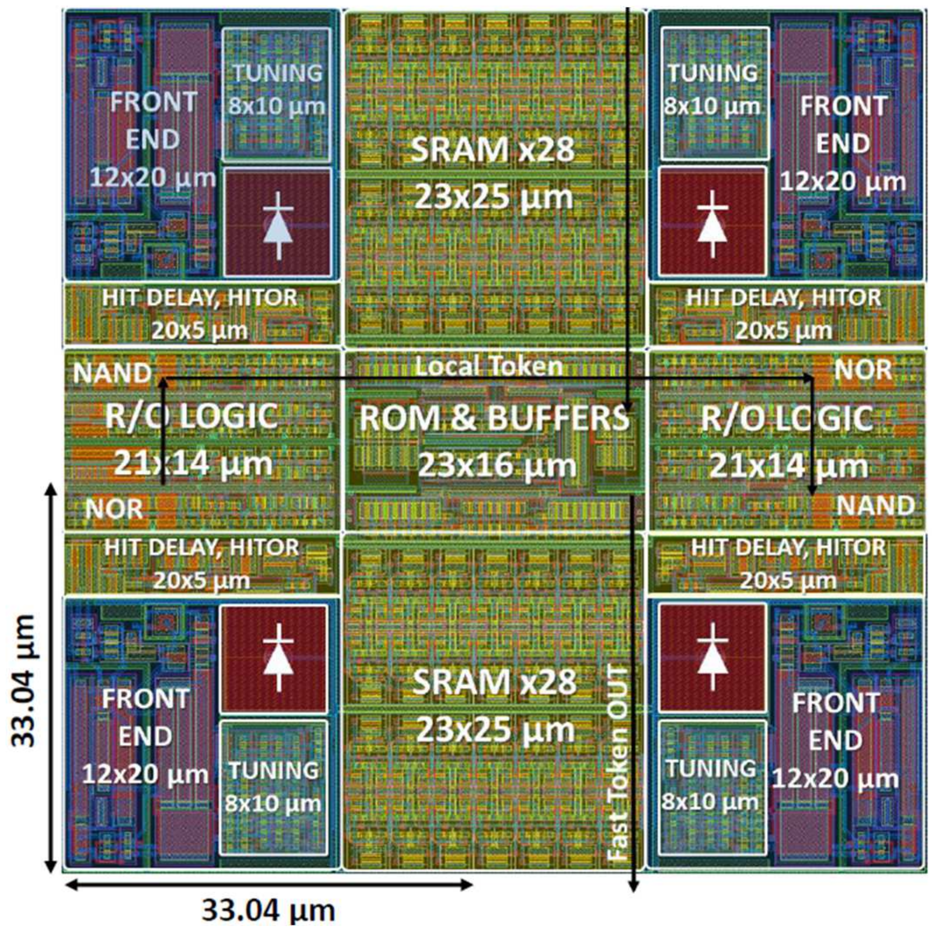


Kostas Moustakas

Power not compromised

TJ-Monopix2 pixel

The TJ-Monopix2 2×2 pixel



→ Built as 2×2 core (area ↓)

→ Readout Logic based on Column Drain architecture a la FE-I3

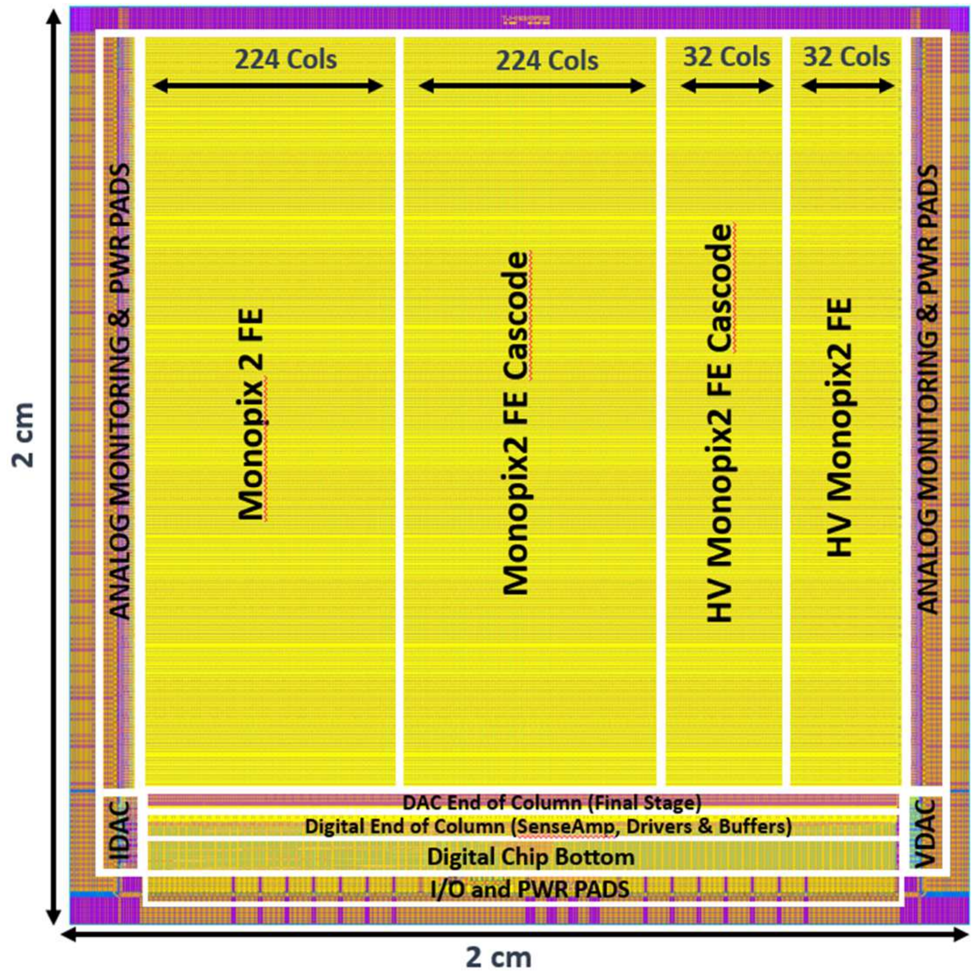
→ 7-bit BCID Time-Stamp

→ Fast token: Internal token ring & group token
  - → Propagation delay reduced from >100 ns to 35 ns
  - → Does not impact readout speed (< 50 ns)

→ Readout logic improvements to mitigate timing issues related to READ slope

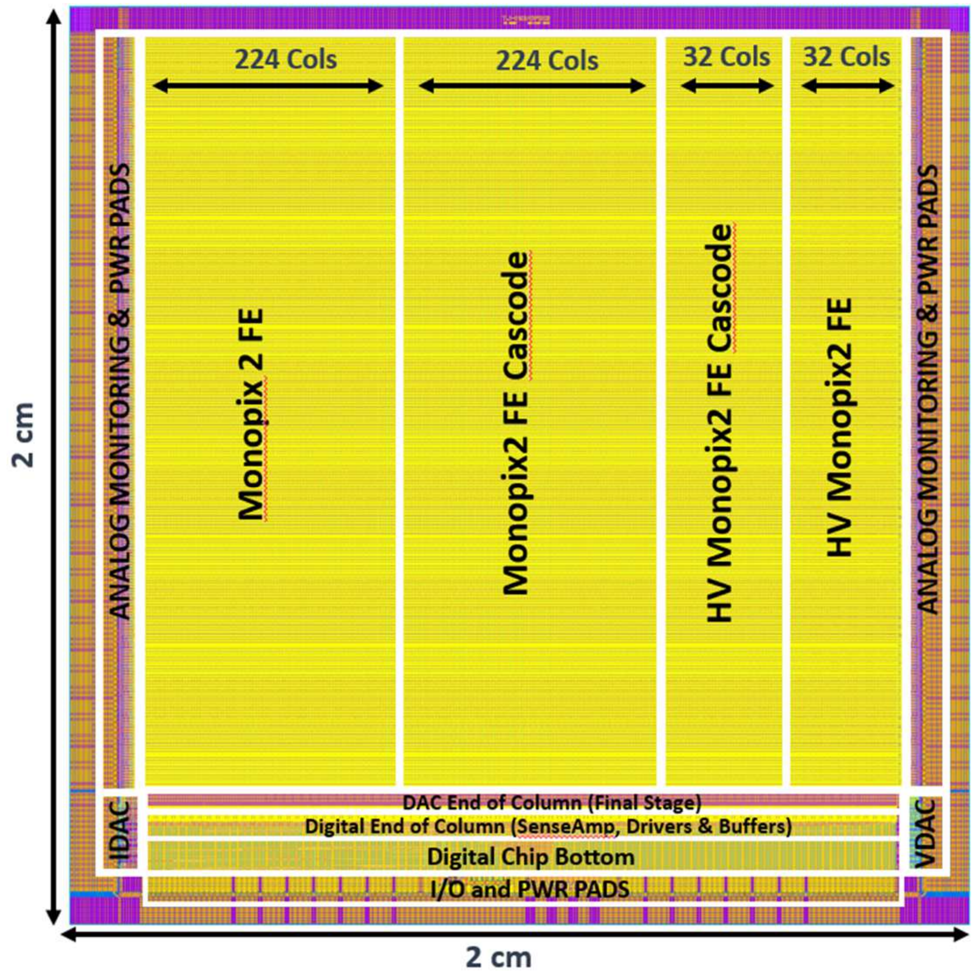
→ Hit delay through column for compensation of BCID propagation time

TJ-Monopix2 Chip Overview



- → 4 flavors: Normal, Cascode, HV, HV Cascode
- → Modular 8-bit DAC, 32 column grouping for voltage drop compensation
- → LVDS TX, RX designed for 5 Gbps
- → Power:
  - → 4 domains: Matrix Analog, Matrix Digital, DAC, Digital Periphery
  - → Matrix analog: ~90 $mW.cm^{-2}$
  - → BCID distribution: ~80 $mW.cm^{-2}$
  - → Periphery: ~ 60 mW

TJ-Monopix2 Chip Overview



	TJ-Monopix1	TJ-Monopix2
Chip Size	1x2 cm² (224x448 pix)	2x2 cm² (512x512 pix)
Pixel size	36 × 40 µm²	33.04 × 33.04 µm²
Noise	≅11 e⁻	< 10 e⁻ (improved FE)
LE/TE time stamp	6-bit	7-bit
Threshold Dispersion	≅ 30 e⁻ rms	< 15 e⁻ rms (improved FE + tuning)
Minimum threshold	≅ 300 e⁻	< 100 e⁻
In-time threshold	≅ 400e⁻	< 150 e⁻
Efficiency (epi)	≅ 70 % (irradiated)	> 95% (irradiated)

* Expectations

→ **Submission TJ-MALTA2 + TJ-MONOPIX2 mid-October!**

LF-Monopix development

1- Introduction

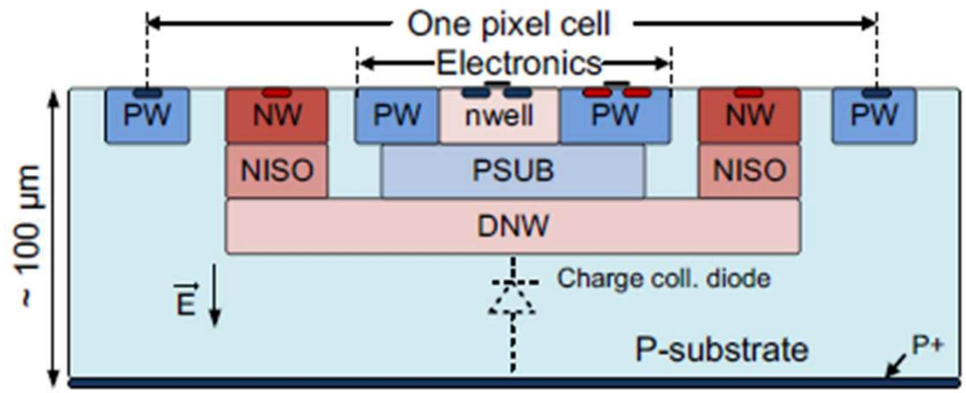
2- TJ 180 nm TJ-Monopix development

3- LF 150 nm LF-Monopix development

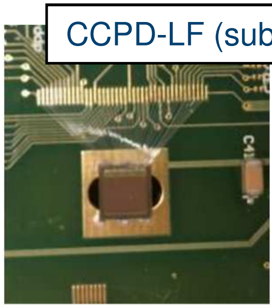
4- Conclusion

LF DMAPS development line

- A large collection diode design:
  - LF 150 nm process
  - Multiple nested wells
  - 6 metal layers + thick top
  - Substrate resistivity > 2kΩ.cm
  - Backside thinning and processing
- Several prototypes:

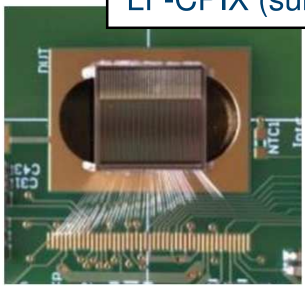


CCPD-LF (subm. 2014)



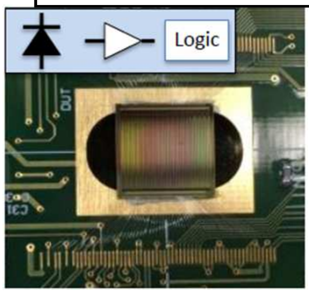
- Pixel size: 33×125 µm²
- Chip size: 5×5 mm²
- Fast Readout with FE-I4
- Thickness: 750/300/100 µm

LF-CPIX (subm. Feb.16)



- Pixel size: 50×250 µm²
- Chip size: 10×10 mm²
- Fast Readout with FE-I4
- Thickness: 750/300/100 µm

LF-Monopix1 (subm. Aug.16)

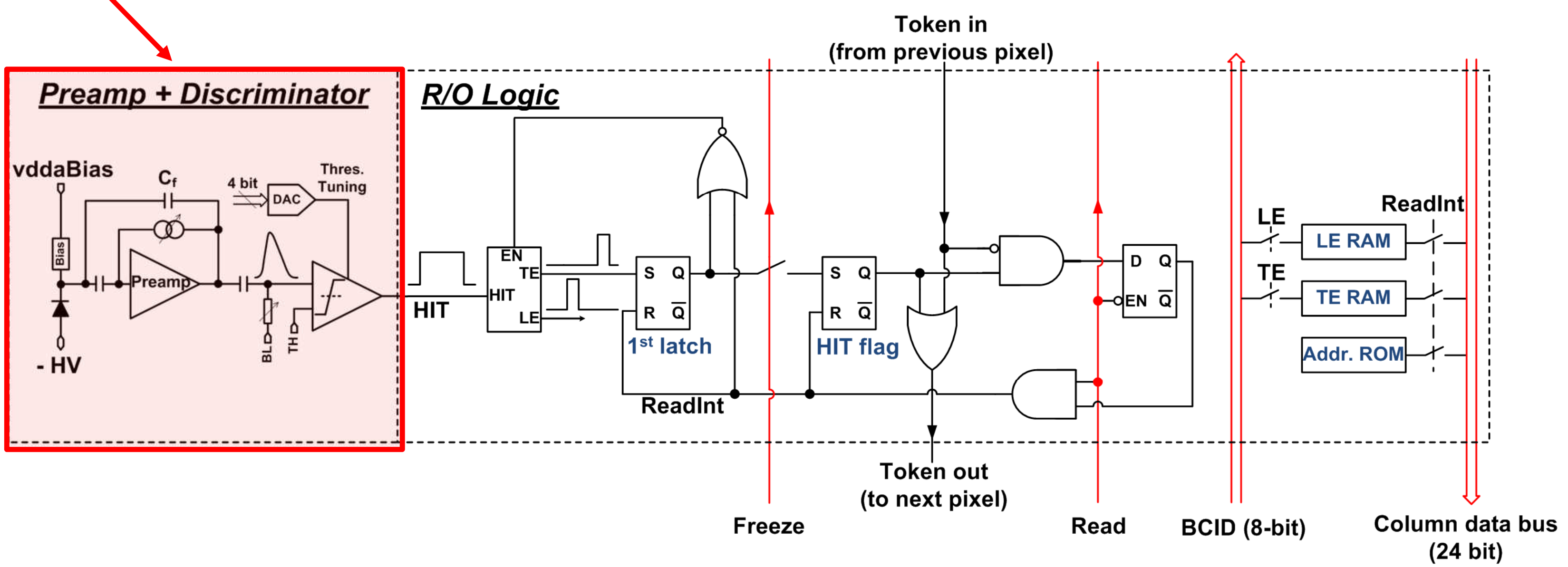


- Pixel size: 50×250 µm²
- Chip size: 10×10 mm²
- Monolithic: Includes Column Drain Readout.
- Thickness: 750/300/100 µm

M. Barbero et al. doi.org/10.1088/1748-0221/15/05/P05013

Focus on LF-Monopix1 analog FE

- The analog FE uses a Charge Sensitive Amplifier

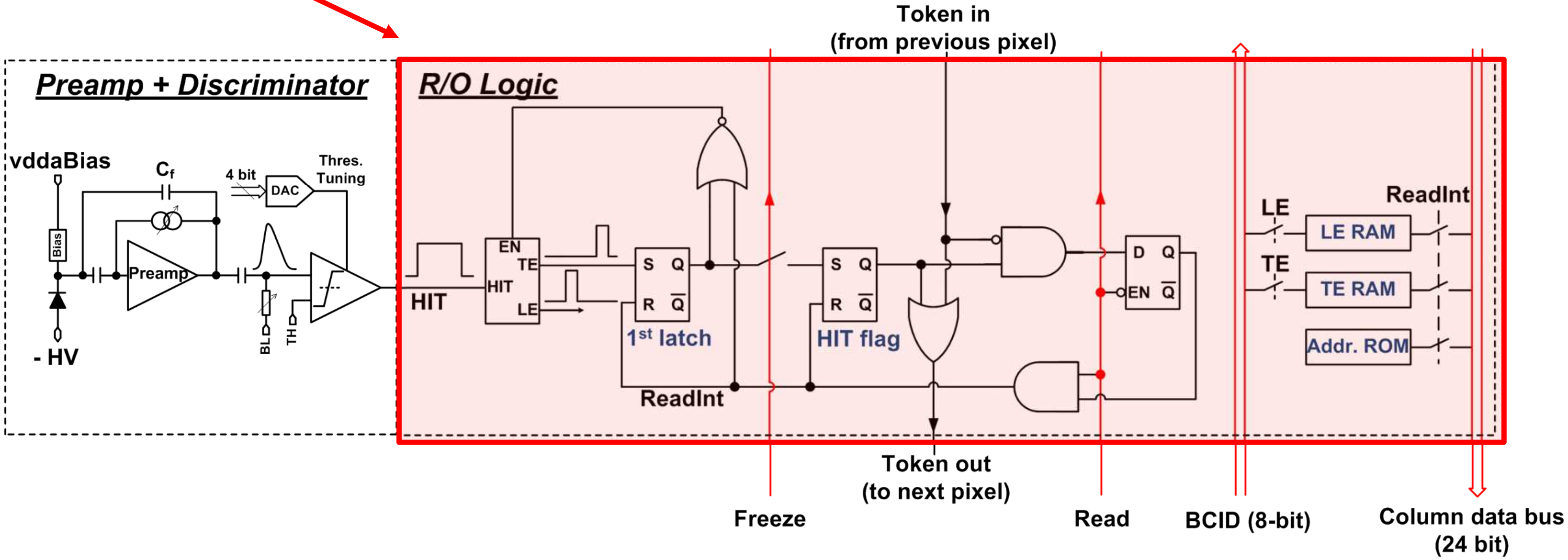


- Gain independent of large $C_{detector}$? (~400 fF here!)
  → Small C_f as $G \sim 1/C_f$ ($C_f \sim 5fF$)
- $\tau_{CSA}\ \alpha\ \frac{C_D}{g_m.C_f}$ and $ENC^2\ \alpha\ \frac{kT\ C_D^2}{g_m\ \tau}$
- Need a large g_m for these large C_D!
- Threshold trimming a must (4 bits in-pixel)

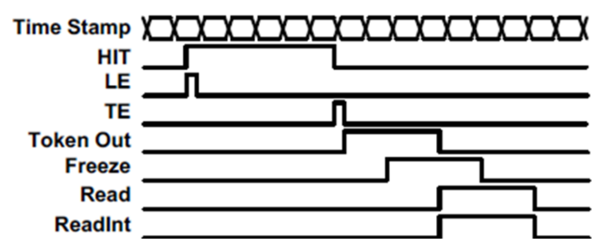
Power: ~40 µW/pix in LF-Monopix1

Focus on LF-Monopix1 digital FE

- The digital FE is based on Column Drain Architecture



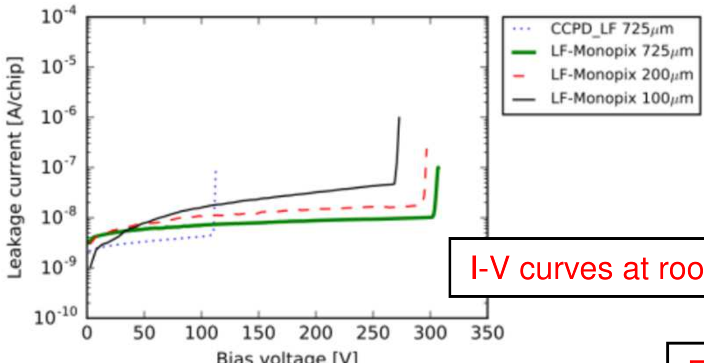
- It provides 8-bit ToA and ToT
- Full custom design:
  - to minimize area and $C_{digital}$
  - Low noise design for critical digital blocks (e.g. current steering logic)



T. Wang, et al., DOI: 10.1088/1748-0221/12/01/C01039
P. Rymaszewski et al., DOI: http://doi.org/10.22323/1.313.0045 v

LF-Monopix1 performances

- High breakdown voltage >250 V
  - Improved wrt previous designs

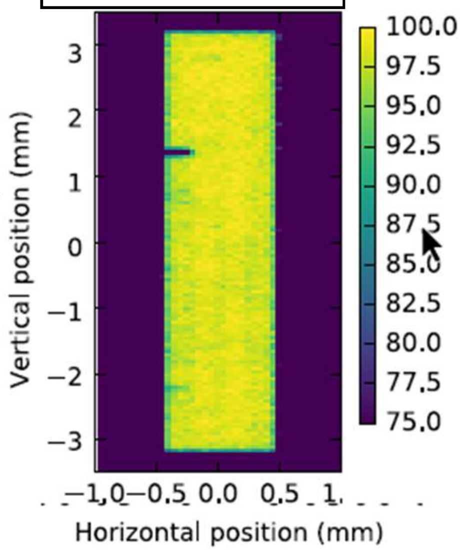


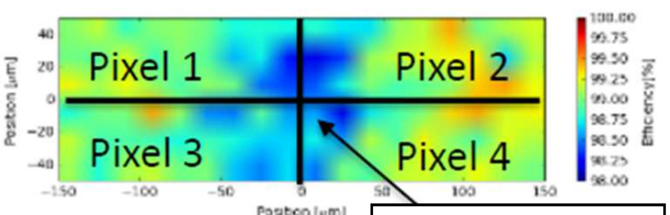
I-V curves at room T

J. Liu, et al, DOI: 10.1088/1748-0221/12/11/C11013
I. Caicedo et. al, DOI: 10.1088/1748-0221/14/06/C06006

- High & uniform efficiency after 10^{15} n.cm^{-2}
  - Bias -130V, dry ice cooled
  - Thres. ~1700 e-
  - 0.2% masked pixels

Efficiency @ 10^{15} n.cm^{-2} : 98.9%!

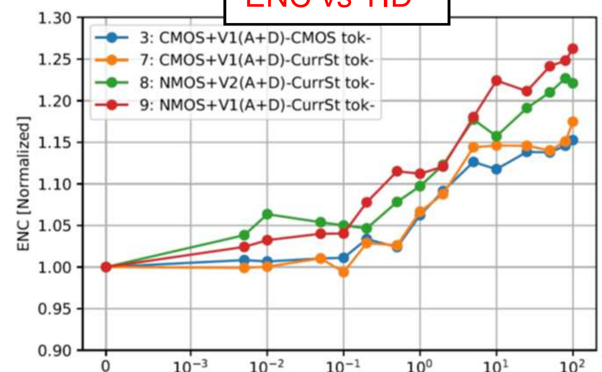




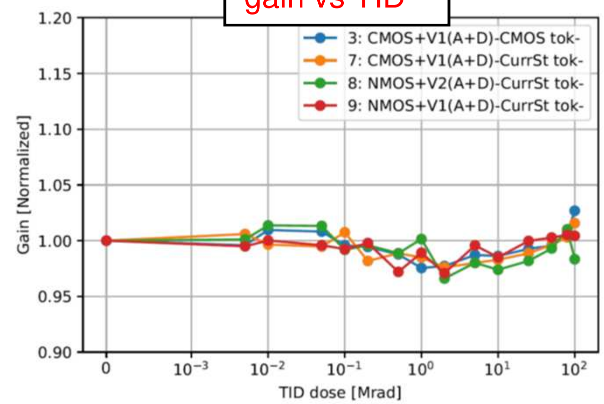
Pixel corner efficiency : 98%

- Moderate noise & gain degradation at 100 MRad:
  - 15-25% ENC ↑ / < 5% gain ↓

ENC vs TID



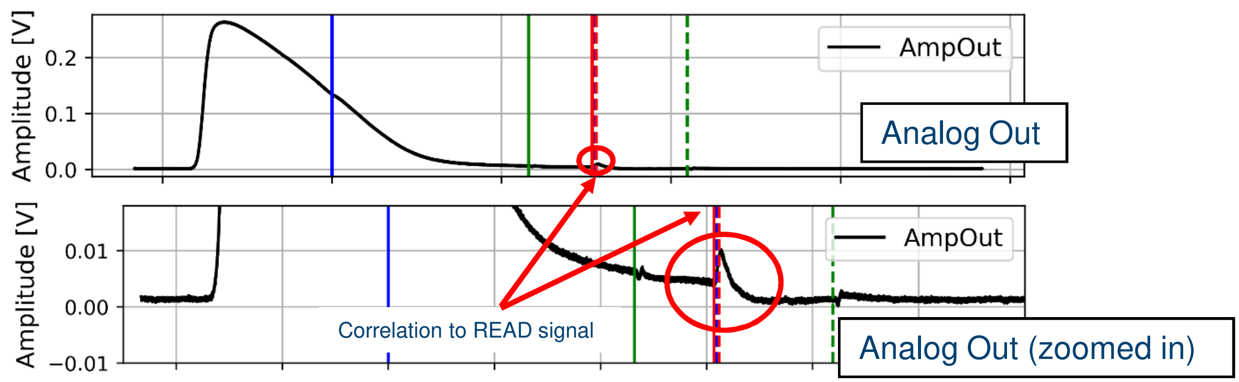
gain vs TID



T. Hirono, et. al, DOI: 10.1016/j.nima.2018.10.059

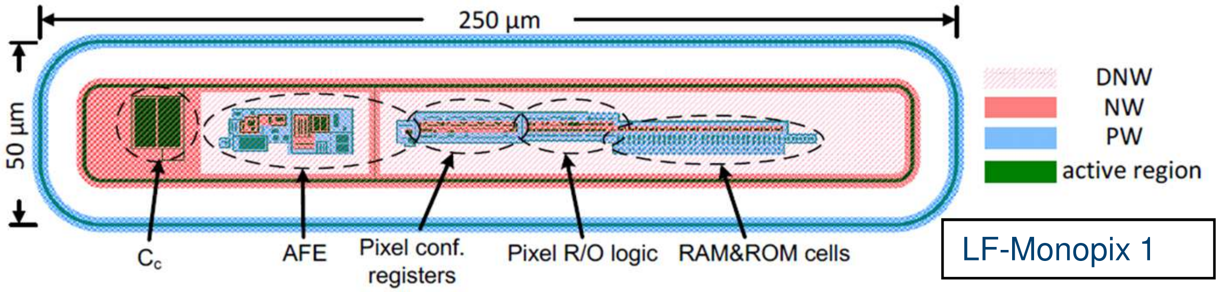
LF-Monopix1 → LF-Monopix2

- LF-Monopix1:
  - Fully functional, high efficiency after 10^{15} n.cm^{-2}.
  - … but: found (small) crosstalk correlated to digital read signal → can generate spurious signals
  - Issue understood (layout)

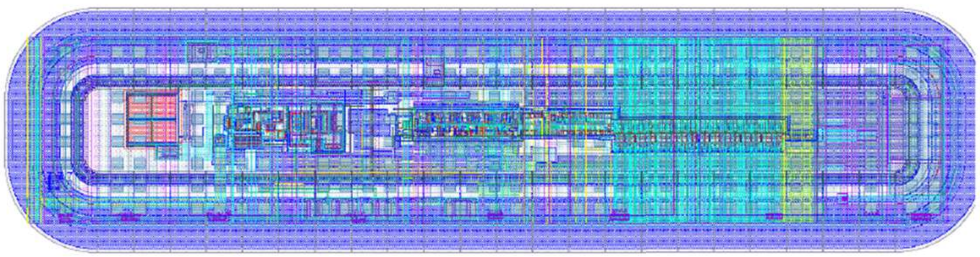


- LF-Monopix2:
  - Improved logic and layout (READ signal related → Xtalk reduction)
  - BCID propagation better and better Column reading.
  - Detector capacitance reduction (for better SNR)
  - Lowering of pixel power consumption (preamp and comparator)
  - Improved discriminator (faster, better match to 6-bit ToT)
  - → Submitted June 2020!

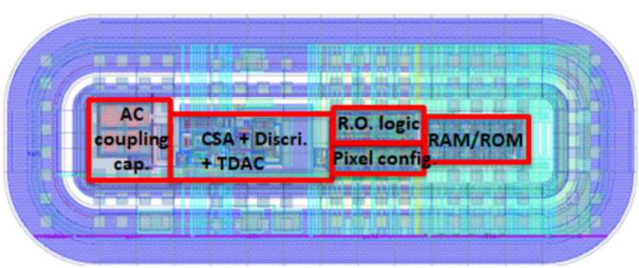
LF-Monopix2 sensor / pixel layout

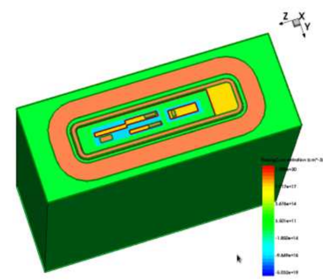


LF-Monopix 1



LF-Monopix 2



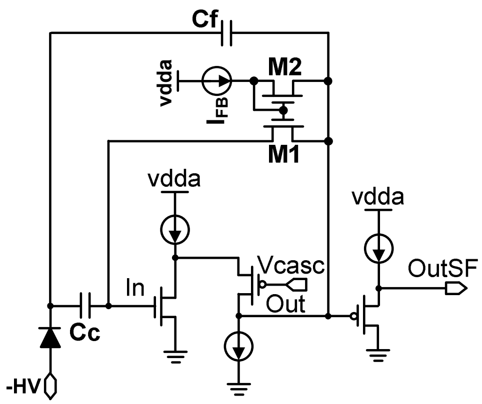


M. Zhao

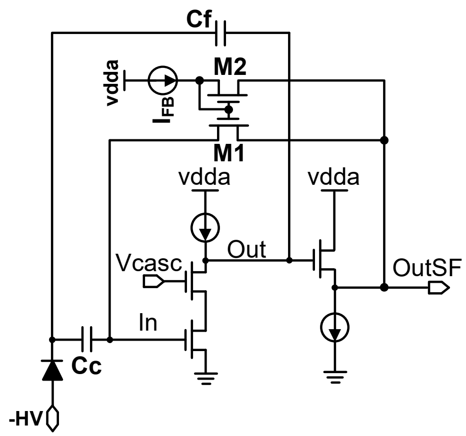
- LF-Monopix2:
  - Pixel size 50 µm × 150 µm
  - Rounded corner for reduced $\vec{E}$ (very HV needed for radiation hardness)
  - Capacitance ~250-300 fF (TCAD estimate)

LF-Monopix2: Analog FE

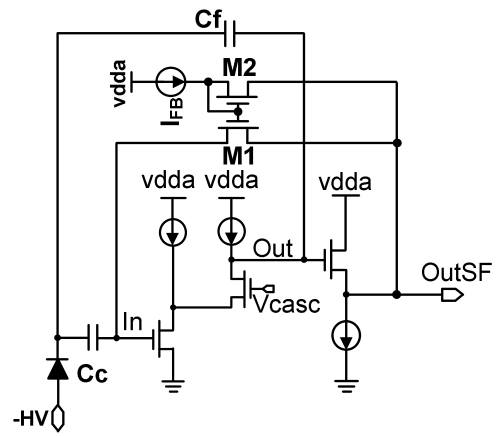
- Explores several CSA flavors:



CSA 1 (a la LF-Monopix1)
Folded cascode



CSA 2
Telescopic cascode
SF in DC feedback loop

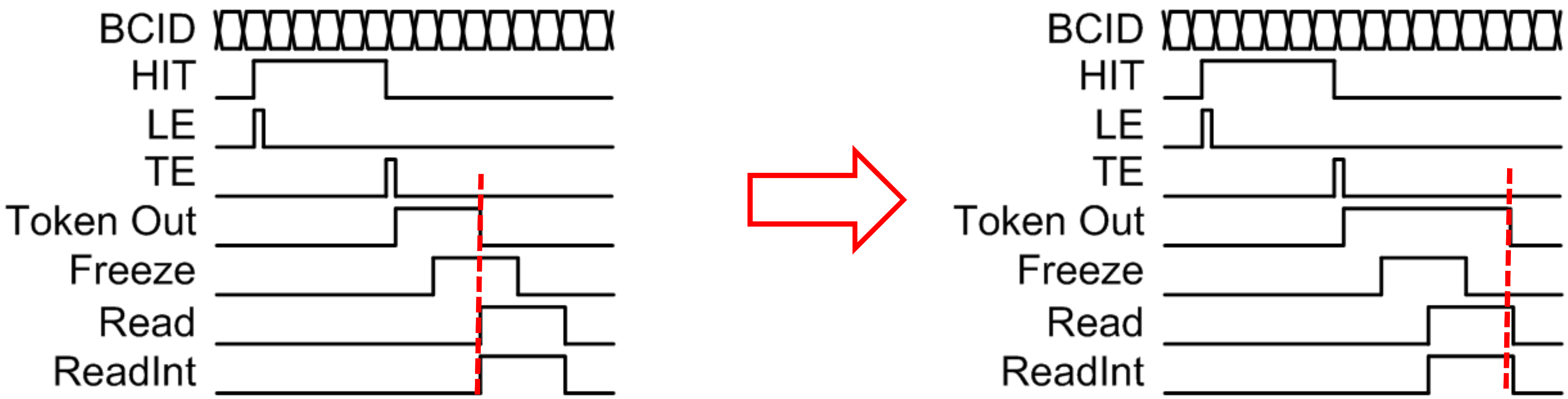


CSA 3
Open loop gain vs BW
SF in DC feedback loop

- Try also lower C_f for higher CSA gain, mitigates discriminator dispersion
- Explores 2 discriminators:
  - 1st: a la LF-Monopix1
  - 2nd: Bring improvements to discriminator design for better timing

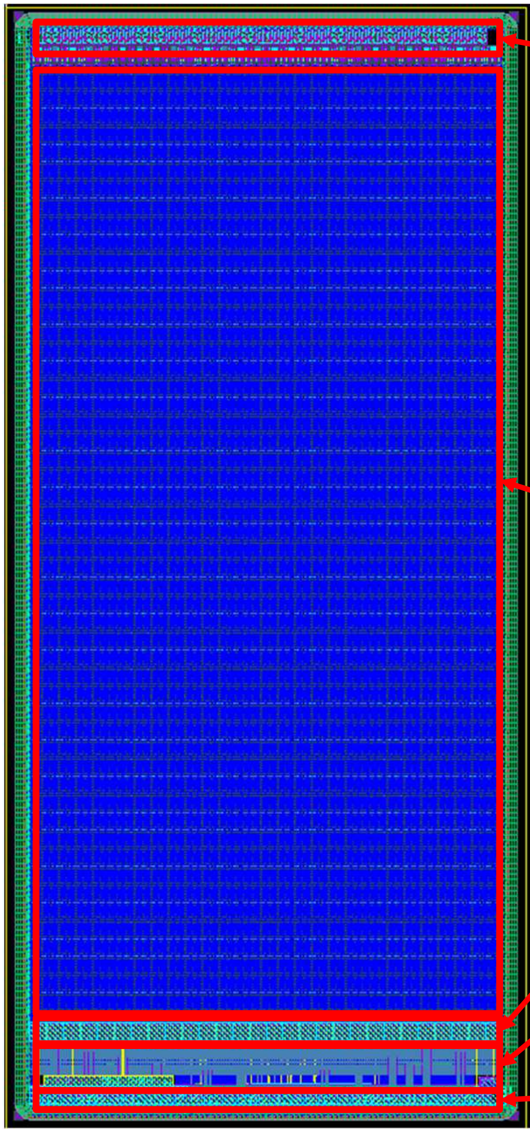
READ crosstalk fixing

- Was related to the fact the token was cleared by the READ rising edge, which led to switching during READ…
- Change logic to clearing on READ falling edge.



- Solution makes longer read cycle, but avoids unnecessary digital switching during read…

LF-Monopix2 Chip overview



Top pads:
Power / Sensor Bias / Some analog Voltage

Pixel array:
Pixel Size: 50×150 µm²
Pixel Matrix: 340×56 pixels
Variations in terms of CSA
Variations in terms of discriminator

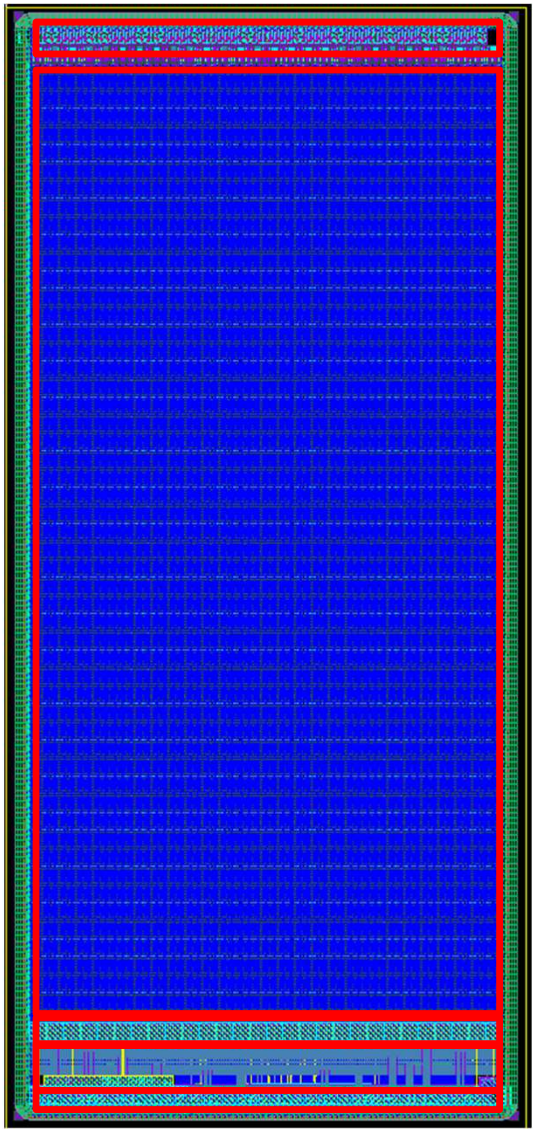
End of Column:
Sense amplifiers
Digital buffers

Periphery circuitry:
Digital logic
DAC + Analog buffer for monitoring

Bottom pads

Submitted June 2020
alongside test structures

LF-Monopix2 Chip overview



	LF-Monopix1	LF-Monopix2
Pixel size	50 × 250 µm2	**50 × 150 µm2**
Cd	~ 400 fF (estimated)	**250 – 300 fF (estimated)**
Analog Power/pixel (CSA + Discri.)	15 µA + 5 µA = 20 µA	**10 µA + 2 µA = 12 µA**
Noise	~200 e^-	**100 ~ 150 e^-**
LE/TE time stamp	8-bit	**6-bit**
ToT @ 6 ke-	---	**200 – 250 ns**
Max. ToT	---	**400 ns**
p-p (rms) thres. dispersion	(~ 100 e^-)	**800 e^- (80 e^-)**
Min. threshold	1500 e^-	**1000 e^-**
In-time threshold	~ 2000 e^-	**1500 e^-**

Submitted June 2020 alongside test structures

Conclusion

1- Introduction

2- TJ 180 nm TJ-Monopix development

3- LF 150 nm LF-Monopix development

4- Conclusion

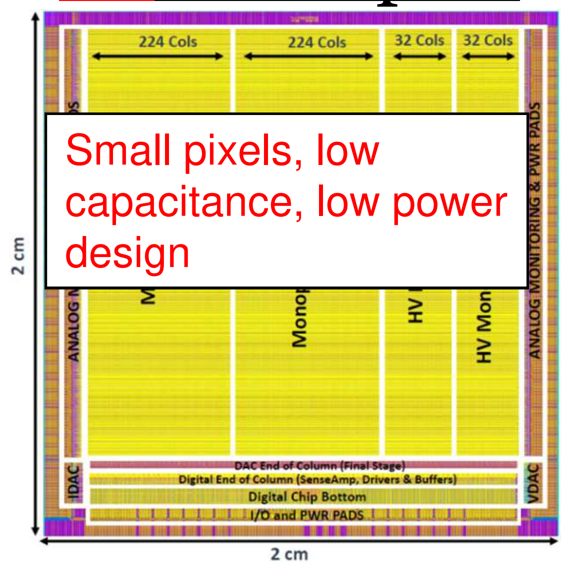
The Monopix2 development

- Out of ITk (challenging schedule) → interesting for post-ITk applications

Talk C. Gemme, Oct 6th

... e+e- environments or future hh ...

TJ-Monopix2:



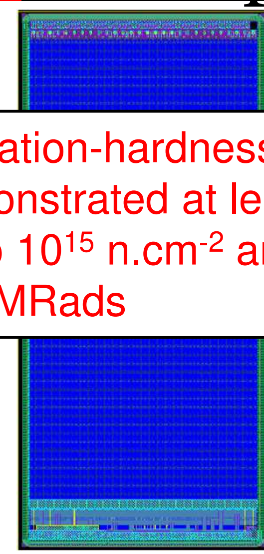
Small pixels, low capacitance, low power design

2×2 cm², 512×512 pixels, 33×33 µm²

New implants for better charge collection after irrad, lower threshold

Submission foreseen October 2020

LF-Monopix2:



Radiation-hardness demonstrated at least up to 10^{15} n.cm^{-2} and 100 MRads

2×1 cm², 340×56 pixels, 50×150 µm²

Analog and digital FE improvements

Smaller pixels, better layout

Submitted in June 2020

→ Back Dec. 2020

Thanks

- Many slides / original material / results borrowed from many colleagues:

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