Depleted Monolithic Active Pixel Sensors in LF 150nm and TJ 180 nm CMOS technologies: The Monopix developments

Vertex 2020 conference
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On behalf of
Introduction

1- Introduction
2- TJ 180 nm TJ-Monopix development
3- LF 150 nm LF-Monopix development
4- Conclusion
Monolithic depleted CMOS

• In some context, could provide advantageous alternative to hybrid pixels.

• Key ingredients:
  – Charges collected by drift.
    • to go above $\sim 10^{13} \text{n}_{eq}\cdot\text{cm}^{-2}$, collecting charge by diffusion is problematic $\rightarrow$ drift (hence standard MAPS $\rightarrow$ Depleted MAPS).
  – Consequence $\rightarrow$ Fast signal response & radiation hardness.
  – Technology requirements $\rightarrow$ High Voltage process (apply 50-200 V), High Resistive wafers (>100Ωcm) and multiple nested wells (for full CMOS & shield)

• Advantages:
  – Usage of commercial process: production capability, reliability, low cost...
  – Simple less expensive module (wrt hybrid): no hybridization and much easier production! Can be used for larger area applications
  – Small pixel size possible (in some process)
  – Less power, less material...

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MAPS and DMAPS

• STAR experiment
  ALPIDE for ALICE upgrade

• DMAPS Monopix development based on original specs for ATLAS ITk outer pixel layer: NIEL > $10^{15} \text{n}_{\text{eq}}\text{cm}^{-2}$, TID > 80 Mrad, Hit Rate > 100 MHz.cm$^{-2}$

• Higher radiation hardness & faster readout need:

  → Cope with NIEL / trapping:
    • Fast collection by drift
  → Have high time resolution:
    • Fast collection by drift
    • Fast analog FE
    • Time stamping on chip

  → Cope with high TID:
    • Process + design methodology

  → Cope with high hit rate:
    • Fast return to baseline in analog FE ($\sim 1$ µs, avoids pile-up)
    • High logic density
    • High output bandwidth
### Specifications vs. Environments

In terms of **radiation hardness and speed:**

<table>
<thead>
<tr>
<th></th>
<th>STAR</th>
<th>ALICE</th>
<th>e.g. future e+e-: ILC</th>
<th>ATLAS HL-LHC Outer layer</th>
<th>ATLAS HL-LHC Inner layer</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Fluence [neq.cm⁻²]</strong></td>
<td>10^{12}</td>
<td>2.10^{13}</td>
<td>10^{12}</td>
<td>2.10^{15}</td>
<td>2.10^{16}</td>
</tr>
<tr>
<td><strong>TID [MRad]</strong></td>
<td>0.2</td>
<td>&lt;3</td>
<td>0.4</td>
<td>100</td>
<td>1000</td>
</tr>
<tr>
<td><strong>Timing [ns]</strong></td>
<td>~200000</td>
<td>20000</td>
<td>O(1000)</td>
<td>25</td>
<td>25</td>
</tr>
<tr>
<td><strong>Hit rate [kHz.mm⁻²]</strong></td>
<td>4</td>
<td>10</td>
<td>250</td>
<td>1000</td>
<td>10000</td>
</tr>
</tbody>
</table>
DMAPS CMOS Community

- Collaboration of ~25 institutes (European project STREAM)

Many technologies tried, but focus last ~3 years has been on: AMS/TSI 180 nm, LF 150 nm, and TJ 180 nm
CMOS sensor development lines

**Monolithic** sensors with electronics all in one!

(a) **large electrode design** / (b) **small electrode design**

- **LFoundry 150 process (or AMS/TSI 180)**
  - **Pros:**
    - Full CMOS
    - Uniform field, short drift distance \(\rightarrow\) radiation hardness (TID & NIEL), \(2.10^{15} \text{n$_{eq}$cm}^{-2}\) proven
    - HV rev. bias > 300V possible
    - BS thinning and processing possible
  - **Cons:**
    - Deep nwell Q collection \(\rightarrow\) big Capacitance (>200 fF) \(\rightarrow\) noise, power & crosstalk

- **TowerJazz 180 process**
  - **Pros:**
    - Full CMOS
    - Small capacitance (<10 fF) \(\rightarrow\) low noise, less crosstalk & low power.
    - Thin detector possible.
  - **Cons:**
    - Limited depletion, long drift distance, low field region \(\rightarrow\) radiation hardness TBD

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I. Peric, DOI: 10.1016/j.nima.2007.07.115
T. Kishishita, et al., DOI: 10.1088/1748-0221/10/03/C03047
P. Rymaszewski, et al., DOI: 10.1088/1748-0221/11/02/C02045
T. Hirono, et al., DOI: 10.1109/NSSMIC.2016.8069902
R. Turchetta, et al., DOI: 10.1016/S0168-9002(00)00893-7
W. Dulinski, et al., DOI: 10.1109/TNS.2004.832947
M. Havránek, et al., DOI: 10.1088/1748-0221/10/02/P02013
TJ-Monopix development

1- Introduction
2- TJ 180 nm TJ-Monopix development
3- LF 150 nm LF-Monopix development
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TJ 180nm: process modification

- A small electrode design:
  - Small pixel size (< 50 µm²)
  - Low capacitance (<3 fF)
  - Low power
  - Reduced digital-analog Xtalk

... but suffers from limited radiation-hardness ⇒ Requires process modification!

- Standard TJ 180 nm Process:
  - High resistivity p-type epi layer (> 1kΩ.cm)
  - Depleted region stays limited (in particular after irradiation)
  - ALPIDE-like

- Modified TJ 180 nm Process:
  - Additional n- implant ⇒ full depletion possible
  - Keeps small capacitance & no big changes to electronic layout
  - MALTA / MONOPIX

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TJ: The Digital Architectures

• 2 approaches have been followed:
  – **TJ-Malta1:**
    • Asynchronous readout: high hit rate, fast signal response, very low power
    • \( \rightarrow \) Lead to TJ-Malta2 developments.
  – **TJ-Monopix1:**
    • Synchronous readout (a la FE-I3 IC): column drain architecture, ToT measurement
Loss of efficiency in corners

The field configuration under the DPWell far from the collection electrode is the issue:

- Requires full depletion under DPW
- Need transversal field components in corners → proposition of extra process modification(s)
- Operation at low threshold essential
Process optimization for radiation hardness: MiniMALTA

- several possibilities found:
  - Deep p well extra implant.
  - Gap in n-type implant.

Change field configuration under DPW to “push” charges towards collection electrode
TJ-Monopix1 ➔ TJ-Monopix2

- **TJ-Monopix1:**
  - Fully functional, but efficiency drop after irradiation.

- **TJ-Monopix2:**
  - Full-scale small-collection diode with improved charge collection.
  - Decrease minimal threshold.

- Joint **TJ-Malta + TJ-Monopix submission**!
- Design on-going, final verification on-going (1st mock layout already sent to founder...).
TJ-Monopix2 sensor

“N-gap”
P-Epitaxial Layer

“Extra DPW”
P-Epitaxial Layer

Collection diode implementation

Implant modification

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TJ-Monopix2 FE

- Low threshold operation crucial! → New FE design for higher gain and less noise.
- Threshold adjustment on pixel level.
- New implant designs, reset optimization

Diode reset → increased input signal, TID

$\uparrow C \rightarrow \text{gain}\uparrow, \downarrow \text{ENC} / \downarrow \sigma_{\text{thr}}$

$\uparrow L \rightarrow \text{gain}\uparrow, \downarrow \text{RTS noise}$

3-5× gain increase!

Analog out

Power not compromised

3-bit threshold tuning

Kostas Moustakas

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TJ-Monopix2 pixel

- Built as 2×2 core (area ↓)
- Readout Logic based on Column Drain architecture a la FE-I3
- 7-bit BCID Time-Stamp
- Fast token: Internal token ring & group token
  - Propagation delay reduced from >100 ns to 35 ns
  - Does not impact readout speed (< 50 ns)
- Readout logic improvements to mitigate timing issues related to READ slope
- Hit delay through column for compensation of BCID propagation time
TJ-Monopix2 Chip Overview

- 4 flavors: Normal, Cascode, HV, HV Cascode
- Modular 8-bit DAC, 32 column grouping for voltage drop compensation
- LVDS TX, RX designed for 5 Gbps

Power:
- 4 domains: Matrix Analog, Matrix Digital, DAC, Digital Periphery
  - Matrix analog: ~90 mW.cm$^{-2}$
  - BCID distribution: ~80 mW.cm$^{-2}$
  - Periphery: ~60 mW
TJ-Monopix2 Chip Overview

→ Submission TJ-MALTA2 + TJ-MONOPIX2 mid-October!
LF-Monopix development

1- Introduction
2- TJ 180 nm TJ-Monopix development
3- LF 150 nm LF-Monopix development
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LF DMAPS development line

- A large collection diode design:
  - LF 150 nm process
  - Multiple nested wells
  - 6 metal layers + thick top
  - Substrate resistivity > 2kΩ.cm
  - Backside thinning and processing

- Several prototypes:

  - Pixel size: 33×125 µm²
  - Chip size: 5×5 mm²
  - Fast Readout with FE-I4
  - Thickness: 750/300/100 µm

  - Pixel size: 50×250 µm²
  - Chip size: 10×10 mm²
  - Fast Readout with FE-I4
  - Thickness: 750/300/100 µm

  - Pixel size: 50×250 µm²
  - Chip size: 10×10 mm²
  - Monolithic: Includes Column Drain Readout.
  - Thickness: 750/300/100 µm

M. Barbero et al. doi.org/10.1088/1748-0221/15/05/P05013
Focus on LF-Monopix1 analog FE

- The analog FE uses a Charge Sensitive Amplifier

  - Gain independent of large $C_{\text{detector}}$? ($\sim 400$ fF here!)
    $\Rightarrow$ Small $C_f$ as $G \sim 1/C_f$ ($C_f \sim 5$ fF)
  
  - $\tau_{\text{CSA}} \alpha \frac{C_D}{g_mC_f}$ and $ENC^2 \alpha \frac{kT C_D^2}{g_m \tau}$

  - Need a large $g_m$ for these large $C_D$!
  
  - Threshold trimming a must (4 bits in-pixel)

Power: $\sim 40 \mu W/\text{pix}$ in LF-Monopix1
Focus on LF-Monopix1 digital FE

- The digital FE is based on Column Drain Architecture

- It provides 8-bit ToA and ToT
- Full custom design:
  - to minimize area and $C_{\text{digital}}$
  - Low noise design for critical digital blocks (e.g. current steering logic)

T. Wang, et al., DOI: 10.1088/1748-0221/12/01/C01039
P. Rymaszewski et al., DOI: http://doi.org/10.22323/1.313.0045 v
LF-Monopix1 performances

- High breakdown voltage >250 V
  - Improved wrt previous designs

  ![I-V curves at room T](image)

  \[\text{J. Liu, et al, DOI: 10.1088/1748-0221/12/11/C11013}\]

  \[\text{I. Caicedo et. al, DOI: 10.1088/1748-0221/14/06/C06006}\]

- Moderate noise & gain degradation at 100 MRad:
  - 15-25% ENC ↑ / < 5% gain ↓

  ![ENC vs TID](image)
  ![Gain vs TID](image)

- High & uniform efficiency after 10^{15} n.cm^{-2}
  - Bias -130V, dry ice cooled
  - Thres. ~1700 e-
  - 0.2% masked pixels

  ![Vertical position](image)

  Erficiencia @ 10^{15} n.cm^{-2}: 98.9%!

  \[\text{T. Hirono, et. al, DOI: 10.1016/j.nima.2018.10.059}\]
LF-Monopix1 $\rightarrow$ LF-Monopix2

- **LF-Monopix1:**
  - Fully functional, high efficiency after $10^{15}$ n.cm$^{-2}$.
  - ... but: found (small) crosstalk correlated to digital read signal $\rightarrow$ can generate spurious signals
  - Issue understood (layout)

- **LF-Monopix2:**
  - Improved logic and layout (READ signal related $\rightarrow$ Xtalk reduction)
  - BCID propagation better and better Column reading.
  - Detector capacitance reduction (for better SNR)
  - Lowering of pixel power consumption (preamp and comparator)
  - Improved discriminator (faster, better match to 6-bit ToT)
  $\rightarrow$ Submitted June 2020!
**LF-Monopix2 sensor / pixel layout**

- **LF-Monopix2:**
  - Pixel size $50 \, \mu m \times 150 \, \mu m$
  - **Rounded corner** for reduced $\overline{E}$ (very HV needed for radiation hardness)
  - Capacitance $\sim 250-300 \, fF$ (TCAD estimate)
LF-Monopix2: Analog FE

- Explores several CSA flavors:
  - CSA 1 (a la LF-Monopix1)
    - Folded cascode
  - CSA 2
    - Telescopic cascode
    - SF in DC feedback loop
  - CSA 3
    - Open loop gain vs BW
    - SF in DC feedback loop

- Try also lower \( C_f \) for higher CSA gain, mitigates discriminator dispersion
- Explores 2 discriminators:
  - 1\(^{st}\): a la LF-Monopix1
  - 2\(^{nd}\): Bring improvements to discriminator design for better timing
READ crosstalk fixing

• Was related to the fact the token was cleared by the READ rising edge, which led to switching during READ...

• Change logic to clearing on READ falling edge.

• Solution makes longer read cycle, but avoids unnecessary digital switching during read...
LF-Monopix2 Chip overview

Top pads:
Power / Sensor Bias / Some analog Voltage

Pixel array:
Pixel Size: 50×150 µm²
Pixel Matrix: 340×56 pixels
Variations in terms of CSA
Variations in terms of discriminator

End of Column:
Sense amplifiers
Digital buffers

Periphery circuitry:
Digital logic
DAC + Analog buffer for monitoring

Bottom pads

Submitted June 2020 alongside test structures
### LF-Monopix2 Chip overview

<table>
<thead>
<tr>
<th></th>
<th>LF-Monopix1</th>
<th>LF-Monopix2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel size</td>
<td>$50 \times 250 , \mu m^2$</td>
<td>$50 \times 150 , \mu m^2$</td>
</tr>
<tr>
<td>$C_d$</td>
<td>$\sim 400 , fF$ (estimated)</td>
<td>$250 - 300 , fF$ (estimated)</td>
</tr>
<tr>
<td>Analog Power/pixel</td>
<td>$15 , \mu A + 5 , \mu A = 20 , \mu A$</td>
<td>$10 , \mu A + 2 , \mu A = 12 , \mu A$</td>
</tr>
<tr>
<td>(CSA + Discri.)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Noise</td>
<td>$\sim 200 , e^{-}$</td>
<td>$100 - 150 , e^{-}$</td>
</tr>
<tr>
<td>LE/TE time stamp</td>
<td>8-bit</td>
<td>6-bit</td>
</tr>
<tr>
<td>ToT @ 6 ke-</td>
<td>---</td>
<td>200 - 250 ns</td>
</tr>
<tr>
<td>Max. ToT</td>
<td>---</td>
<td>400 ns</td>
</tr>
<tr>
<td>$p-p$ (rms) thres.</td>
<td>$(\sim 100 , e^{-})$</td>
<td>$800 , e^{-} (80 , e^{-})$</td>
</tr>
<tr>
<td>dispersion</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Min. threshold</td>
<td>1500 $e^{-}$</td>
<td>1000 $e^{-}$</td>
</tr>
<tr>
<td>In-time threshold</td>
<td>$\sim 2000 , e^{-}$</td>
<td>1500 $e^{-}$</td>
</tr>
</tbody>
</table>

Submitted June 2020 alongside test structures
Conclusion

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The Monopix2 development

- Out of ITk (challenging schedule) → interesting for post-ITk applications
  ... e+e- environments or future hh ...

TJ-Monopix2:

Small pixels, low capacitance, low power design

2×2 cm², 512×512 pixels, 33×33 µm²

New implants for better charge collection after irrad, lower threshold

Submission foreseen October 2020

LF-Monopix2:

Radiation-hardness demonstrated at least up to $10^{15}$ n.cm⁻² and 100 MRads

2×1 cm², 340×56 pixels, 50×150 µm²

Analog and digital FE improvements

Smaller pixels, better layout

Submission in June 2020 → Back Dec. 2020
Thanks

- Many slides / original material / results borrowed from many colleagues:

  Tomasz Hemperek, Magdalena Munker, Kostas Moustakas, Patrick Pangaud, Heinz Pernegger, Walter Snoeys, Tianyang Wang, Norbert Wermes... and more...


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