

First test results from the ITkPixV1 pixel readout chip

Vertex 2020 - 06.10.20

Timon Heim - LBNL
on behalf of RD53 Collaboration
and ITkPixV1 Testing Team

	RD53	Current Pixel
Chip Size	2x2 cm ²	2x2cm ²
Pixel Size	50x50 μm ²	50x250 μm ²
Pixel Hit Rate	3 GHz/cm ²	400 MHz/cm ²
Trigger rate	4/1 MHz	100 kHz
Trigger Latency	12.8 μs/51.2 μs	6.4 μs
Current consumption	<8 μA/pixel	20 μA/pixel
Radiation Tolerance	0.5 Grad	300 Mrad
Min. stable Threshold	600 e	1500 e



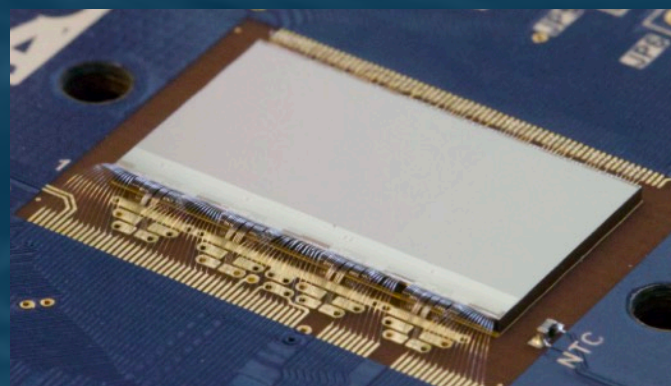
RD53: 22 collaborating institutes,
around 20 active designers

Requirements doc: <https://cds.cern.ch/record/2663161>

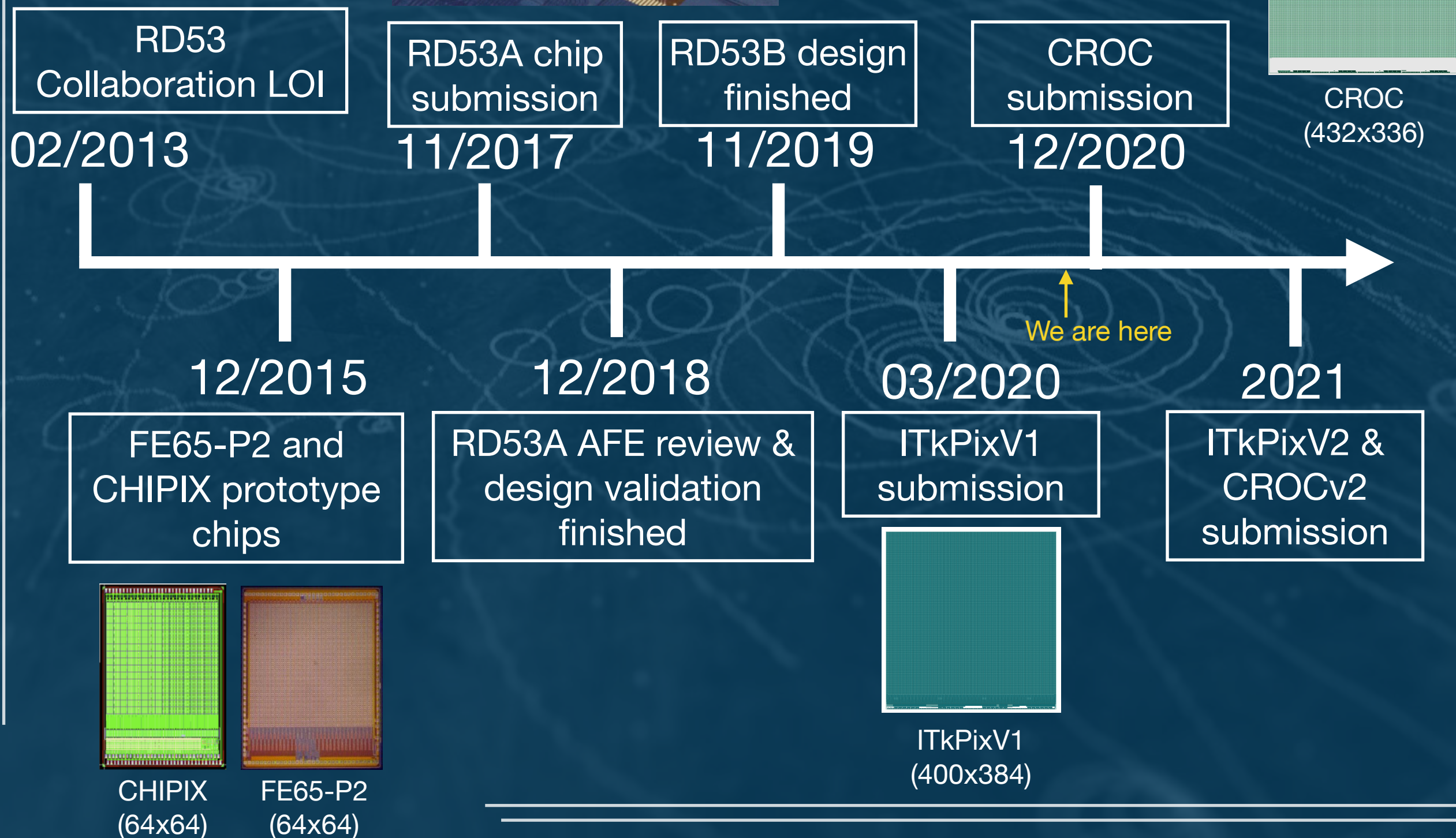
RD53 Collaboration in charge of:

- Characterization of 65nm technology in radiation environment
- Design of readout chip for the use in the ATLAS/CMS HL-LHC Pixel detectors
 - Analog front-end
 - Analog IPs (Bias DACs, monitoring ADC, CDR/PLL, high-speed serialiser, SLDO, References, ...)
 - Digital logic (hit buffering, data compression, ...)
- Initial end-goal was half-size demonstrator chip RD53A
- Was extended to design pre-production and production version of readout chips

RD53A (400x192)



Timeline

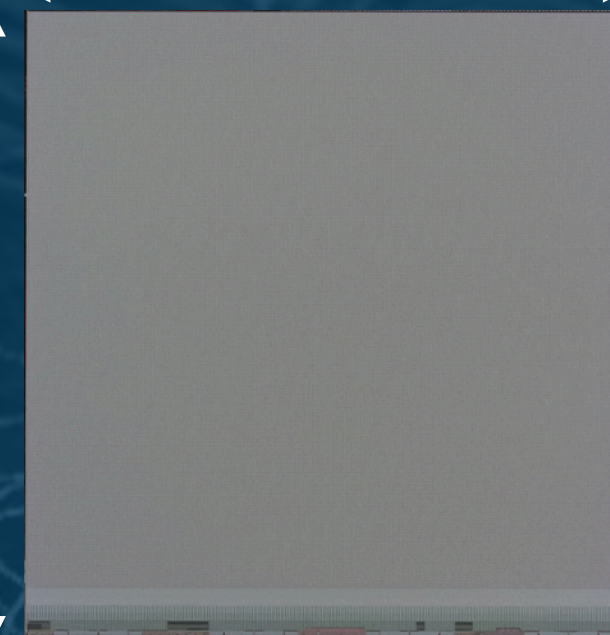


RD53B:

- Virtual chip/Design Library
- Touched or improved nearly every piece of RD53A
- Will be assembled in two versions:
 - ATLAS ITkPixV1 (400x384 pixels)
 - Differential analog FE
 - CMS CROC (432x336 pixels)
 - Linear analog FE
- Digital RTL shared between both chips
- Same End-Of-Chip (analog and digital) for both chips
 - Same pad ring

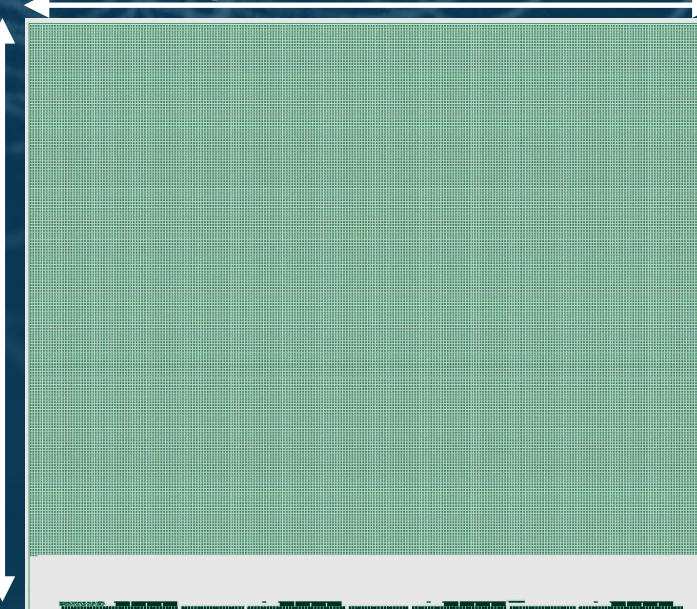
400 pixels / 20 mm

384 pixels / 20.7 mm



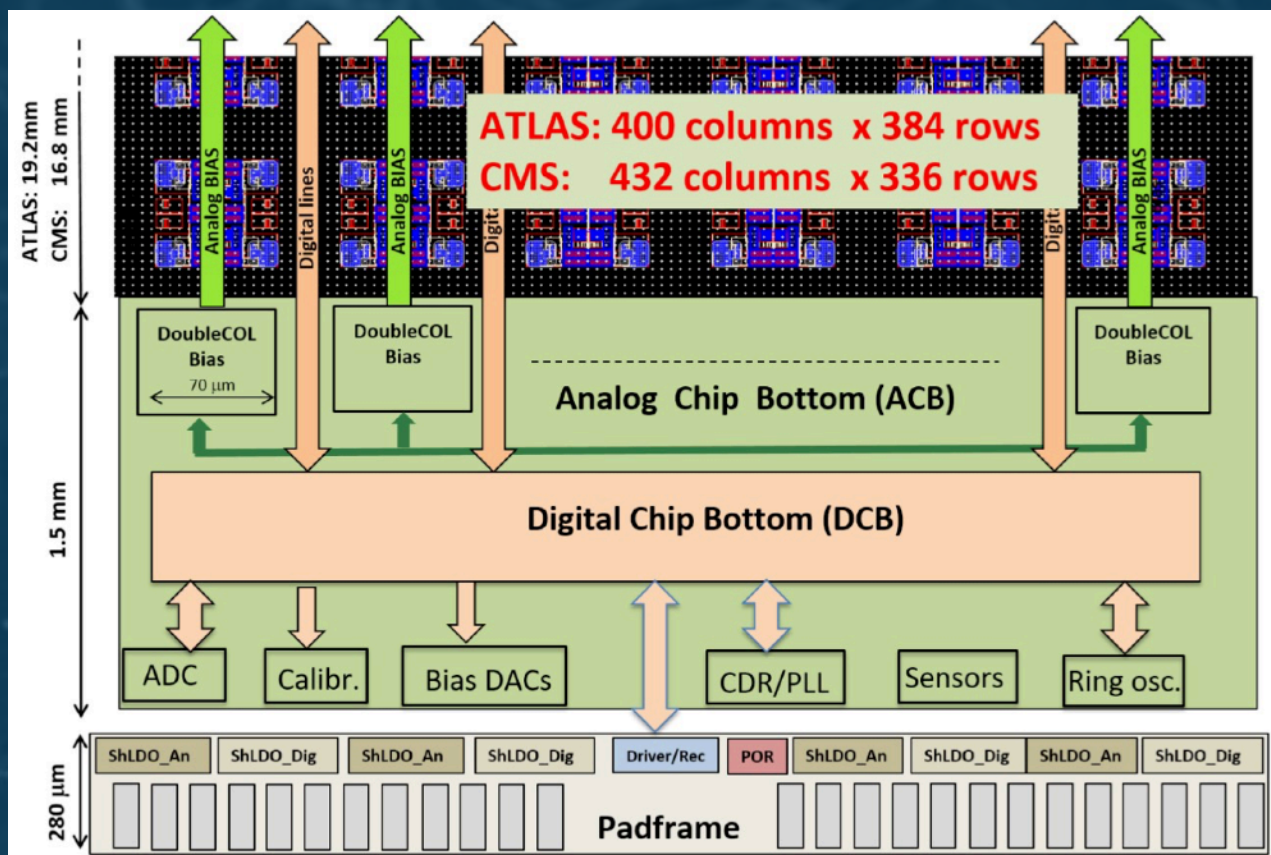
432 pixels / 21.6 mm

336 pixels / 18.3 mm



RD53B Chip Manual: <https://cds.cern.ch/record/2665301>

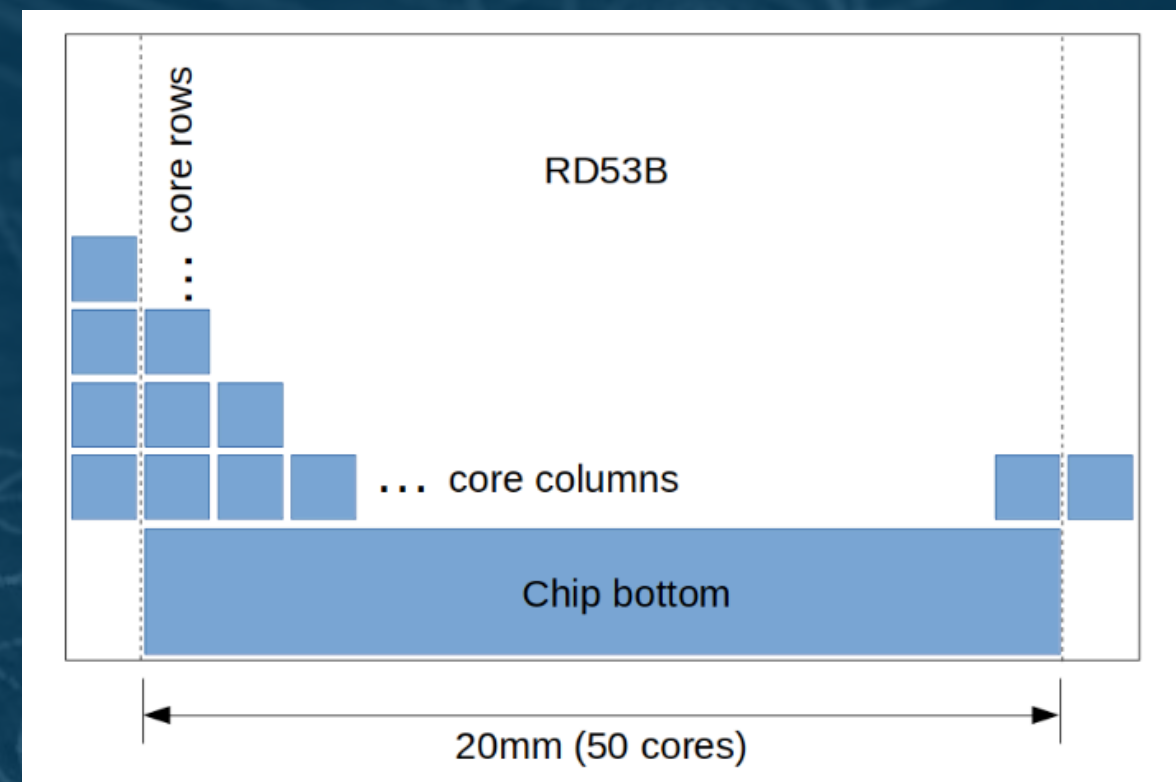
Analog View



Analog:

- Multiple analog blocks integrated in analog chip bottom
 - Most of them tested in-silicon in mini-ASICs before RD53B submission
- Analog islands organized in 2x2 pixels

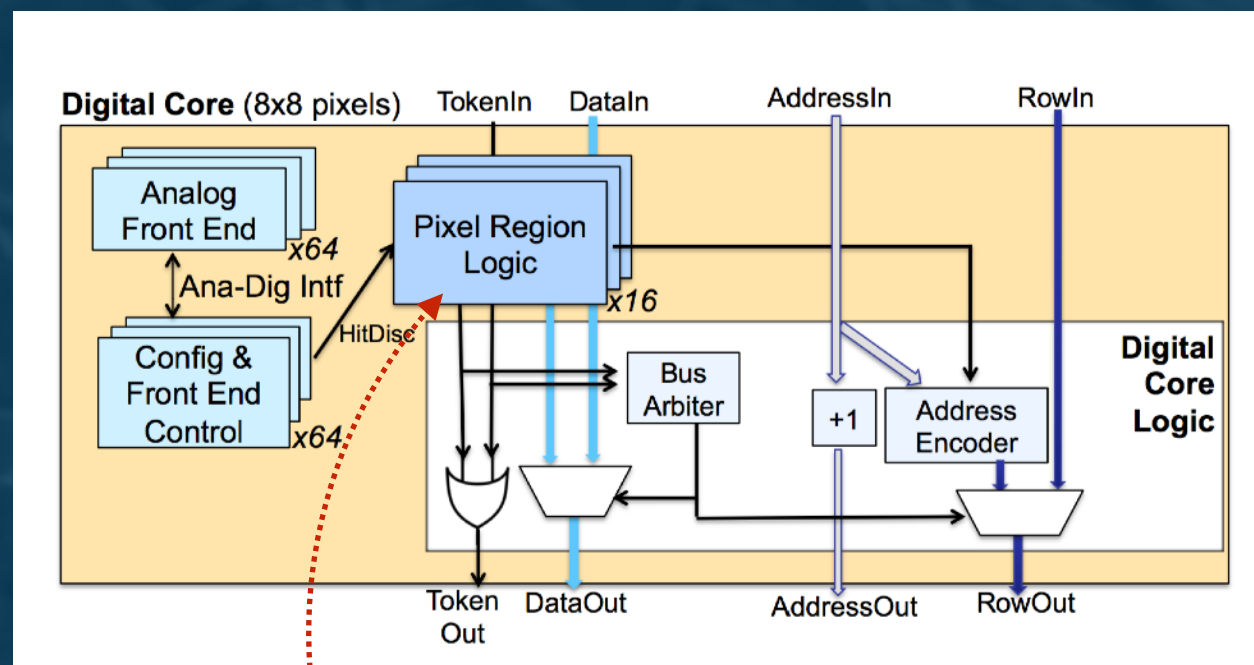
Digital View



Digital:

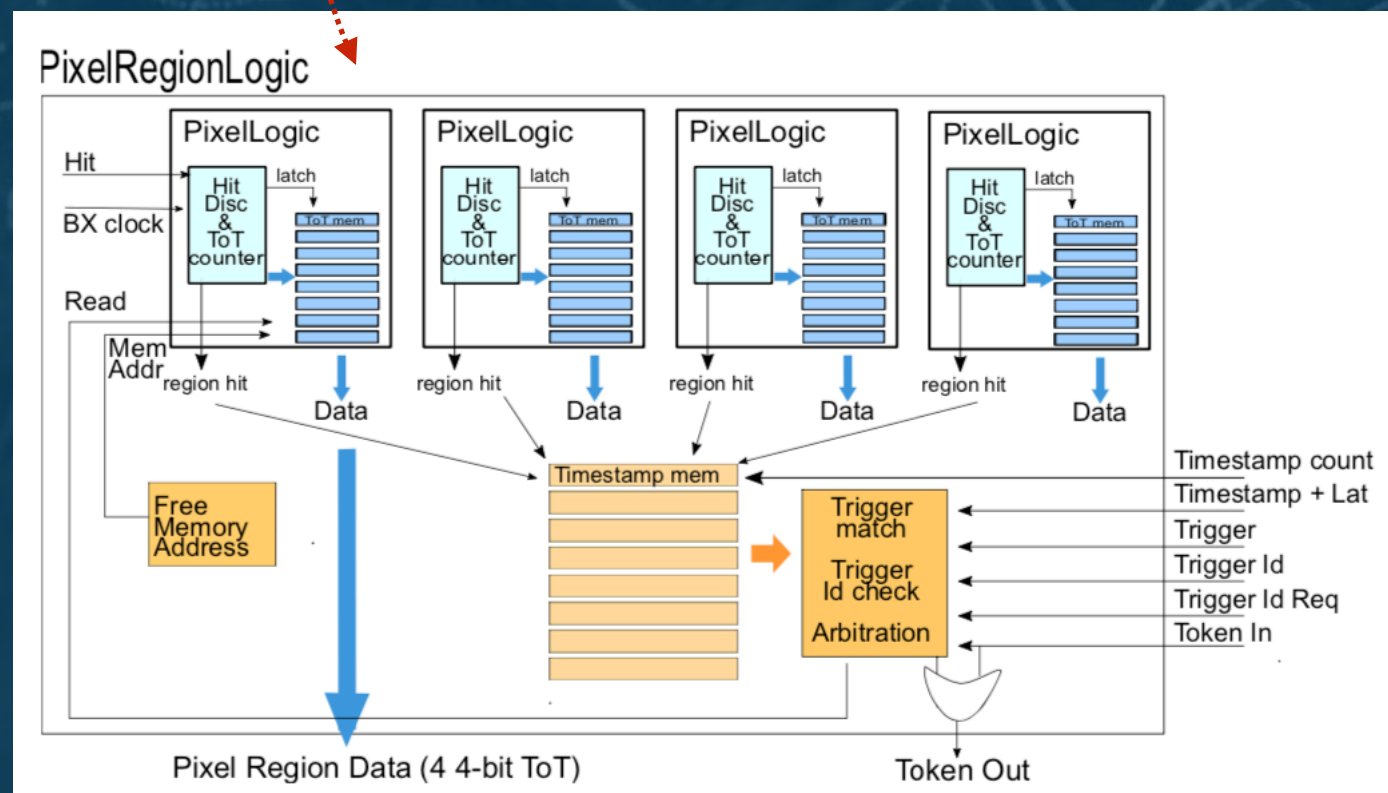
- Organized in digital cores (8x8 pixels)
- Core is flat digital synthesized “sea”, with 16 analog islands integrated
- Stepped and repeated to create pixel matrix
 - Number of core columns/rows is changed to create ATLAS/CMS chip
- Cores are interconnected for configuration and readout

Digital Core & Pixel Region Logic



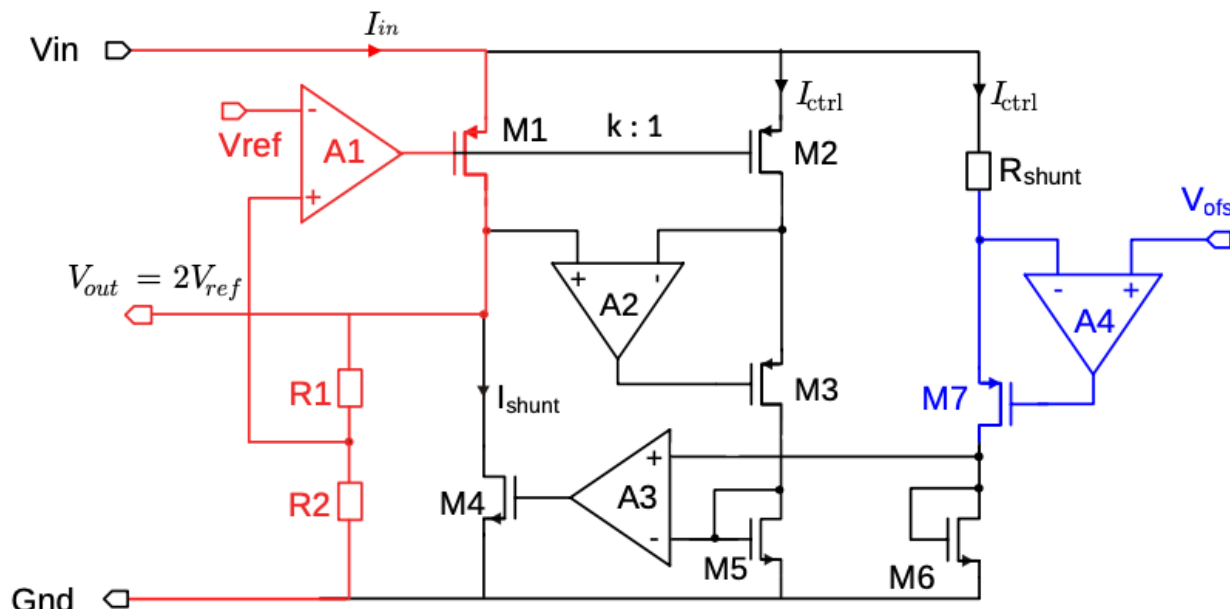
Digital Core:

- Contains 16x Pixel Region Logic (1x4 pixels)
- Read out of hits along core column

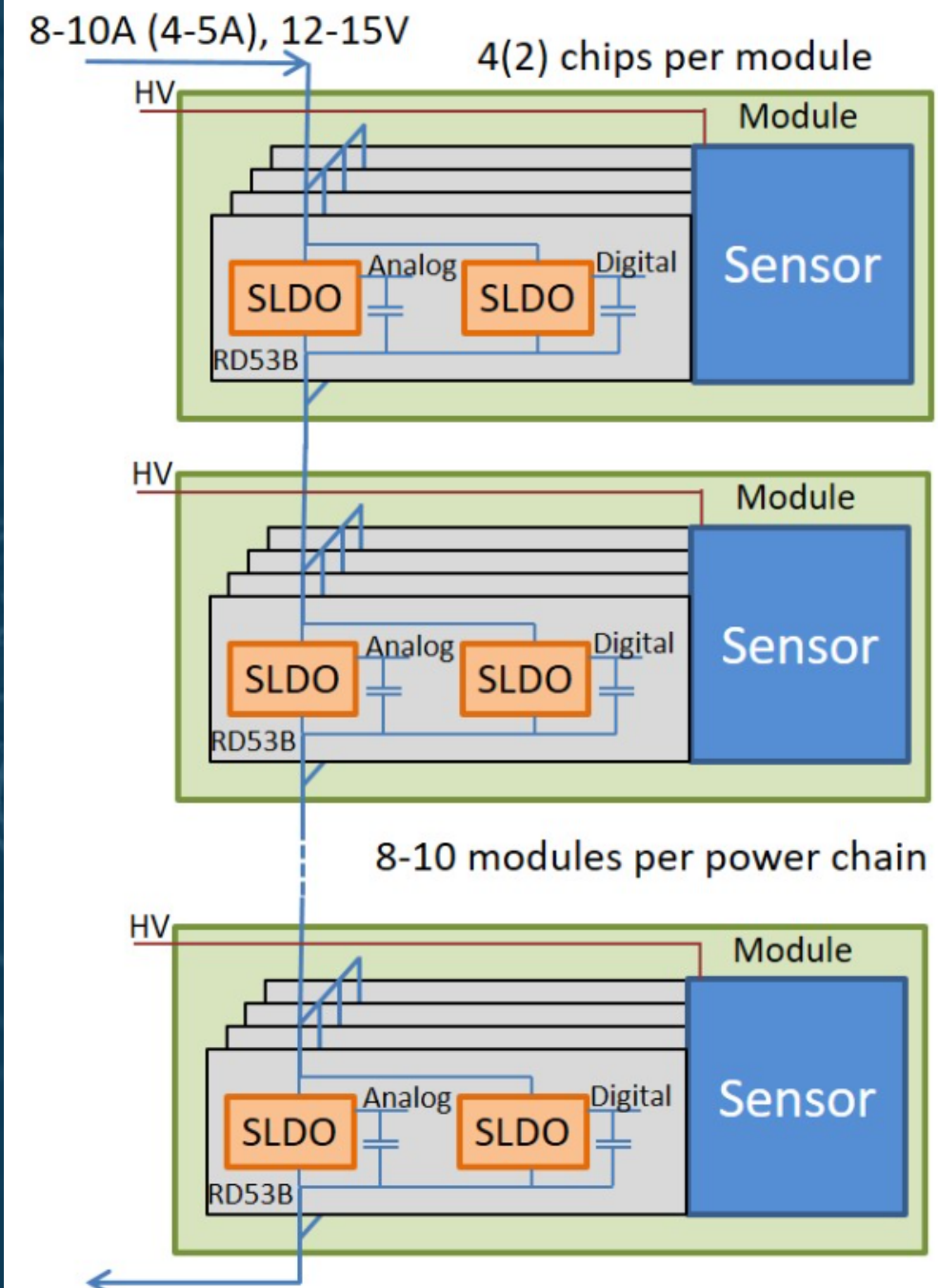
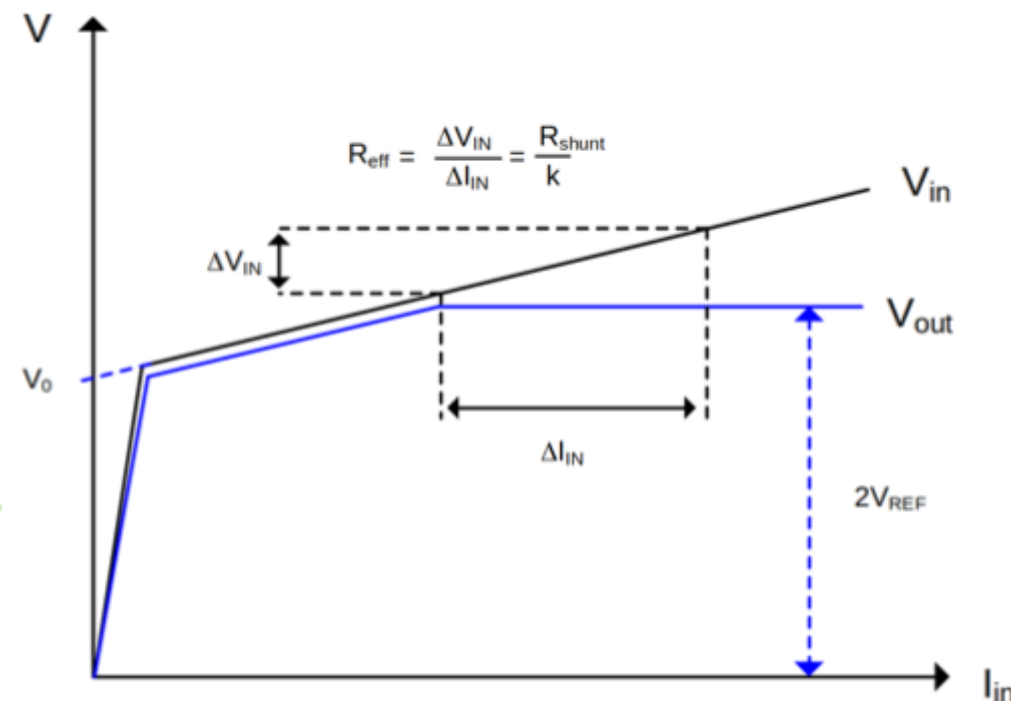


Pixel Region Logic:

- Hits are saved as ToT (Time-over-Threshold) associated to a time stamp (bunch crossing)
- Each pixel has 8x 4-bit ToT memories



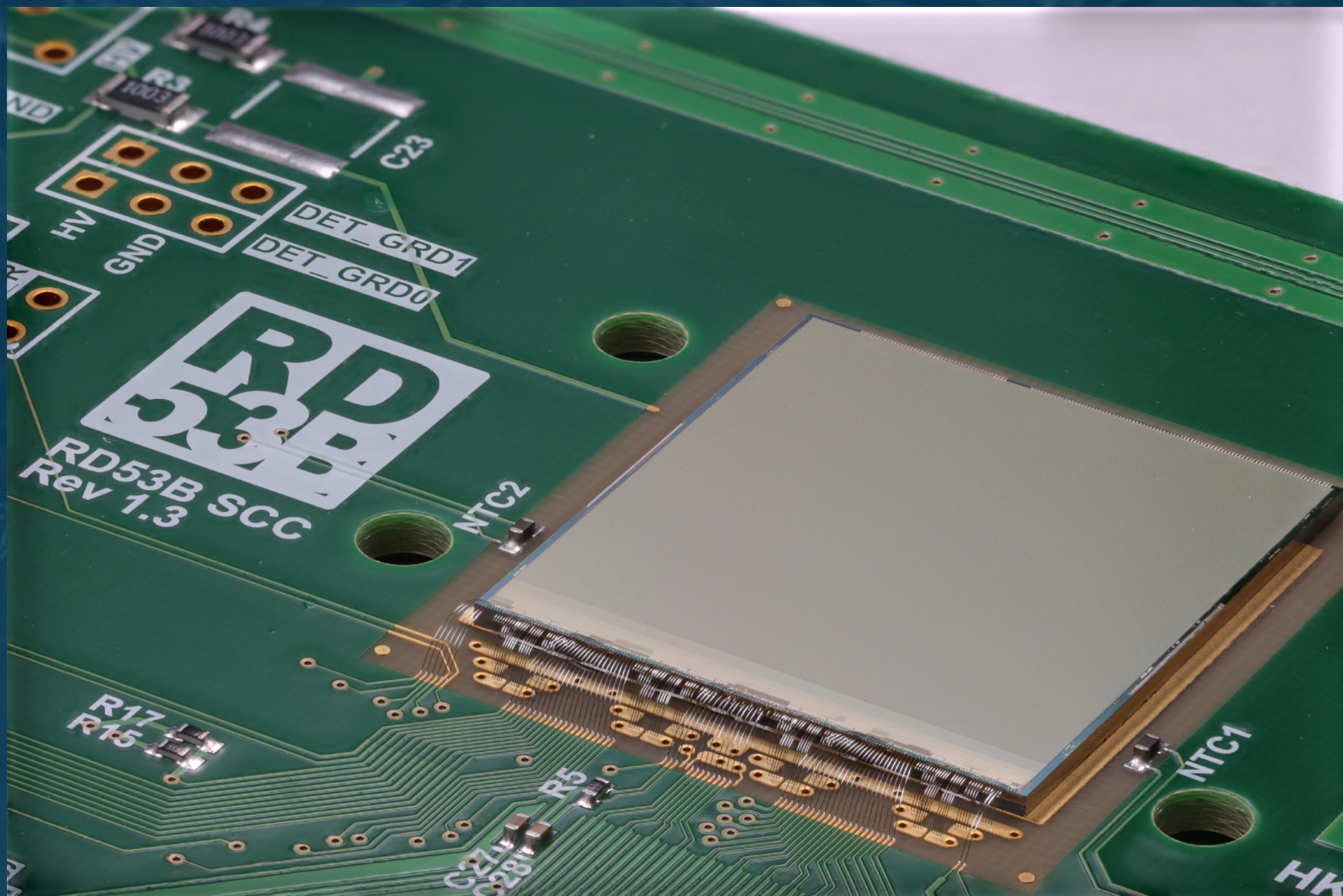
Linear Regulator Shunt Circuit Offset Circuit



Serial powering enables large reduction in mass of services.

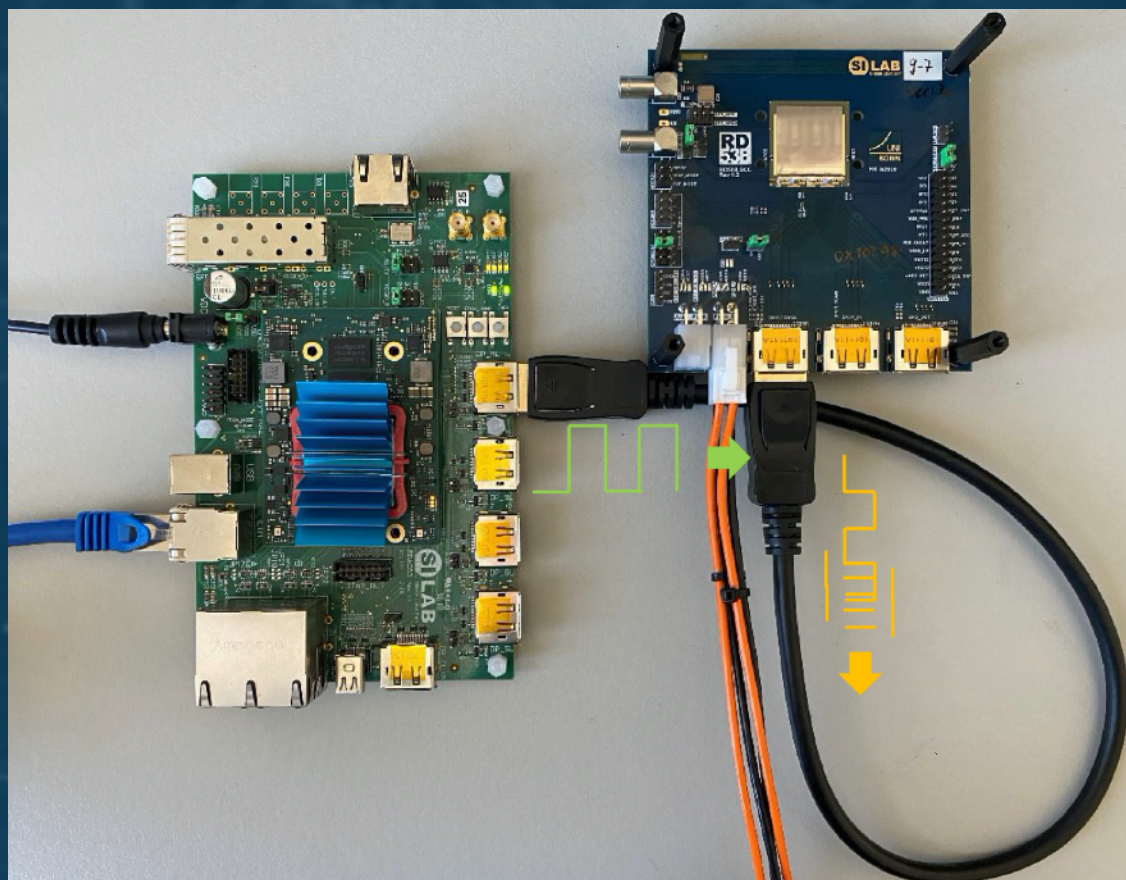
ITkPixV1 on Single Chip Card

June 2020



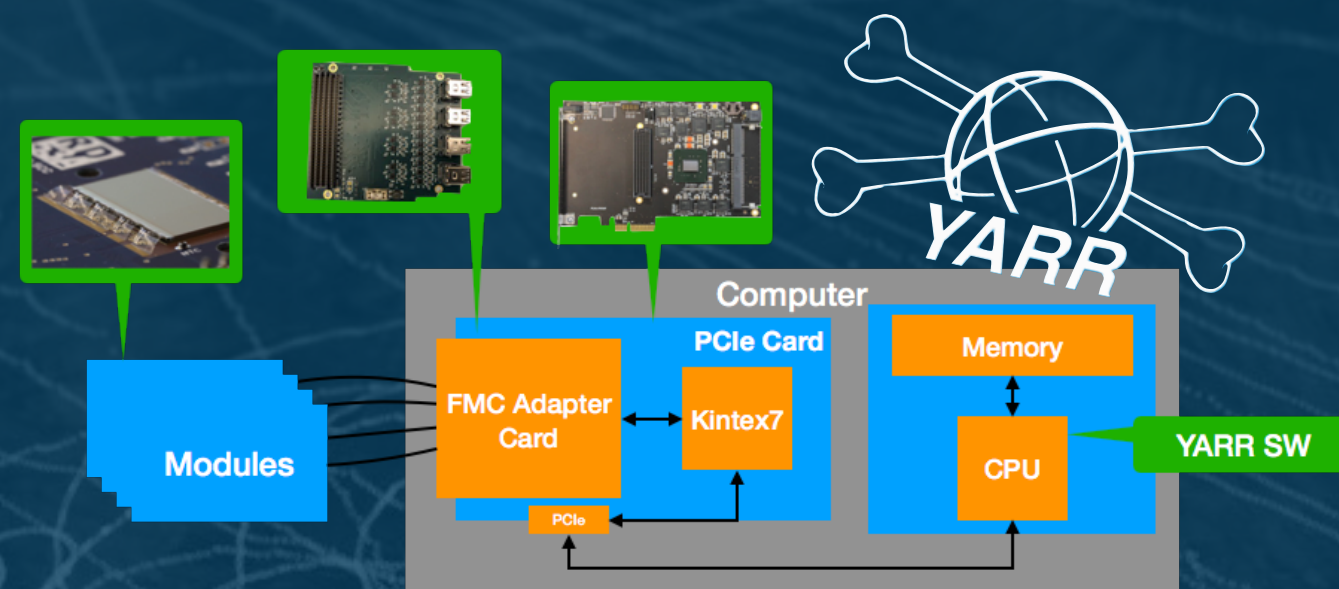
<https://gitlab.cern.ch/silab/bdaq53>

<https://gitlab.cern.ch/YARR/YARR>



BDAQ53:

- Custom base board with commercial FPGA plug-in
- Ethernet communication to PC
- Python based SW library
- Specifically targets chip characterization



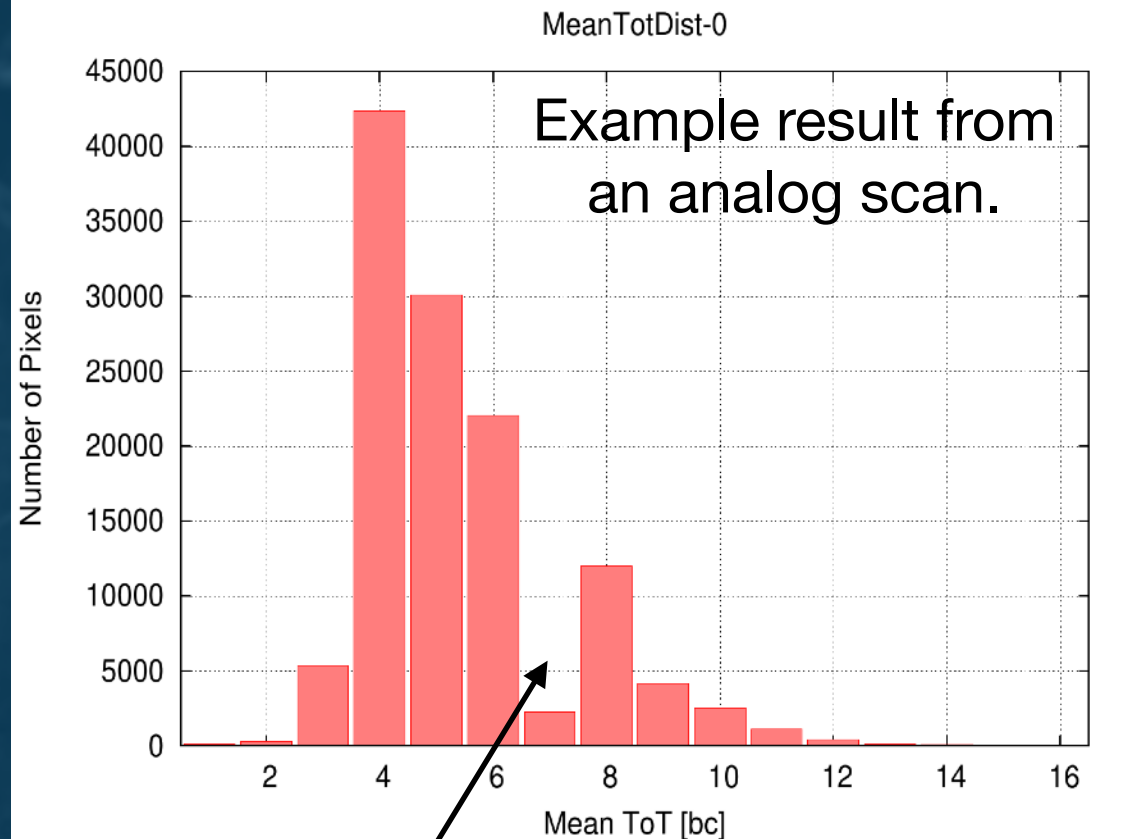
YARR:

- Commercial PCIe FPGA board with custom FMC adapter card
- PCIe communication to PC
- C++ based SW library
- Hardware agnostic SW aimed at growing from chip characterization all the way to detector operation

Does it work?

- All measurements up to now indicate that **94% of the chip is working!**
- However the **6% manifested in a large current on the digital rail** (around 2A @ 1V, analog current was as expected) which initially gave us a headache
 - Not a simple short and independent of clock
 - Behavior consistent over all chips tested (~20), multiple test sites (Bonn, CERN, LBNL), and wafer batches (production batch was split in two by TSMC)
 - Thermal imaging did not reveal any smoking gun
 - Analysis of PCM (Process Control Monitoring) shows no anomalies
 - All of this **points to a design bug** (with some hindsight)
- Does **not prevent us from chip operation and testing!**
 - Only prevents some high level system tests

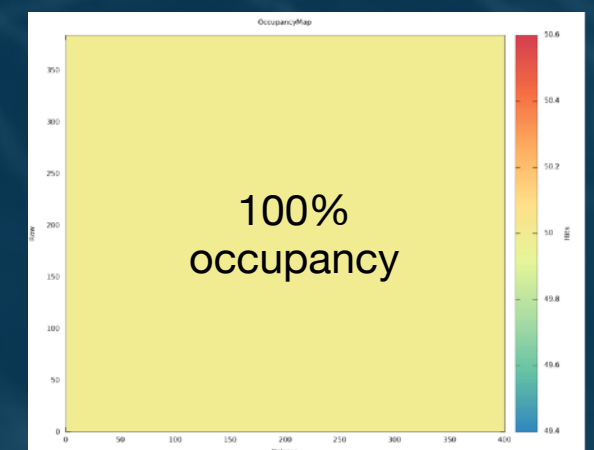
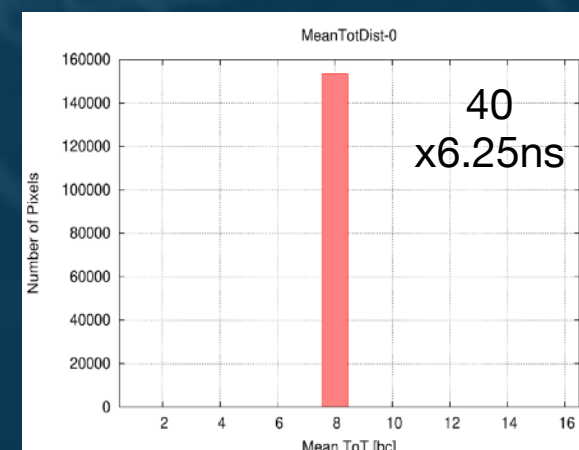
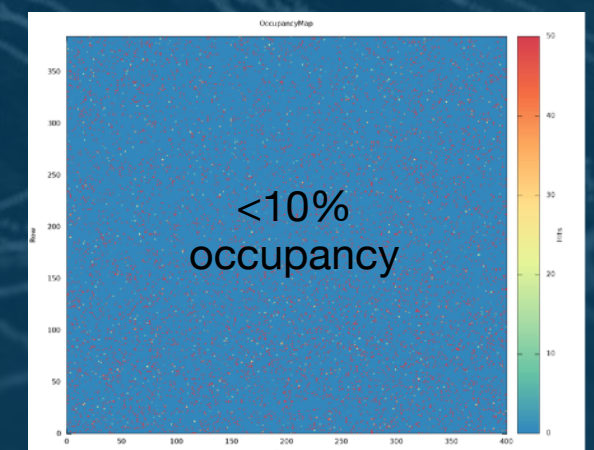
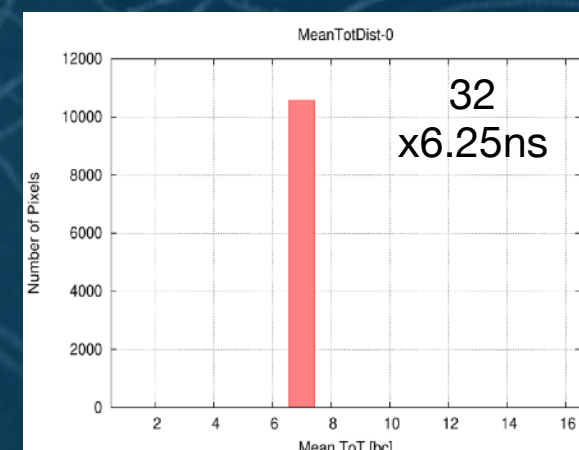
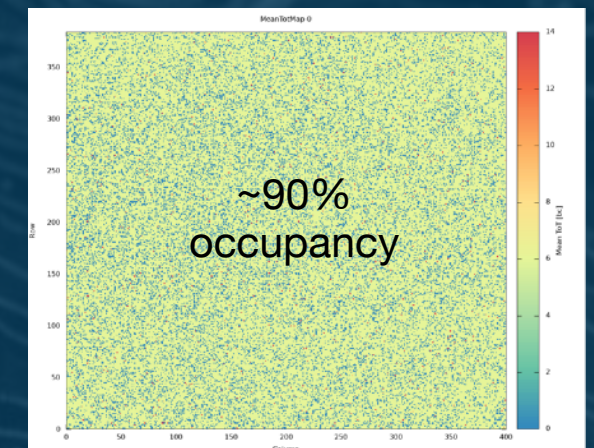
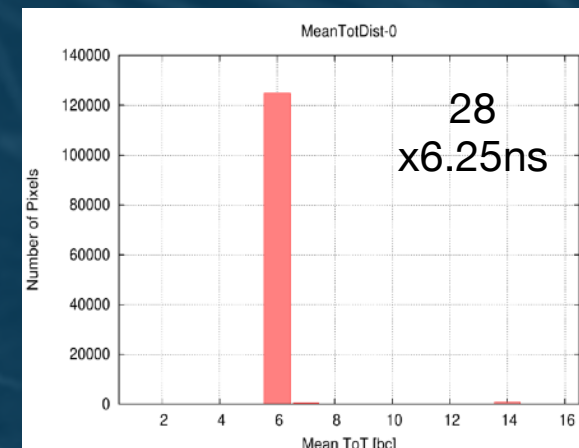
Missing ToTs



Missing hits for ToT=7

Hits with a ToT having more than one bit set '1' are "lost". ToT's with two '1's see around ~10-20% loss, ToT's with three '1's have more than 90% hit loss.

Digital Scans (fixed hit length)



- Missing ToTs pointed in the direction of the ToT memories
- Made from multi-bit latches (custom) used for the first time in RD53B due to area congestion (RD53A used a standard latch)
- **Discovered bug in multi-bit latch** which allows **direct path from VDDD to GND under specific circumstances**, which also leads to some internal nodes not being on a well defined potential and appearing as flipped to '1' bits on the output
- A ToT = '1111' is the internal code for 'no hit' and will not be read out, which explains the hit loss we saw for specific ToT values when all bits appear flipped to '1'
- Each multi-bit latch could have a **"leakage" of around 2uA** when in this state, 1.2M of these (153k pixels * 8) result in a **total current of 2.4A**
- This was further confirmed by setting all ToT memories to '0000' which results in no direct path from VDDD to GND
- **In this state the digital current is as expected** (200mA with no cores enabled, 600mA with all cores enabled)

Working with current ITkPixV1:

- **Chip verification is proceeding**, most blocks can be tested in this version albeit sometimes needing some work arounds
 - Analog front-end will be verified using the precision ToT feature
 - Setting all ToT memories to '0000' sets the chip in normal current state
- Main issue: high power-up current makes it impossible to use this chip for system testing of serial power chains

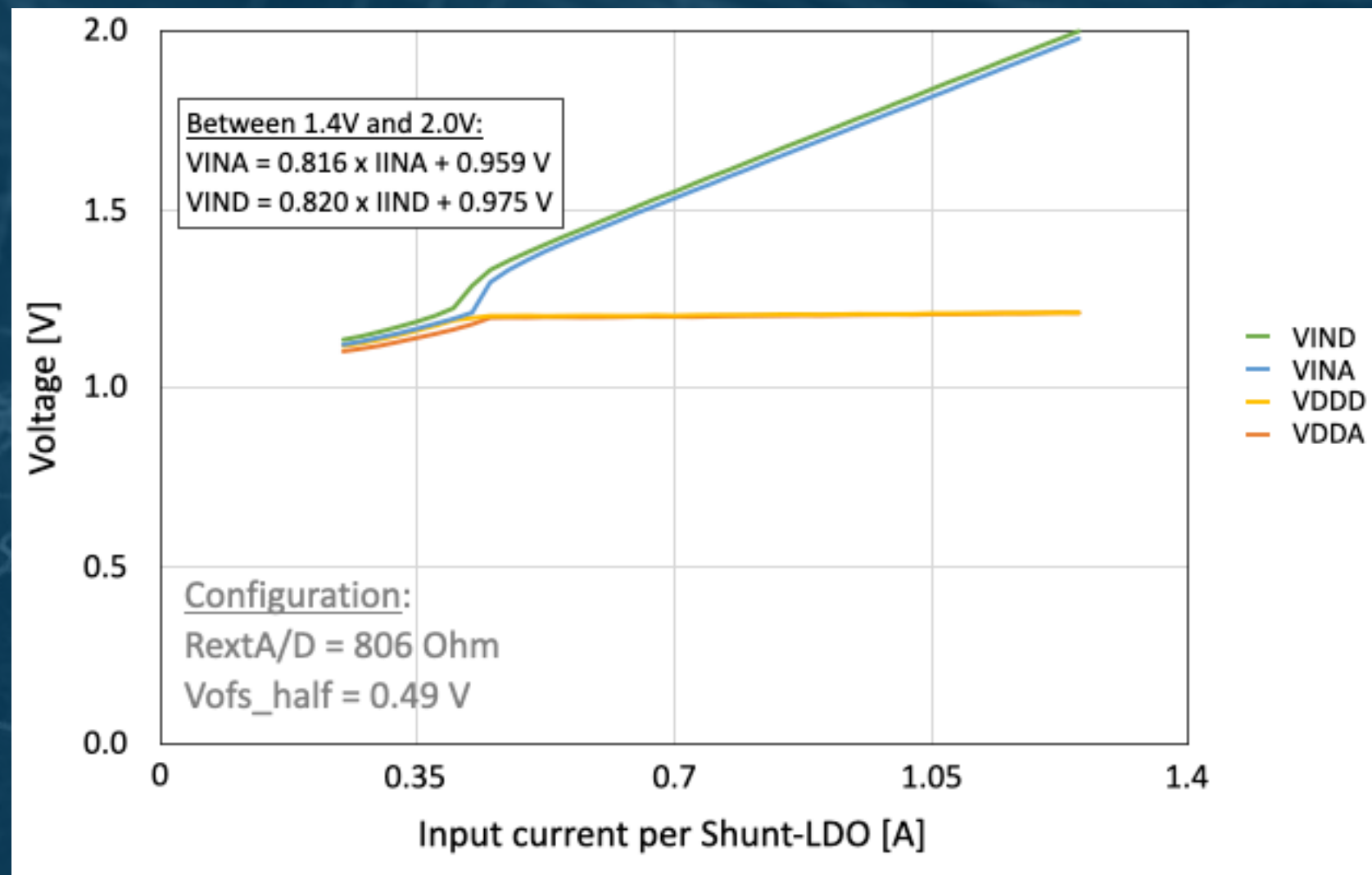
Patch in metal Layer (ITkPixV1.1):

- 4 wafers are being held at TSMC before further processing (after poly)
- Found way to fix high digital current and hit-loss, by transforming the multi-bit latch into single-bit latch
 - Only requires change of two masks (M1 and VIA12)
 - Submitted this week
- ITk Pixel **pre-production will rely on this chip**

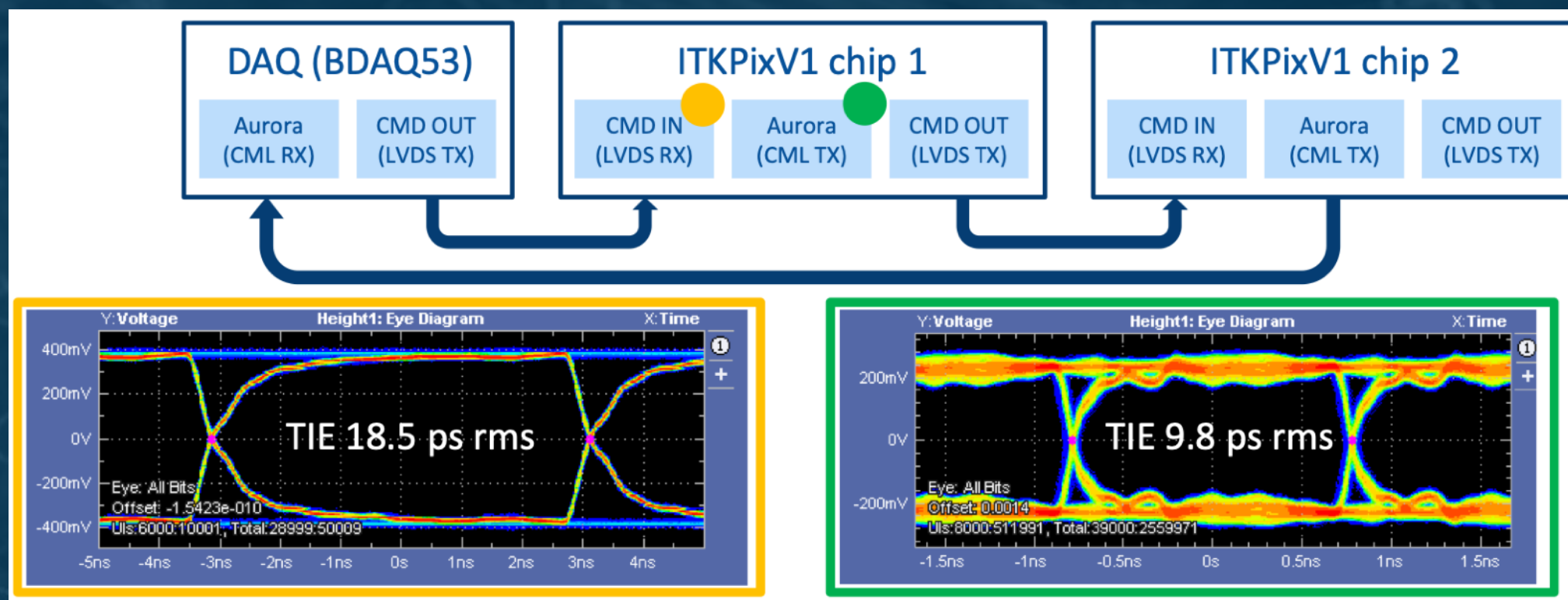
Towards CMS submission and ITkPixV2:

- Due to the high routing congestion multi-bit latch can not simply be replaced by single-bit latches
- A new multi-bit latch has been designed and verified, but the space saving is not as dramatic (only around 75% smaller than single-bit latches)
- Some triple redundancy in the pixel registers can be dropped to make space
- **Work in progress**

Shunt-LDO Regulator



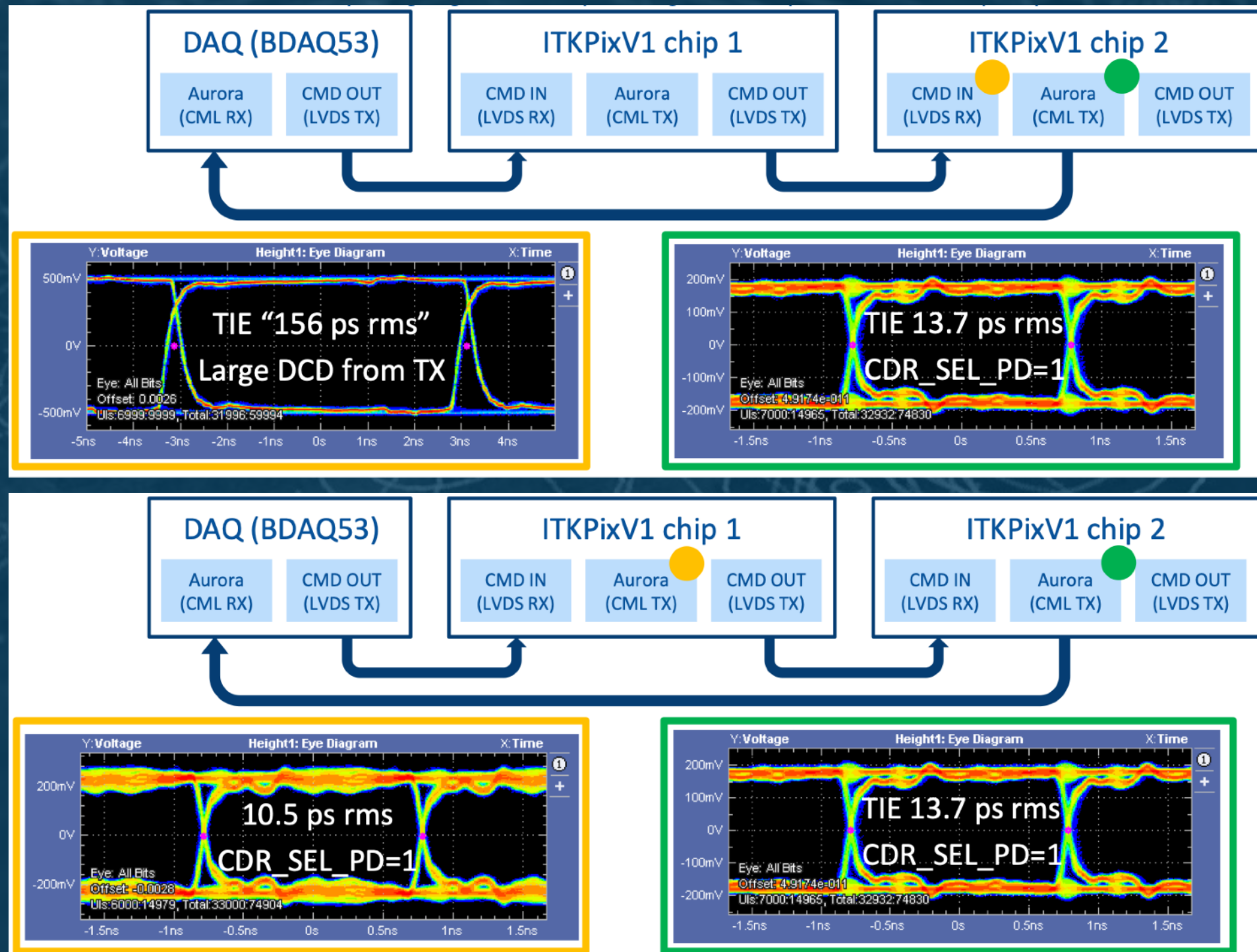
- Once digital current reduced, **Shunt-LDO behaves as expected**
 - Note specific shunt configuration shown not final
- Preliminary tests of over-voltage and under-shunt protection successful



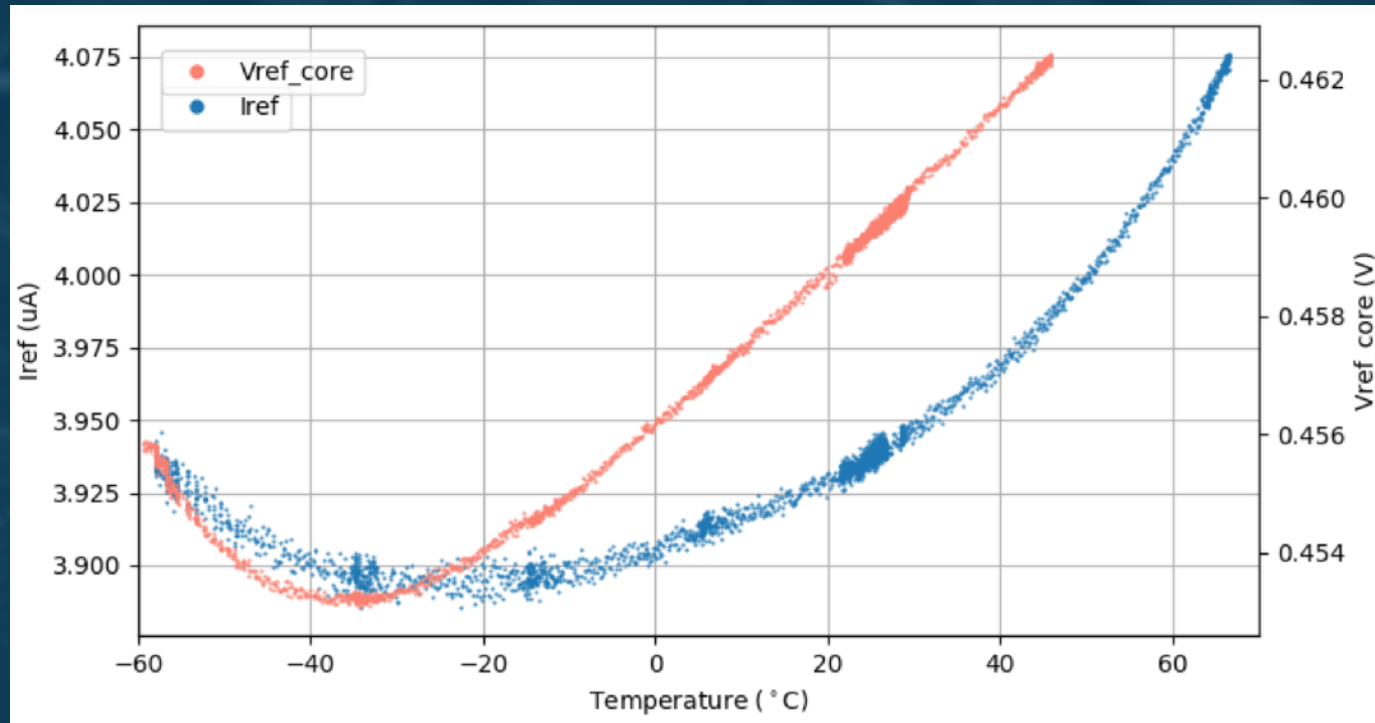
- 160MHz clock recovered from custom DC balanced CMD protocol (160Mbps)
 - 40MHz bunch crossing clock derived via special sync frames
- Internal PLL multiplies 160MHz up to 1280MHz clock which is used to drive the four 1.28Gbps data outputs
 - Need very low jitter to drive signal through more than 6m low-mass cable and be received within margin
- First measurement with ITkPixV1 showing **CDR working within requirements**
 - **Huge improvement** compared to RD53A

CMD Forwarding

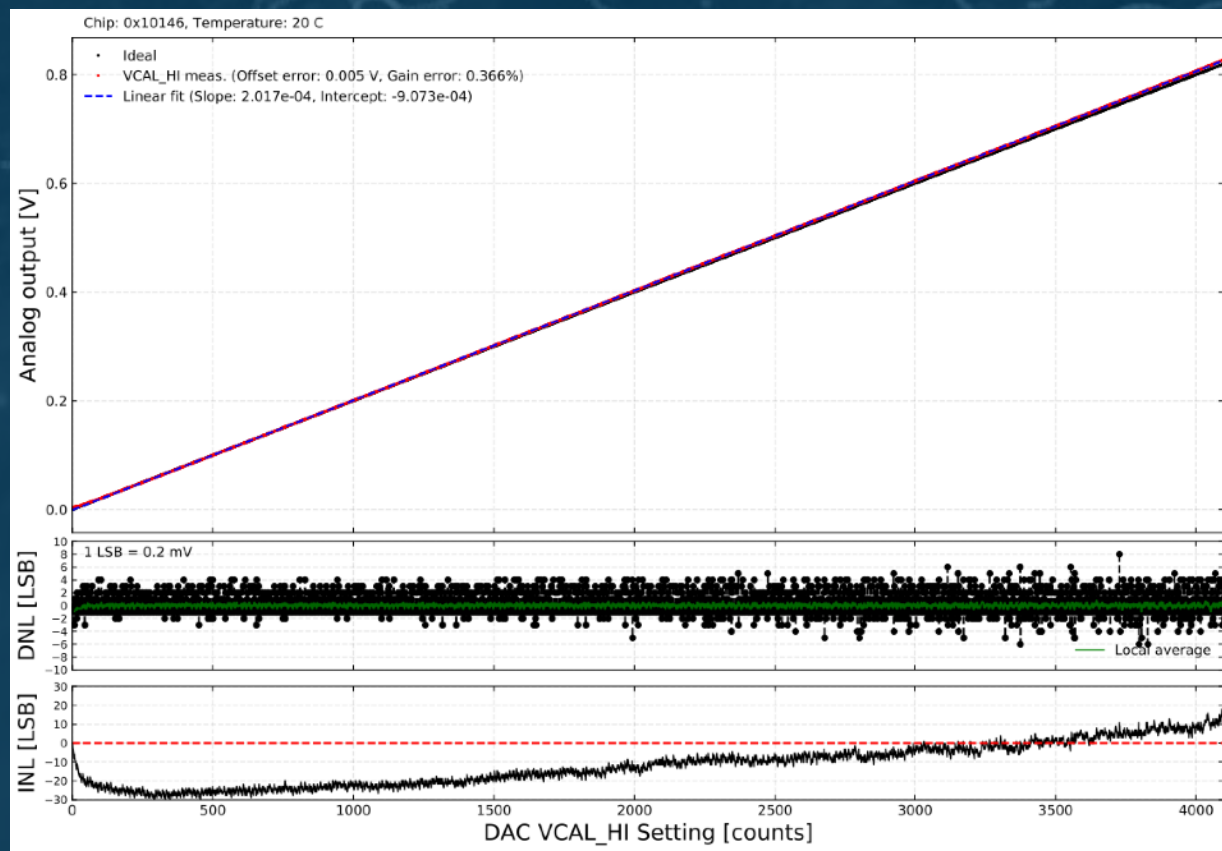
Global purpose LVDS outputs allow forwarding of CMD (to save on services).



Analog Circuits



Reference Voltage:
4% difference
over 120C temperature range

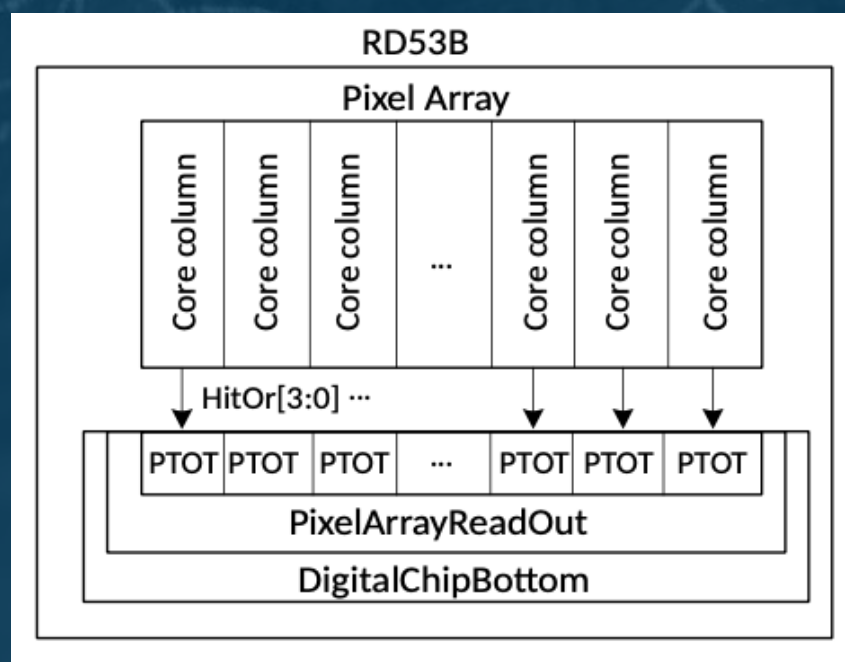
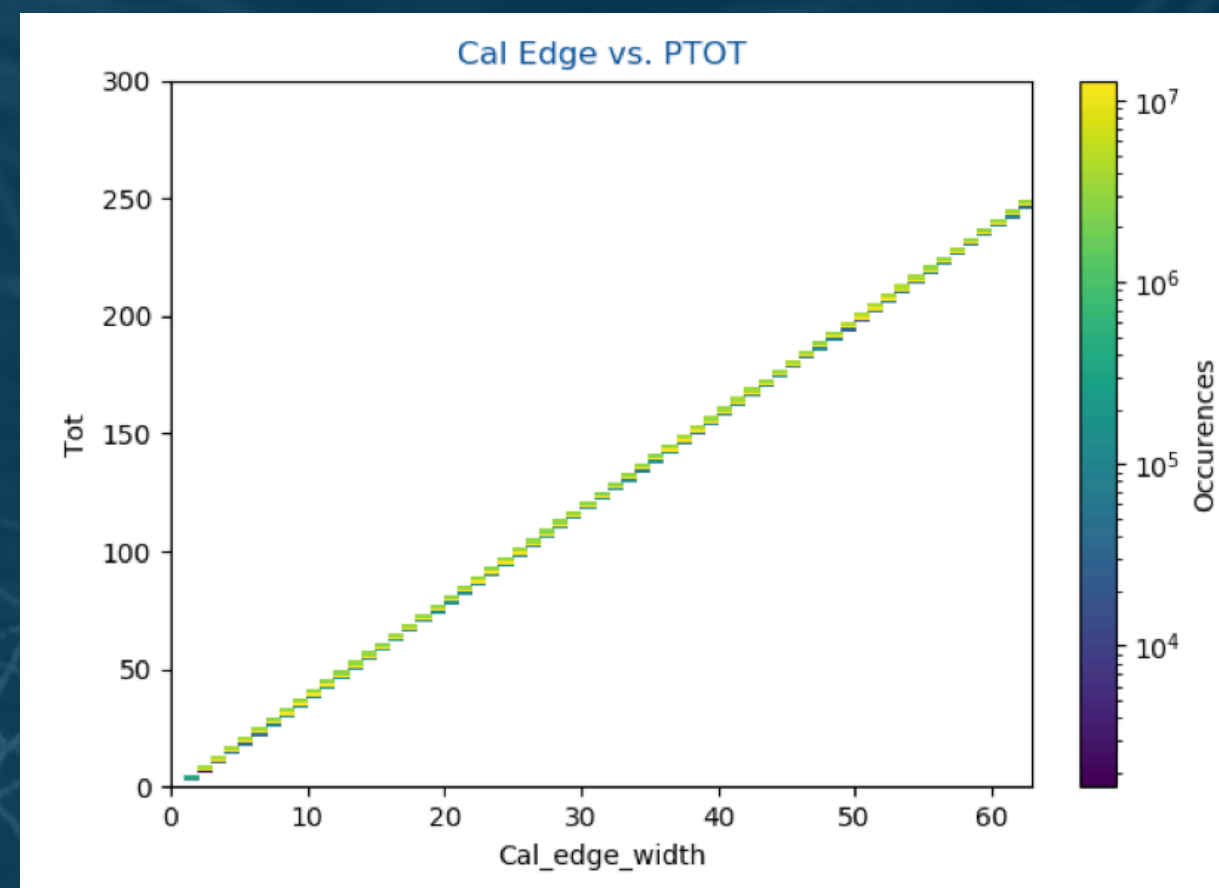
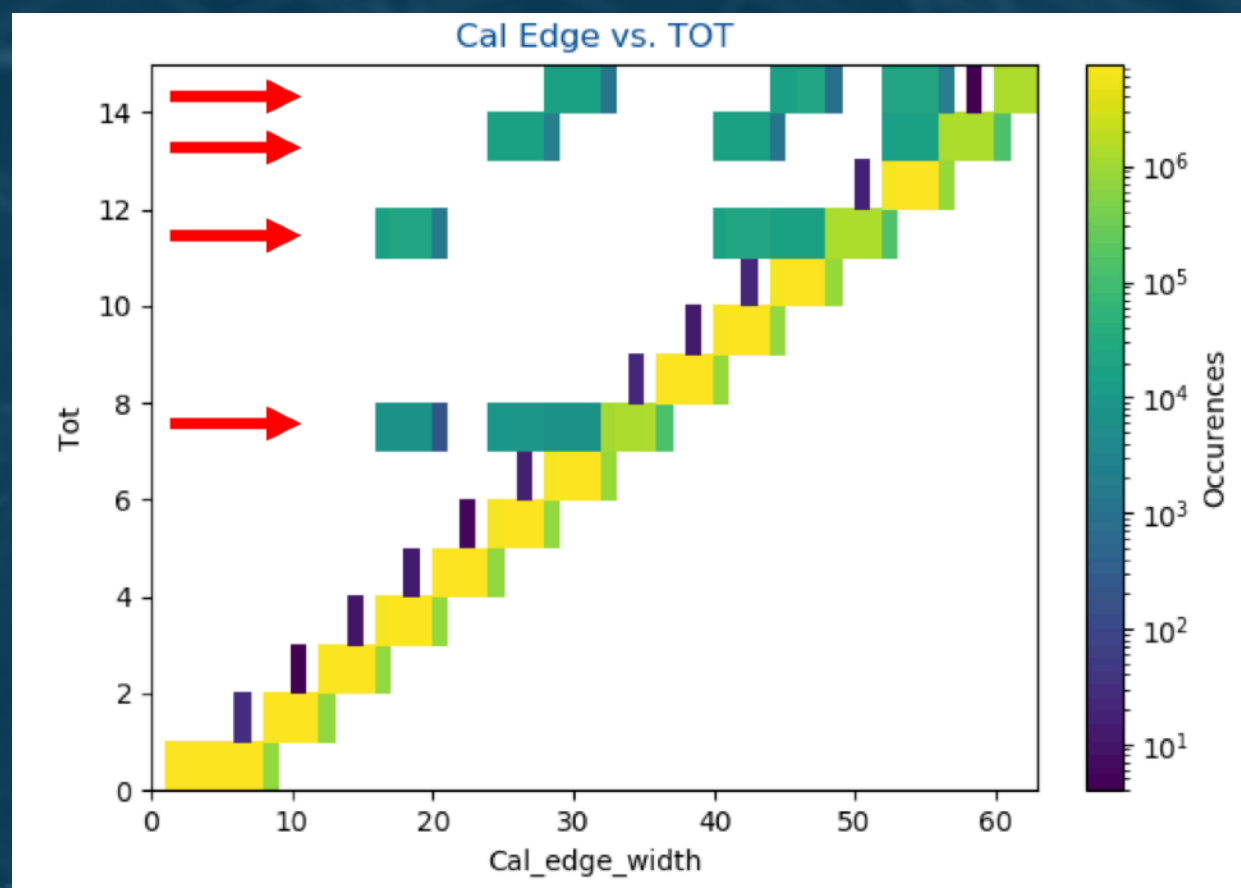


Injection DAC linearity measurement.

Internal capacitance measurement circuit can determine injection capacitance and derive DAC to electron conversion:

Chip	Cap [fF]	Cap Error [fF]
0x10157	7.565	0.01
0x102b7	7.351	0.01
0x102a7	7.465	0.01
0x10165	7.379	0.01
0x10277	7.436	0.01
0x10297	7.522	0.01

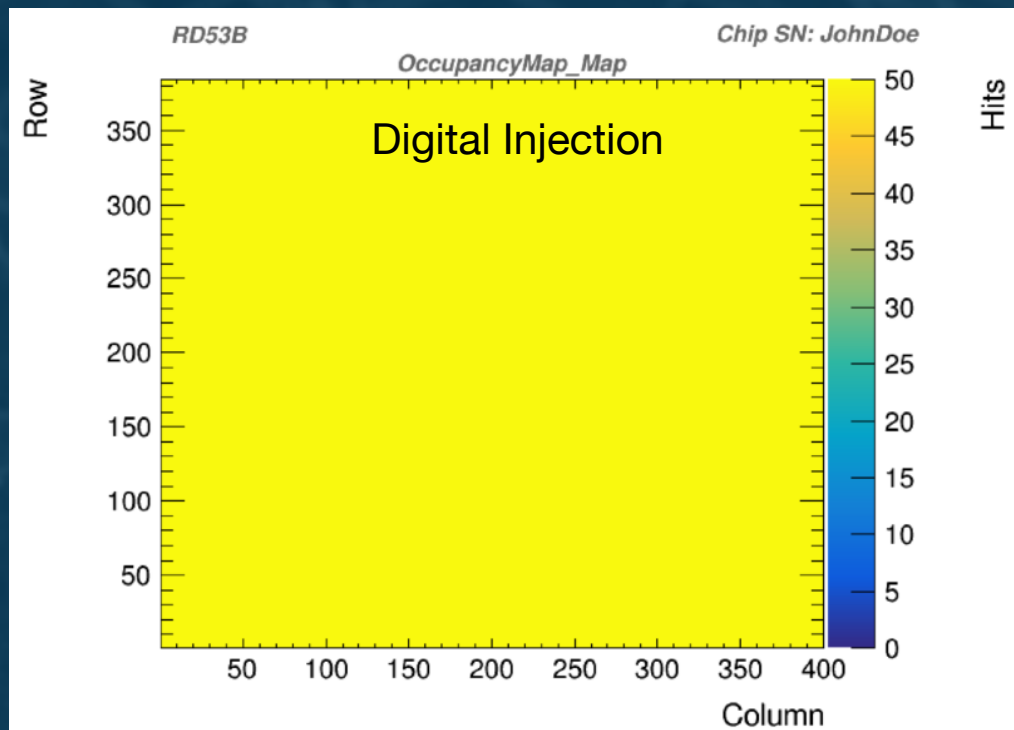
1 LSB = 5e



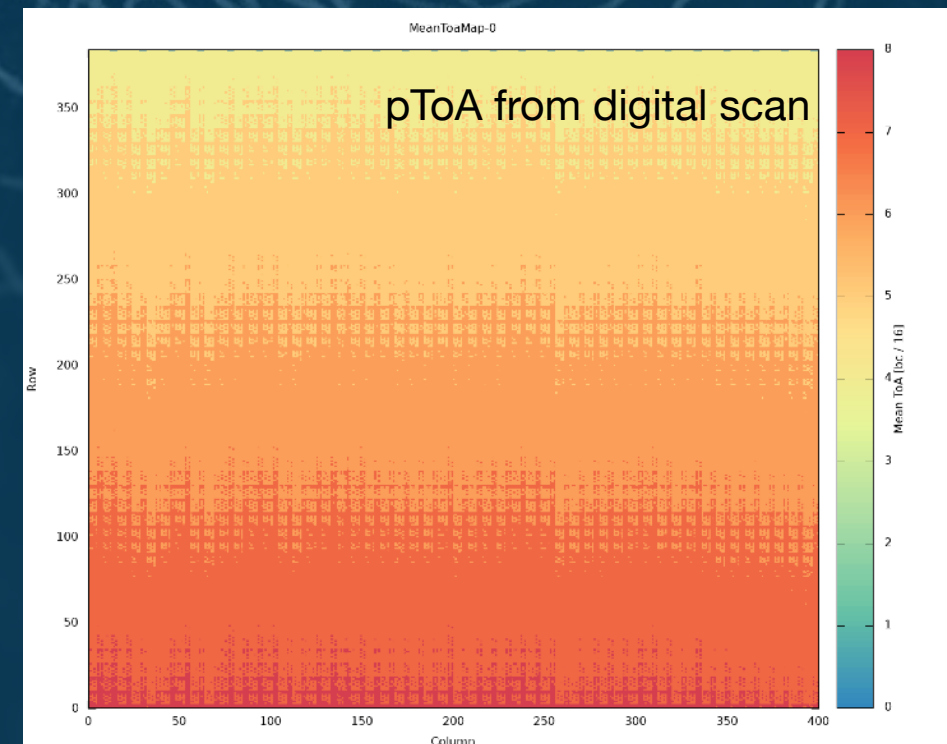
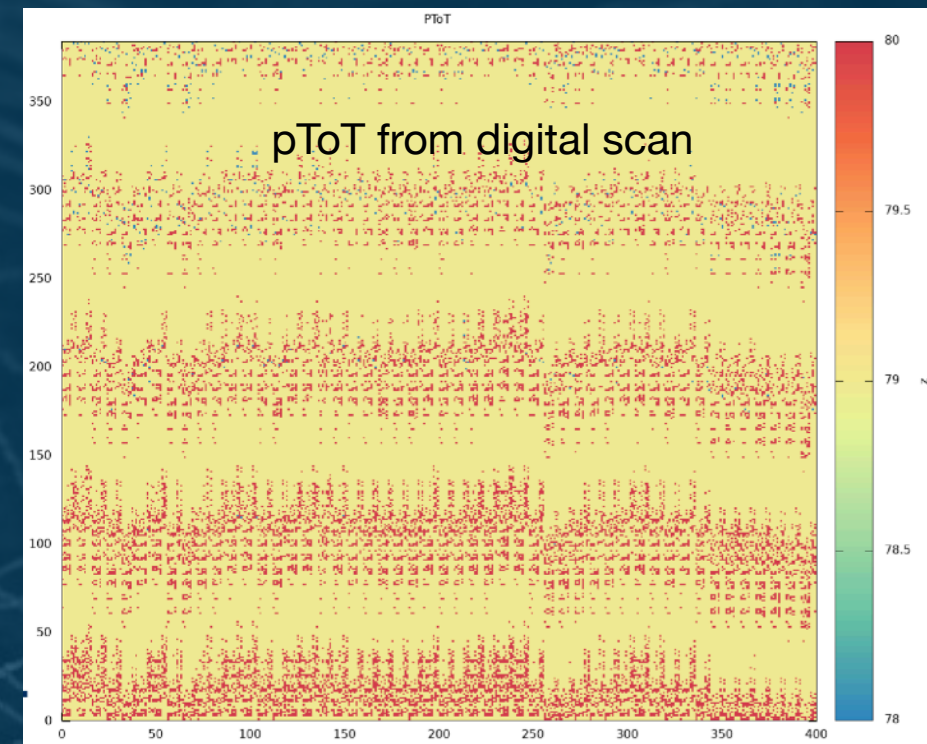
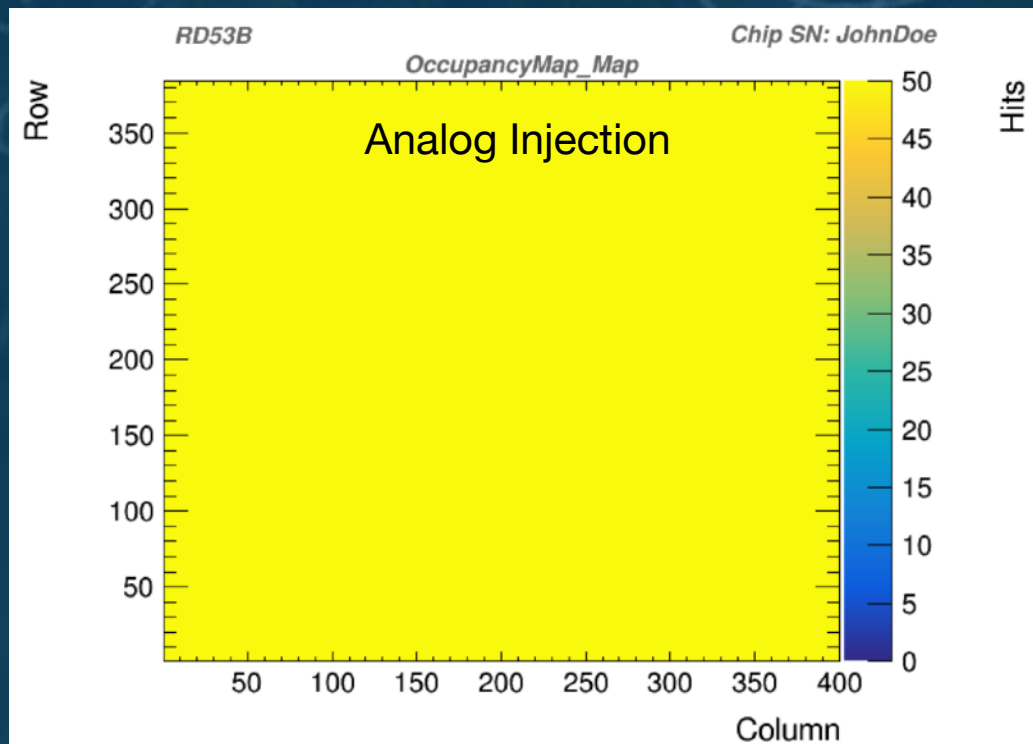
Precision ToT/ToA:

- Each core column has 4 precision ToT counters (640MHz) connected to HitOr bus
 - HitOr bus: OR of all pixel discriminators
- Does not use multi-bit latch as memory
- Only know column information
 - Can recover pixel position during scans by knowing injection configuration
- Also gives precision timing information (1.5625ns)

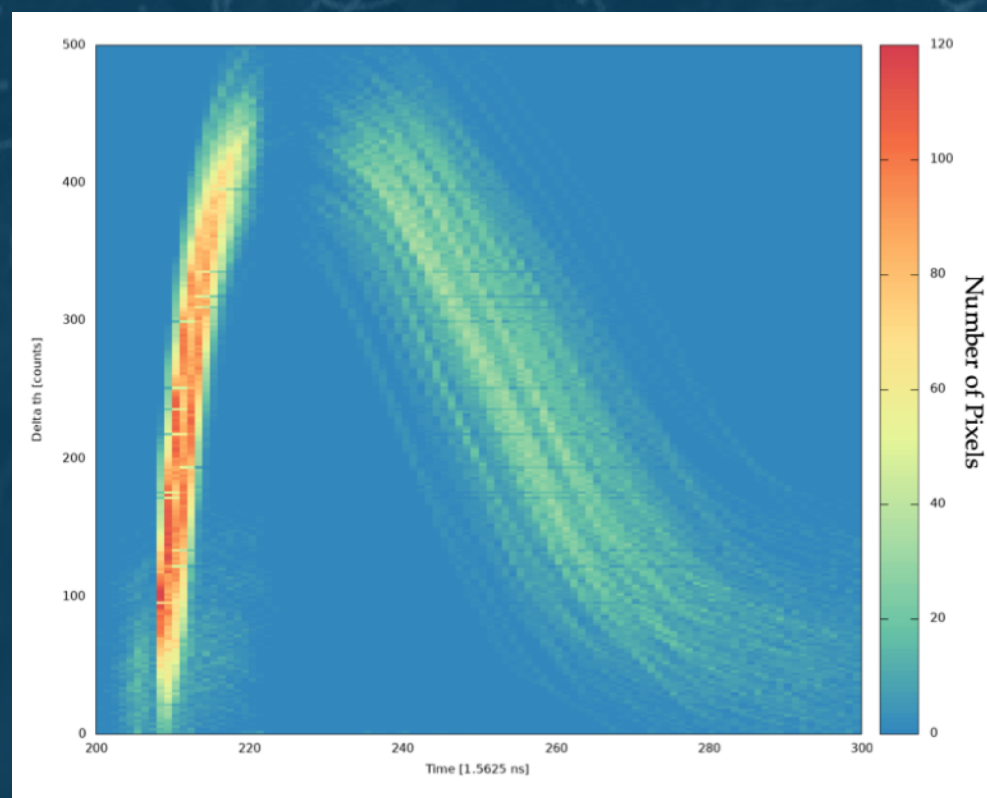
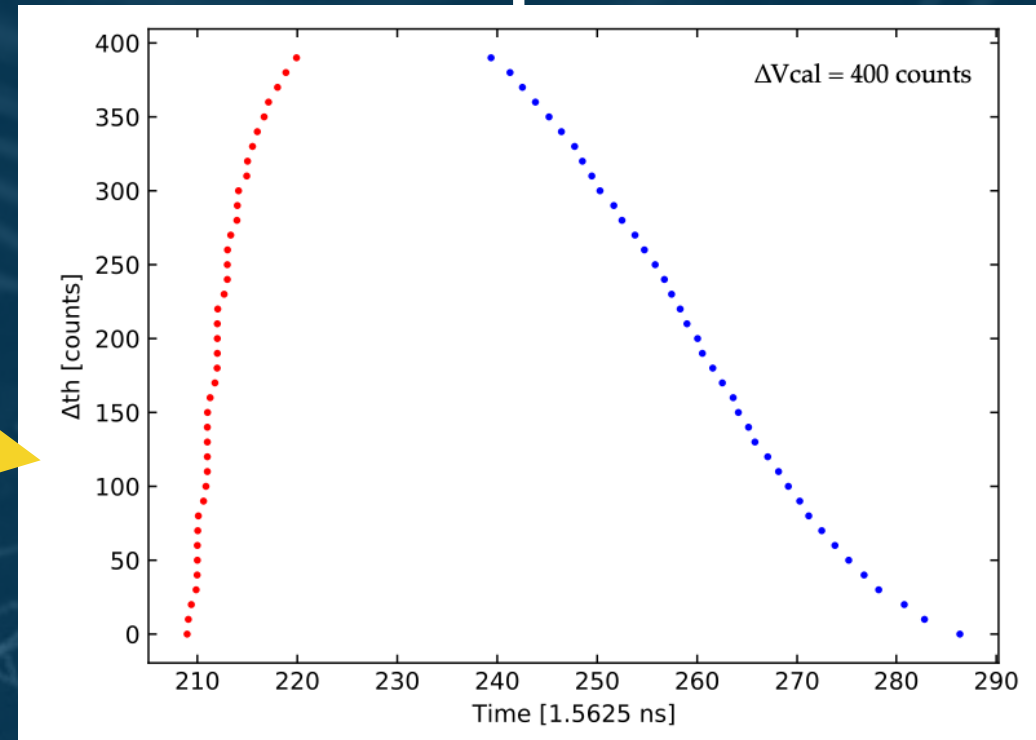
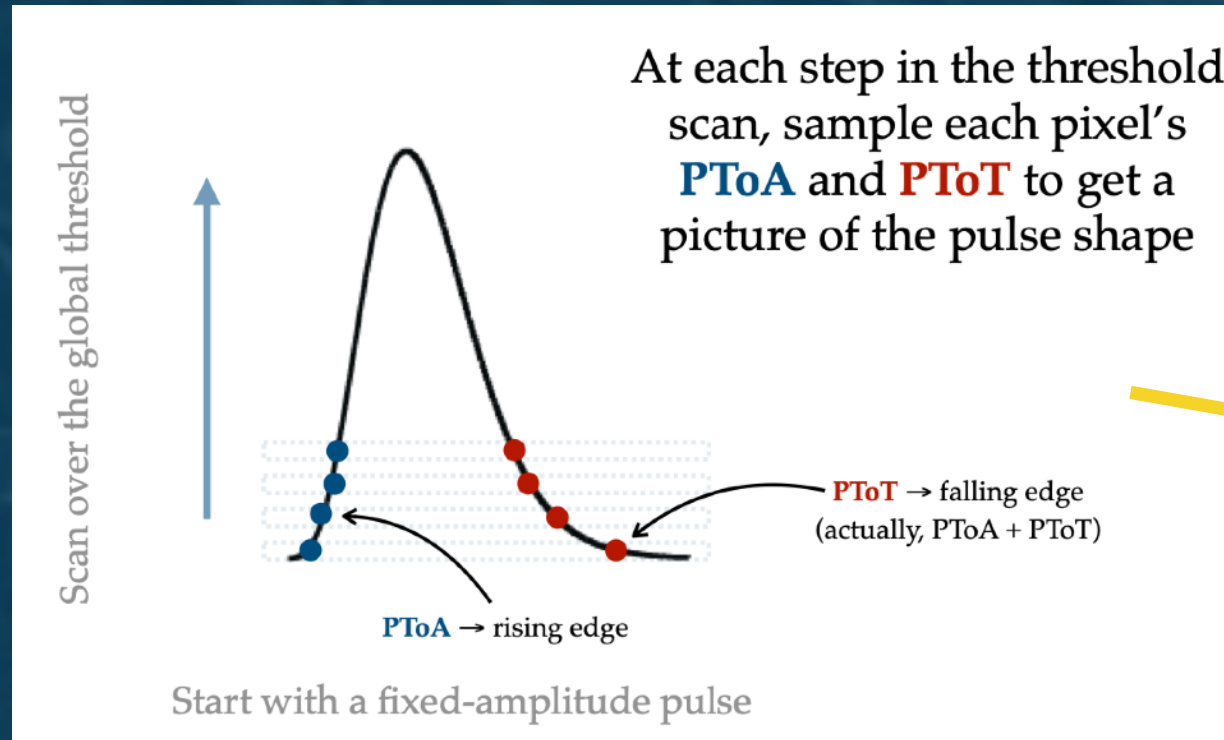
Digital and Analog Scans



All 153600 pixels responding 100%

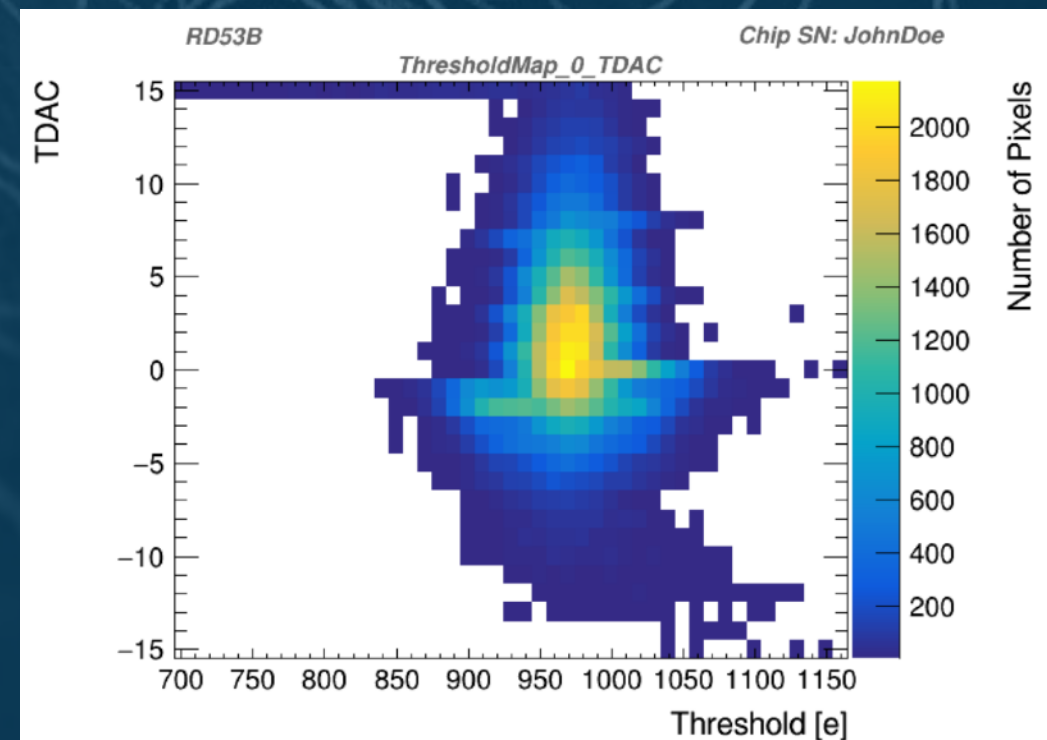
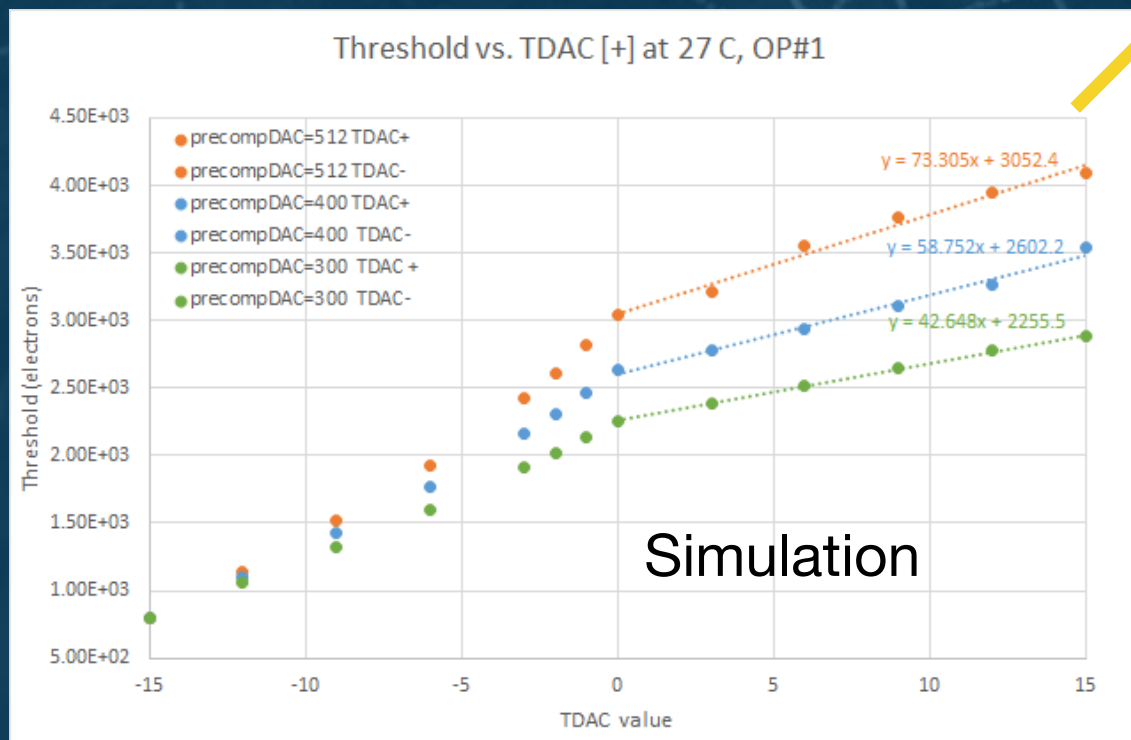
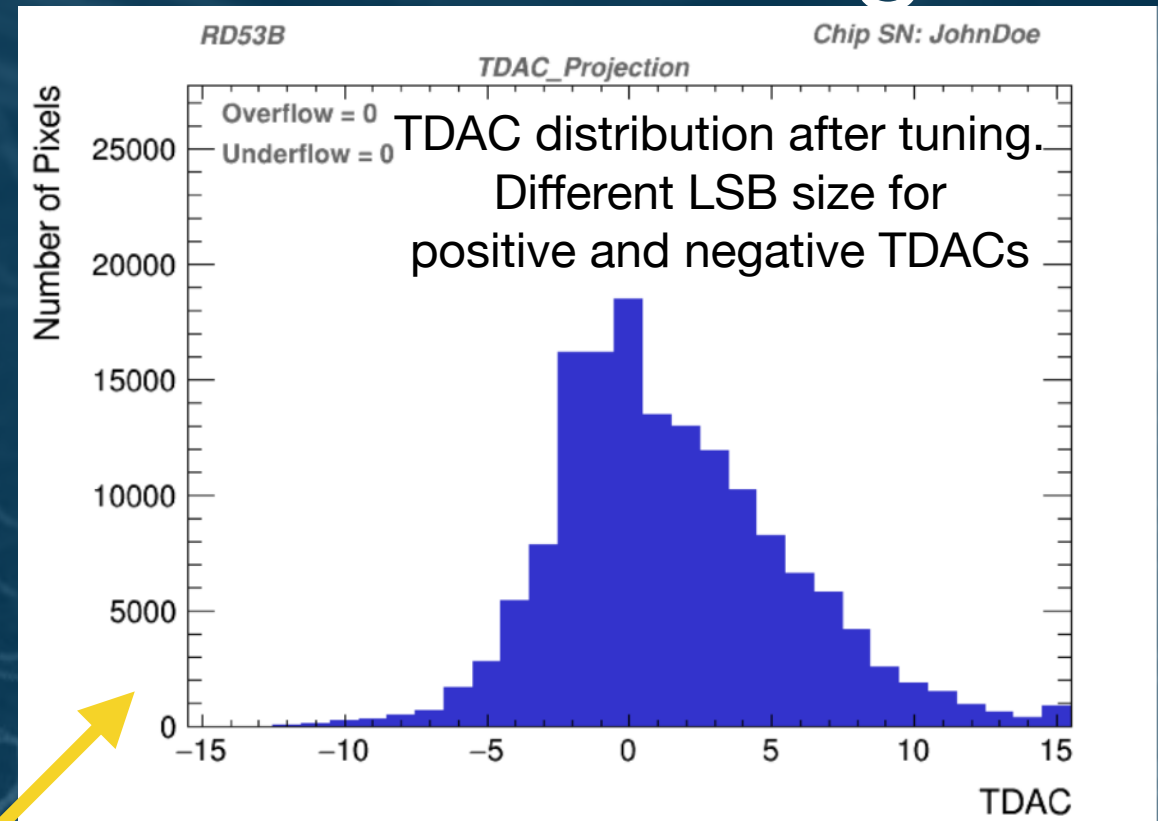
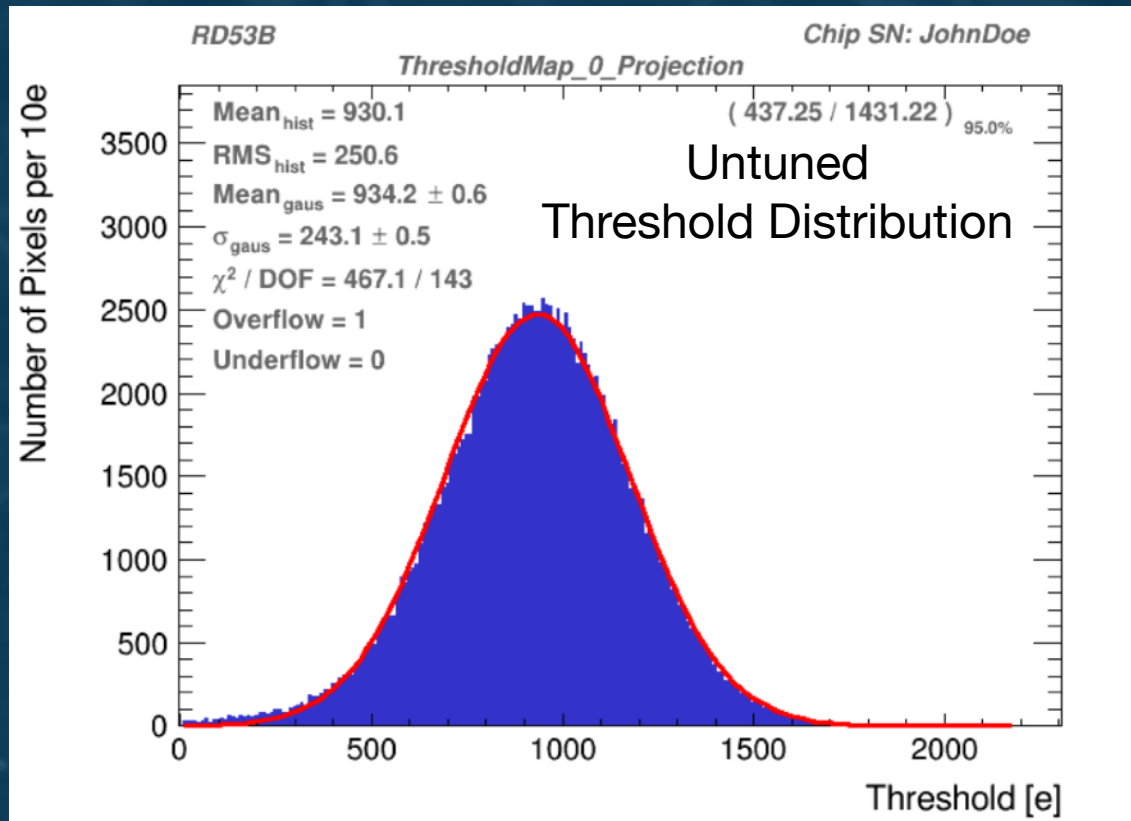


Front-End Scope

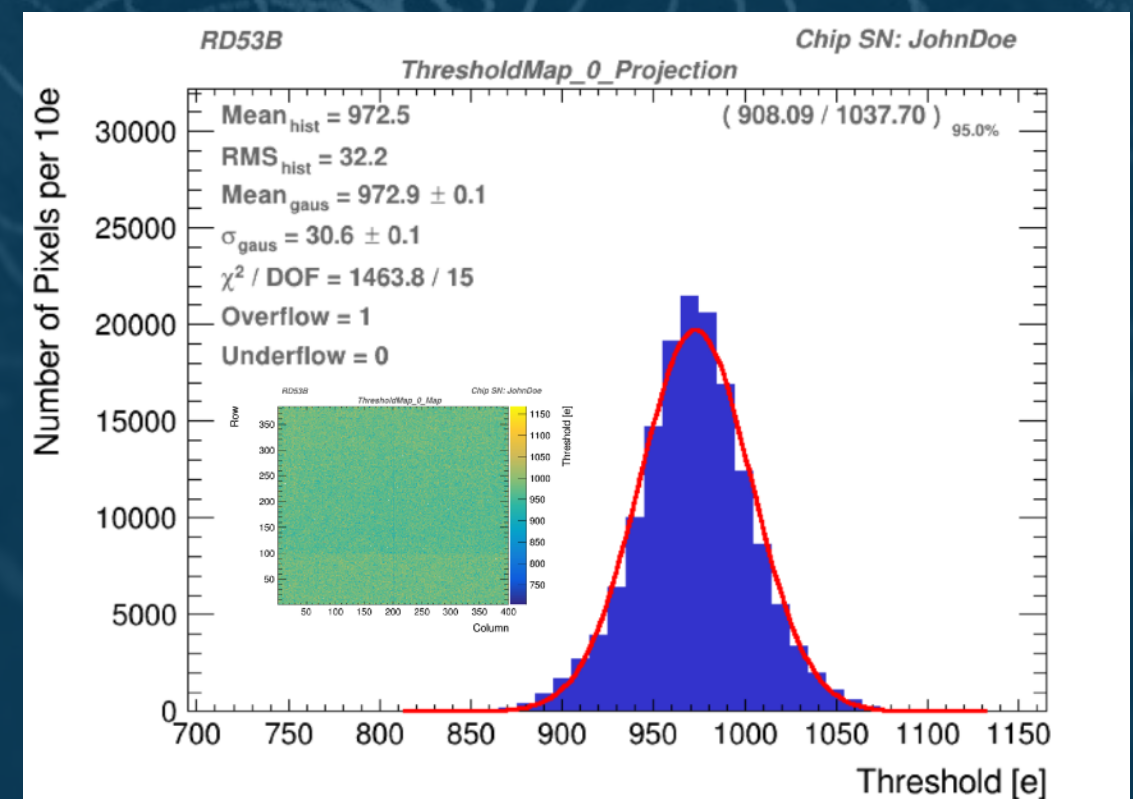
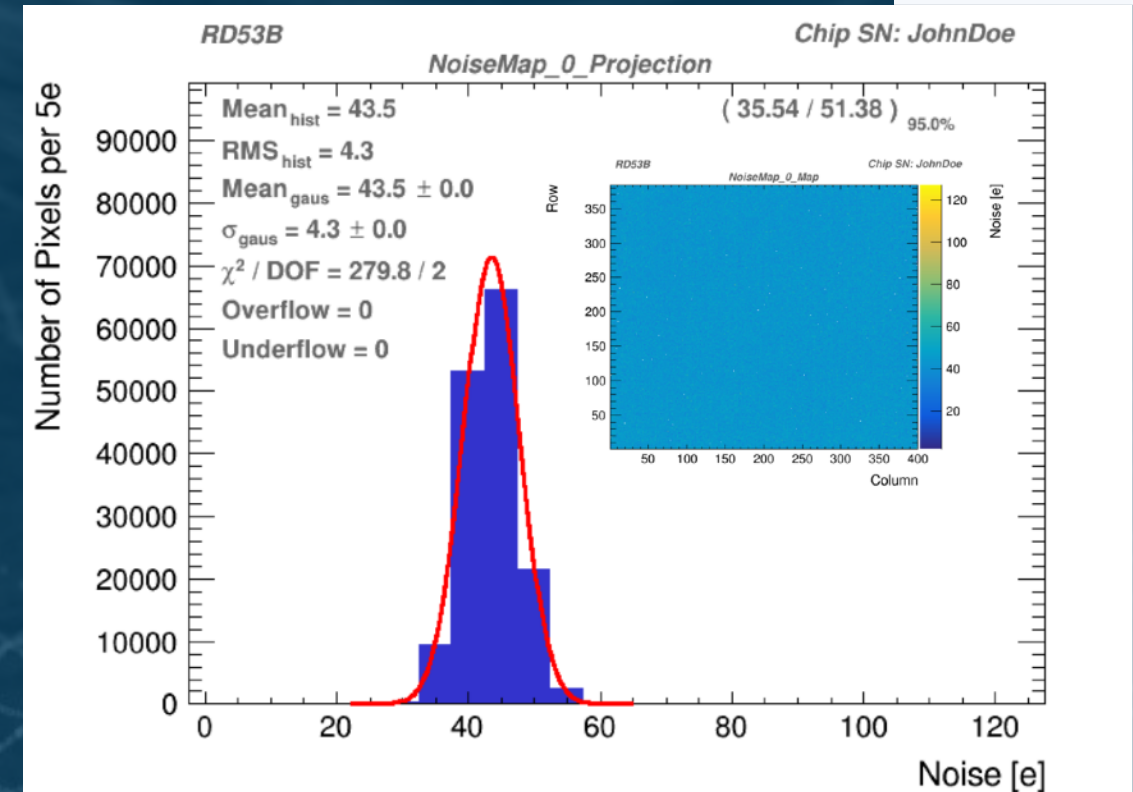
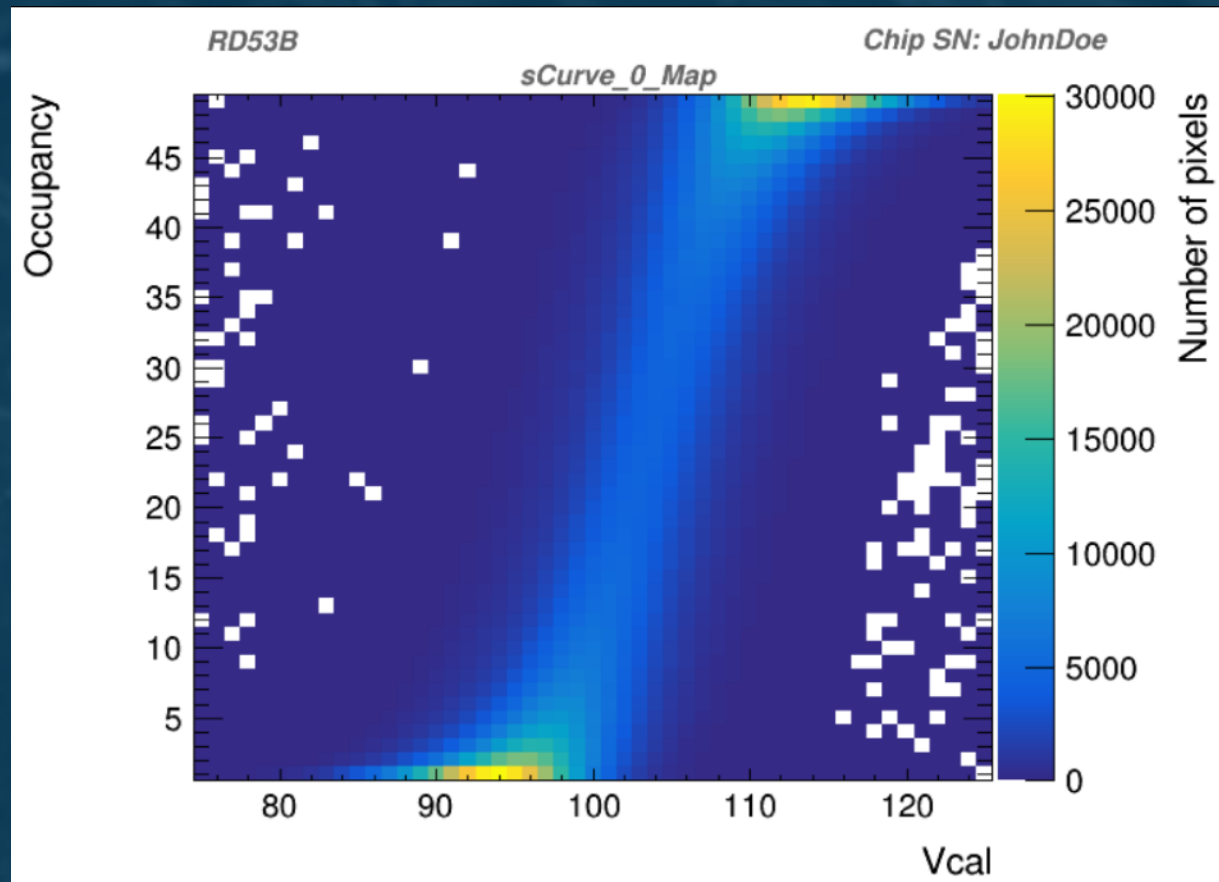


- Creative use of PToT and PToA enables direct look at second stage amplifier output
 - In the past only possible via debug pads directly wired into the analog front-end
- Will be used to make precision measurements of analog front-end

Threshold Tuning

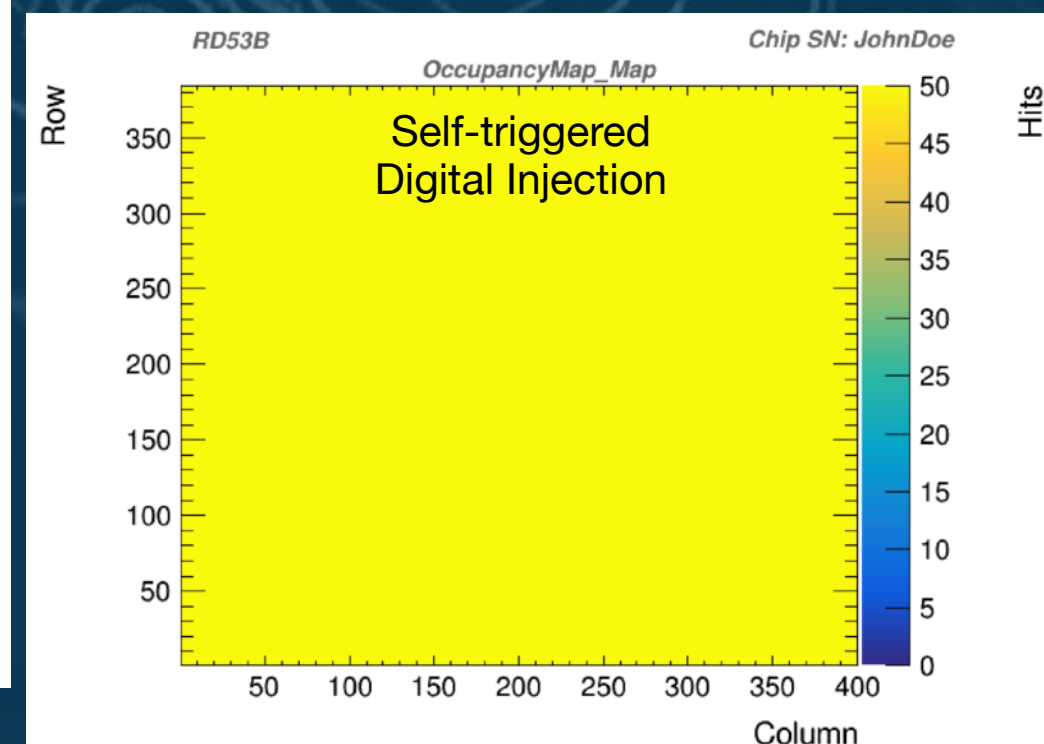
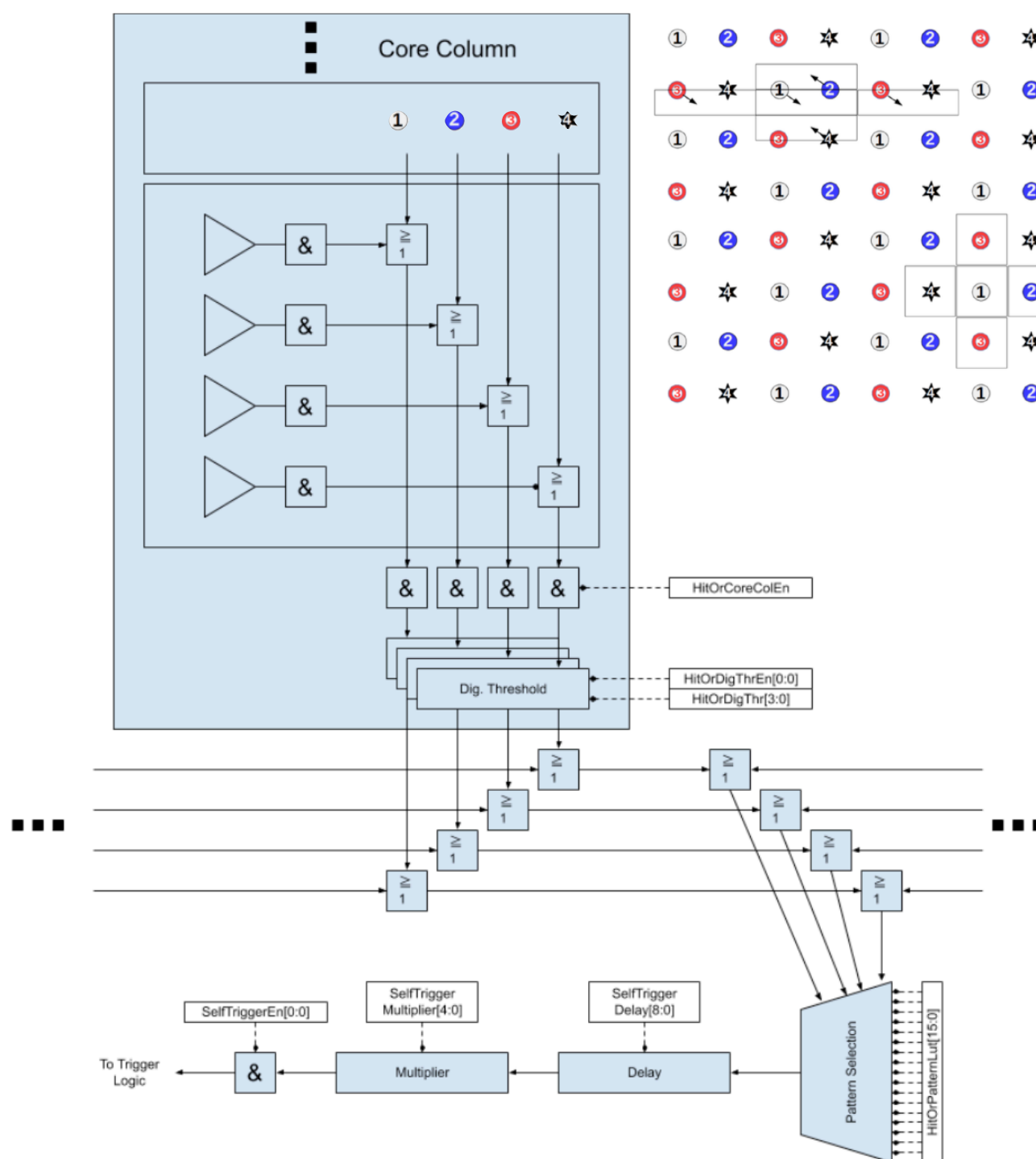


Threshold/Noise Results



- Innermost layer settings (5.5uA analog per pixel)
- First results from tuning very promising
 - Very low noise (no sensor capacitance)
 - Good tuned threshold dispersion
 - Very homogenous maps
- Next: explore more analog front-end working points and measure performance with sensor

- Uses HitOr bus to **register pixel hits and issue trigger to itself**
- Will be primarily used for source scans
- Tested with digital injection and **working as expected**
- Has additional functionality (using the 4 different HitOr busses) to trigger on specific cluster patterns



Probe Card:

- First version designed and produced
- Interface mimics Single Chip Card and integrates readily with test system
- Very large number of needles and very dense (200 needles over 2cm)
- Wafer probing system currently being commissioned
 - Will supply probed wafers for module flip chipping in coming months



Summary and Conclusion

- ITk Pixel pre-production chip **ITkPixV1** was submitted in March 2020 by the **RD53 Collaboration**
- Wafers were delivered in June 2020 and upon first power-on we discovered an **abnormally large digital current**
 - Traced digital current back to **bug in ToT memory**, which also leads to hit loss
- Bug **prevents ITkPixV1** to be used for some important system testing
- **Developed a patch** only changing two mask layers, to be submitted **ITkPixV1.1** which will be used for pre-production and majority of testing
- **ITkPixV1 testing progressing well** and everything working well so far
- Big next steps in testing:
 - Analog front-end characterization, Xray irradiations, Sensors assemblies, system testing
- Conclude chip verification in time for ITkPixV2 submission (ITk Pixel detector production chip)

Backup

Collaboration board chair:
Lino Demaria, Torino

Interface to experiments: Co-spokespersons

Jorgen Christiansen, CERN (CMS) , Maurice Garcia-Sciveres, LBNL (ATLAS)

- General organization, Funding, Specifications,

Experiment observers

Duccio Abbaneo, CERN (CMS) , Kevin Einsweiler, LBNL (ATLAS)

RD53 design framework for final pixel chips: Flavio Loddo, Bari; Deputy: Tomasz Hemperek, Bonn

Floorplan/integration:
Flavio Loddo, Bari

- Pixel array, Bump pad, EOC, Power distribution, Bias distribution, Analog/digital isolation, Integration, Verification

Analog FEs with biasing:
Luigi Gaioni, Bergamo;

- Ennio Monteil, Torino;
Amanda Krieger, LBNL
- Specification/performance, Interface, Analog isolation, simulation model, Abstract, Integration, Verification

Monitoring:

Mohsine Menouni, CPPM;
Gianluca Traversi, Bergamo,
IP designers

- Specification/performance, Interface, Analog isolation, simulation model, Abstract, Integration, Verification

PAD frame: Hans Krueger, Bonn

CDR/PLL: Piotr Rymaszewski, Bonn
High speed drv: Konstantinos Moustakas, Tianyang Wang, Bonn
Diff. IO: Gianluca Traversi, Bergamo

Digital integration:

Tomasz Hemperek, Bonn; Luca Pacher, Torino

• **Simulation Framework:**

- Sara Marconi, CERN;
- Framework, Hit generation/ import MC, Reference model / score board, Monitoring/verification tools, Readout rate estimations, Behavioural pixel chip, SEU injection.

• **Pixel array logic:**

- Sara Marconi, CERN
- FE interface, Latency buffer, Core/column bus

• **Digital chip bottom:**

- Roberto Beccherle, Pisa; Francesco Crescioli, LPNHE;**
- Configuration, Control interface, Readout data format/protocol, Compression

• **Verification:**

- Sara Marconi, CERN; Attiq Rehman, Bergen,**
Joel De Witt, Santa Cruz
Cesar Gonzales Renteria, LBNL
Peilian Liu, LBNL
SEU: Pedro Leitao, CERN; Rafael Girona, Sevilla
SET: Fernando Munoz Chavero, Sevilla
LPGBT: Pedro Leitao, CERN
Mixed signal: Luca Pacher, Torino;
Aikaterini Papadopoulou, LBNL
- Functional, SEU, Interfaces, specifications

• **Library cells:**

- DICE: Denis Fougeron, Mohsine Menouni, CPPM
Timing characterization : Sandeep Miryala, FNL

Serial Power:

SLDO: Michael Karagounis,
Andreas Stiller, Dortmund.
Bandgap: Gianluca Traversi,

Verification: Alvaro Pradas, ITAINNOVA;
Stella Orfanelli, CERN; Dominik Koukola, CERN

- Shunt-LDO integration, On-chip power distribution, Optimization for serial powering, System level power aspects, Power Verification

Design for testability:

Giuseppe De Robertis, Bari

- Scan path, BIST, production test patterns, Fault simulation, bump bonding testing

IPs: Support and possible updates

Current DAC: Bari
Voltage DAC: Prague
ADC, mux, temp: CPPM
Power on reset: Seville
Ring oscillator: LAL
Analog buffer: RAL

Support and services:

Tools, design kit: Wojciech Bialas, CERN
Repositories: Flavio Loddo, Bari; Luca Pacher, Torino; Tomasz Hemperek, Bonn
Radiation model: Mohsine Menouni, CPPM; CERN

Testing: Timon Heim, LBNL

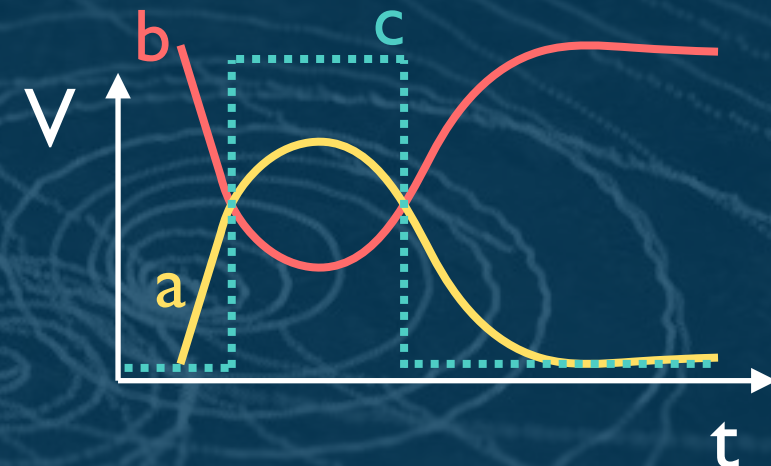
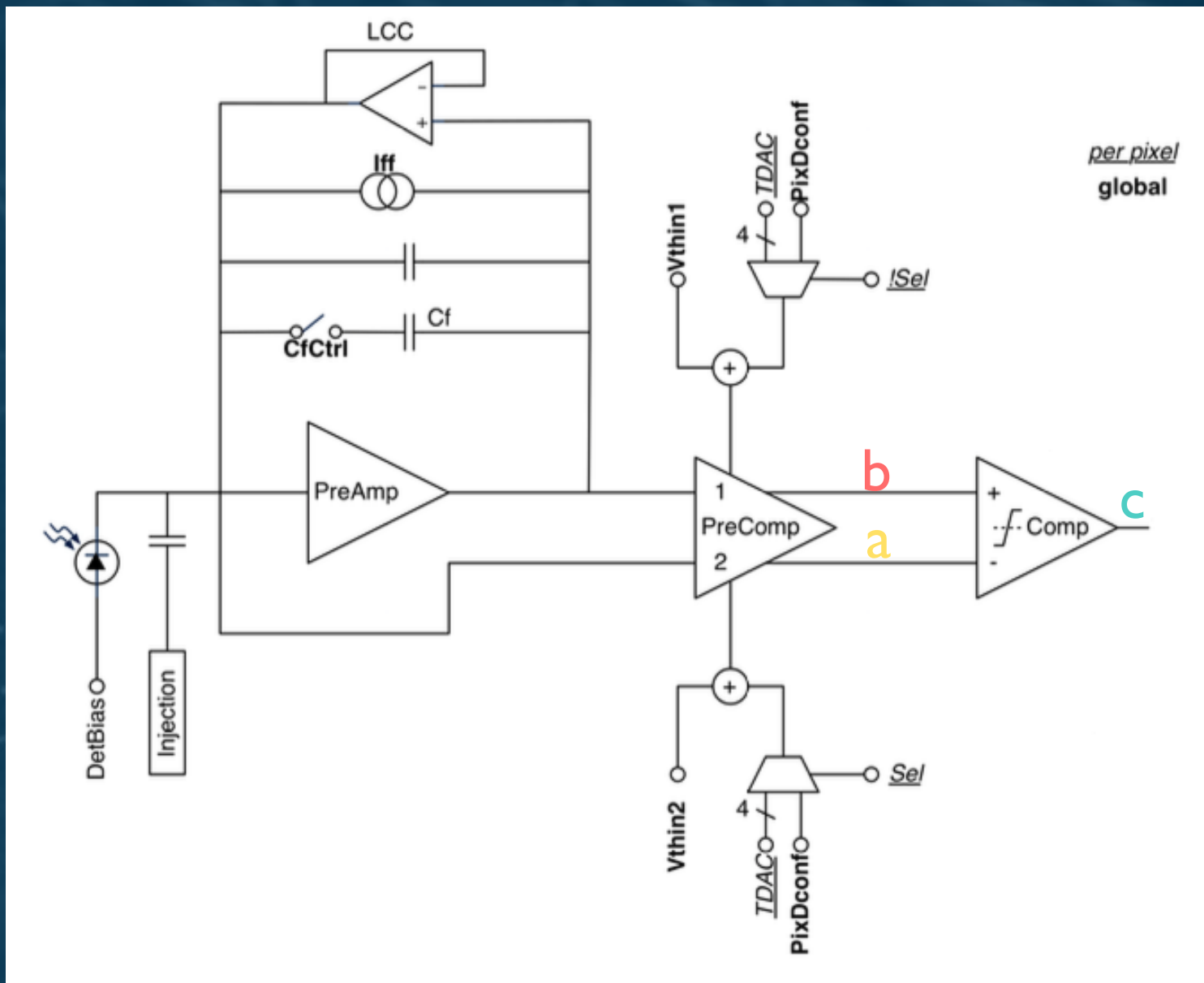
YARR system: Timon Heim, LBNL
BDAQ53 system: Marco Vogt, Michael Daas, Yannik Dieter, Hans Krueger, Tomasz Hemperek, Mark Standtke Bonn
Radiation test: Luis Miguel Jara Casas, CERN, Mohsine Menouni, CPPM.
Plus many ATLAS/CMS groups not formally part of RD53

Pixel sensor and bump-bonding:

Fabian Huegging, Bonn (ATLAS),
Georg Steinbrueck, Hamburg (CMS)

Names in bold: Member of RD53 management board

Differential Front-End

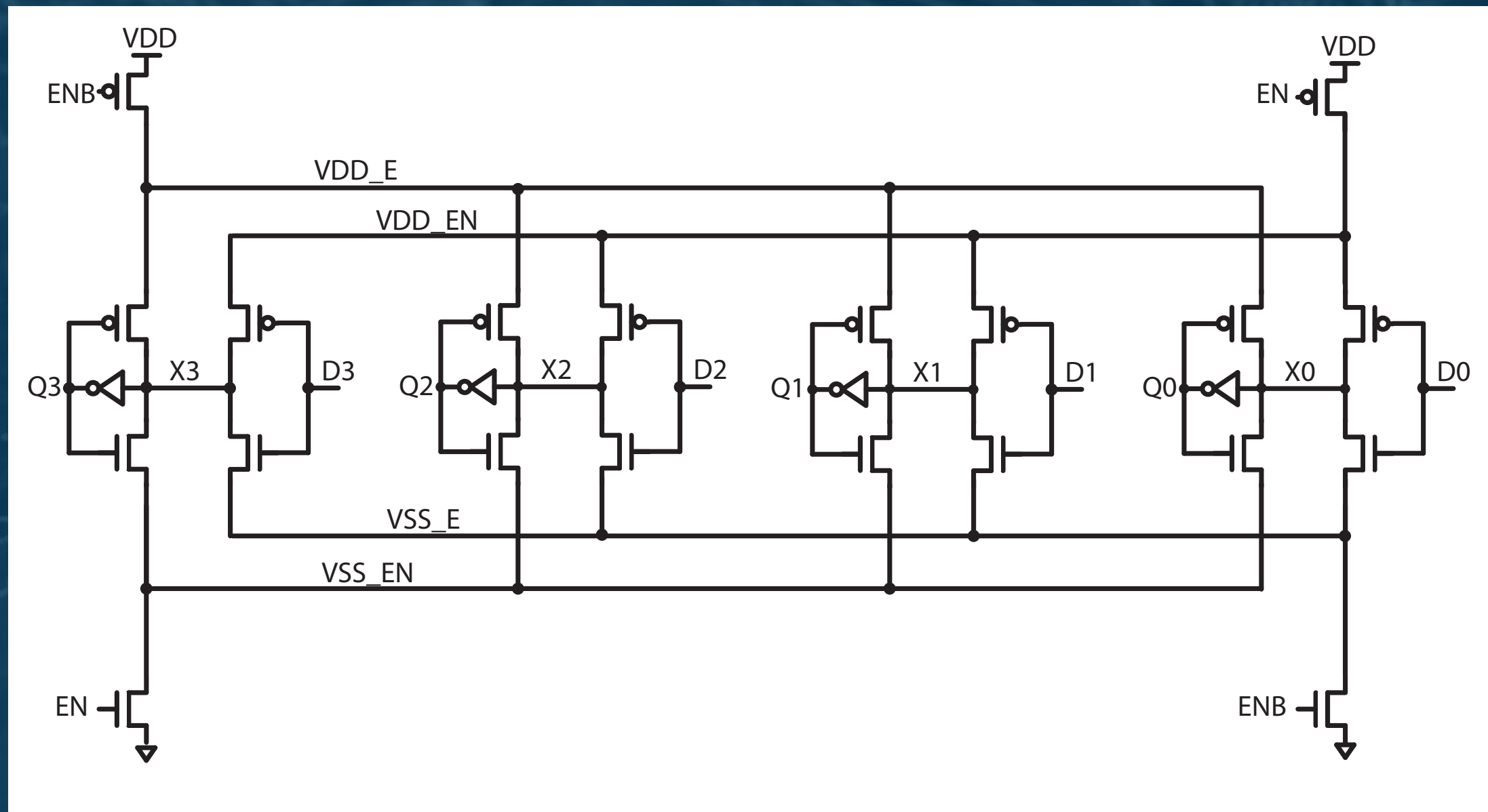


Charge Sensitive Amplifier:

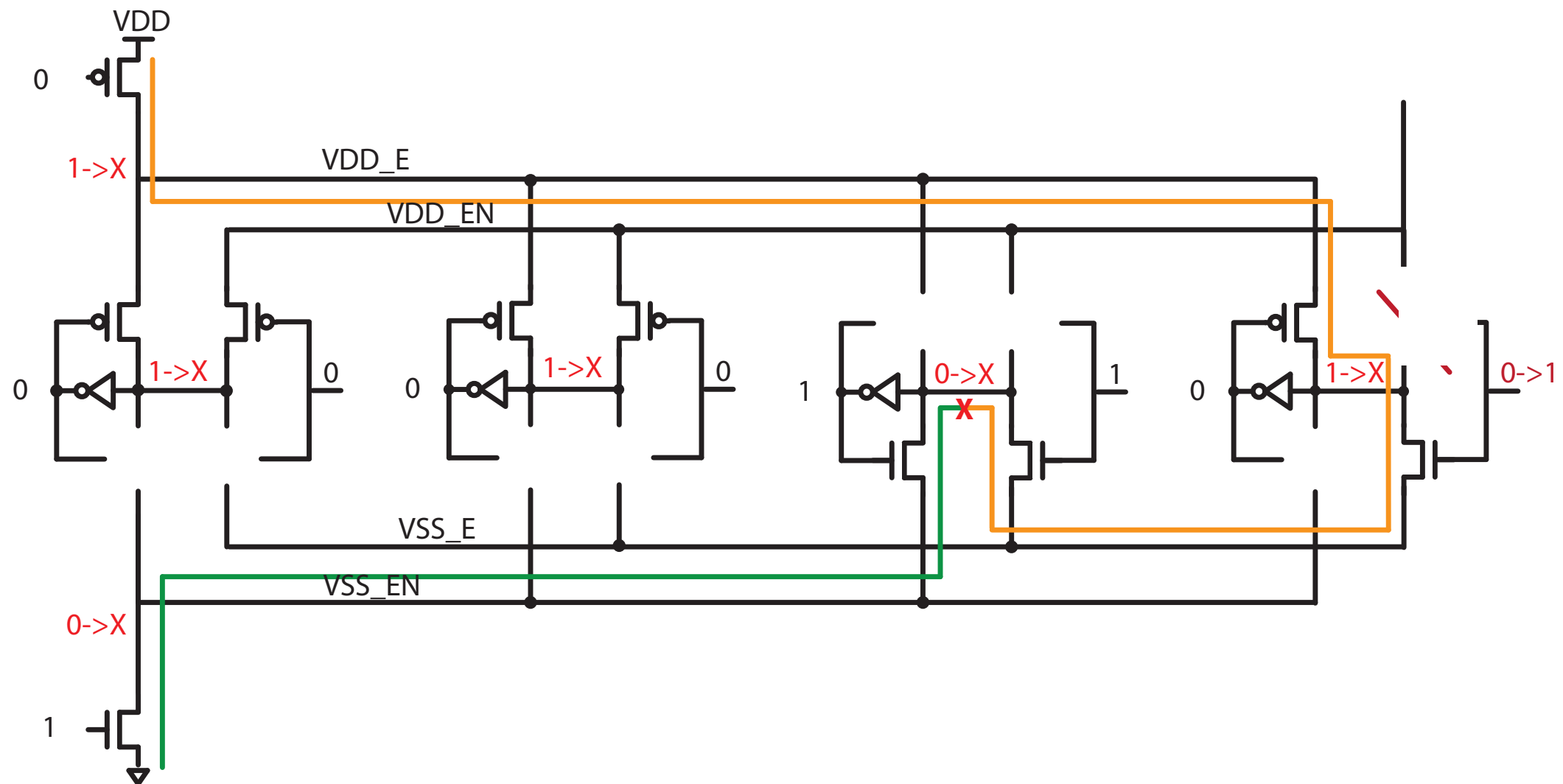
- Straight cascode design
- Global settings for I_f (8bit DAC)
- No per pixel adjustment
- Selectable gain

Two Stage Comparator:

- Differential design
- Global 8bit threshold DAC
- Two per pixel 4bit threshold DACs
- Optimised for low threshold operation



EN=1, D=0010->0011



How did the Bug make it into the Final Design?

- Multi-bit latch was designed during RD53A design stage as a potential alternative to single-bit latches to improve routing congestion (multi-bit latch is 50% smaller)
- It was **not used for RD53A** yet it remained in the design library
- Designer of latch left RD53 collaboration after submitting the design and it was assumed that the design was finished and fully verified (it was not)
- The latch was then used in RD53B to reduce congestion in digital core
- The **specialized commercial tool** used to build the electrical model, extracting timing, power, and signal integrity values from the physics design of digital cells **did not detect that the multi-bit latch had pattern dependent issues**
- A more recent version of the same tool now reports a problem

Working around the Bug

- ToT memories do not have a reset (it would be an SEU vulnerability) and are in a random state after power-on, hence most are in a state where they allow current to flow from VDDD to GND
- The current path can be broken by setting ToT memories to '0000'
- Can be achieved by quickly injecting a very short digital pulse very frequently to overwrite all memories

After setting all ToT memories to '0000' we see the **expected digital current of 600mA** (with all cores enabled). This allows testing all features without influence from current!

(Analog current is as expected, 700mA after configuration)

