Smart Three-Dimensional (3D) Chip Stacking Process for Detectors using High Energy Physics Experiments

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1. Introduction
   Necessity of 3D Technology for Vertex Detector

2. Proposed 3D Process
   Au μ-Bump for 2 chip connection
   TBV for top side interconnect
   Proposed 3D process flow

3. 3D process verification by detector evaluation results / β-ray tracking observation

4. Summary
**Requirements for Detector**

“**Simultaneous detection** of hundreds of particle tracks with **micrometer spatial** and **nanosecond timing** precision in **harsh radiation environment** close to the point of their production.”


- **Spatial Resolution**: around few micrometer ⇒ few ten μm in pixel size
- **Timing Resolution**: around few nanosecond ⇒ precise hit timer in pixel
- **Track detection**: multiple hit position memory
- **Low material budget**: thinner detector as 50-100 μm, less bump metal
- **Radiation hardness**: up to around MGy

Complex circuit in reasonable small pixel

with low material budget and high radiation tolerance.

To fulfil the requirements, **circuits stacking on sensor** is one way.
Monolithic detector using silicon-on-insulator (SOI) technology. Detector chip (handle Si) is electrically connected to readout circuit (SOI layer) by small via fabricated by a conventional LSI process.

**Advantages of SOI Monolithic Detector**
- Commercial CMOS process to fabricate SOI detector
- Extremely Low material budget (can thin down to 50 µm)
- Easy to embed circuits in pixel
- Low parasitic capacitance
Using SOI pixel sensor technology, around 10 µm pixel size was achieved with embedding an analog amplifier in pixel.

For the vertex detector, multiple hit locations, timing, (and analog signals) must be detected. This requires additional circuits in a pixel.

From consideration of circuit layout for these functions, the pixel size must exceed 30 µm and difficult to fulfil the required spatial resolution.

Need chip stacking (3D) technology with an SOI pixel detector chip!!
Existing 3D Technology

Well known 3D stacking method for imager

**SONY**: developed for backside illumination
Already in mass production and well mature process

- Cu-Cu bonding (Fusion Bonding) and TSV
  - very smooth surface and Cu bonding pad
  - dedicated equipment for TSV

3D Process for Quantum Beam Imager

**Fermi Lab. Group**
Tezzaron 3D process
- Cu-Cu and Ni-Ni bonding
- TSV

**EU Group / AIDA WP3 Project**
Fraunhofer SLID
- Cu-Sn SLID bonding
- TSV

Need very smooth surface.
Additional processes for 3D are required.

G. W. Deptuch et al., IEEE Trans. ED 63(1)


Y. Kagawa et al., Tech Digest of IEDM 2016, pp. 208-211
Consideration of R/O Chip Performance and Cost

Future prospects for readout chip
- High Speed Operation
- More Complex Logic Circuit

Solution: Readout chip fabricated by an advanced process technology such as 65 nm or below.
- Expensive mask set
- Expensive run cost

Actually ...
Limited Budget
Limited # of required chips

Shuttle Service !!

Requirements for 3D process
- Chip form: CoC or CoW
- No additional wafer process for 3D

CoC: chip on chip, CoW: Chip on Wafer
Candidates for Au μ-Bump

Stable Process
- large bonding Margin
  - deformation bump has larger margin than pillar bump

low temperature process
- less than 200°C

no extrusion
- Au has no extrusion

Good in scalability
- Bump size must be limited by lithography

Select two candidates for μ-bump

Au Cone Shape μ-Bump
Au Cylinder Shape μ-Bump
Process Flow of Au Cone Shape Bump

Key Technology: Au nano-particle deposition
Characteristics of Au Cone Shape Bump

Au Cone Shape Bump

Cross section of junction

Bump Resistance

Daisy chain resistance (Ω)

# of bump connection

Sample #1
Sample #2
~0.25 Ω/bump
Process Flow of Au Cylinder Shape Bump

Key Technology: inverse-tapered photoresist & low incident-angle sputtering

Bump Hole Patterning

Low incident angled Au Sputtering

Resist Lift-off
Characteristics of Au Cylinder Shape Bump

Au Cylinder Shape Bump

Cross section of junction

Bump Resistance

- Chip #1: 153.9 Ω, 0.38 Ω
- Chip #2: 167.8 Ω, 0.41 Ω
- Chip #3: 133.9 Ω, 0.33 Ω

*R_bump: include parasitic resistance of interconnect
### Summary of Au μ-Bump

<table>
<thead>
<tr>
<th>Item</th>
<th>Au Cone Shape Bump</th>
<th>Au Cylinder Shape Bump</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bump Resistance</td>
<td>~ 0.25 Ω/bump</td>
<td>~ 0.37 Ω/bump</td>
</tr>
<tr>
<td>Bump Yield</td>
<td>&gt; 97%</td>
<td>&gt;99.5%</td>
</tr>
<tr>
<td>Reliability</td>
<td>Qualified for Thermal Cycle Test</td>
<td>Qualified for Thermal Cycle Test</td>
</tr>
<tr>
<td>Mechanical Damage by Bump Bonding</td>
<td>normal</td>
<td>low</td>
</tr>
<tr>
<td>Productivity</td>
<td>OK</td>
<td>OK</td>
</tr>
<tr>
<td>Au deposition Through-put</td>
<td>too low</td>
<td>normal</td>
</tr>
</tbody>
</table>

**Au Cylinder Shape Bump** was used in the first 3D trial run for quantum beam imager.
Top Side Electrode Formation

Need to make electrical connection from metal wiring of upper chip to top side.

"Via" already exists in front-end process and can be used as "via" to top side when handle Si of upper chip is etched-off.

TBV (Through BOX Via)

Via size : 0.3 um

Concerning

(1) affect MOST characteristics
(2) contact resistance of TBV

Too much process steps !!
Need extra equipment !!
Concerns for Upper Chip

Because of supporting Si removal of upper chip, transistor characteristics change around the bump is the most concerning issue.
Results of MOSFET Characteristics
Proposed 3D Process Flow

(a) after Via 5 formation [receiving chip for 3D process]
(b) under bump metal deposition & patterning
(c) Au bump formation
(d) lower & upper chip alignment

(e) bump bonding & adhesion glue injection
(f) upper Si removal [expose through BOX via]
(g) upper metal deposition & patterning [bonding pad & backside gate]
(h) passivation deposition & patterning
Pixel Circuit of Vertex Detector (SOFIST)
First Trial Run of Imager

(a) after Via 5 formation [receiving chip for 3D process]
(b) under bump metal deposition & patterning
(c) Au bump formation
(d) lower & upper chip alignment

1 Pixel

30.0um

(c) bump bonding & adhesion glue injection
(f) upper Si removal [expose through BOX via]
(g) upper metal deposition & patterning [bonding pad & backside gate]
(h) passivation deposition & patterning
Patterns of lower chip can be seen through upper chip because handle Si in upper chip was removed.

Green patterns in the peripheral are backside of SOI layer of upper chip.

Bonding pads on upper chip are also shown.
β-ray Track Observation and Bump Yield

50K event accumulation

102 × 102 pixels

Source: $^{90}\text{Sr}$

# of failure pixels: 4 of $102 \times 102$

$$1 - \frac{4}{102 \times 102} \sim 99.96\%$$
Radiation Hardness Test for Adhesion Glue

Proton irradiation: 400 kGy
(5 × 10^{14} cm^{-2} in 1 MeV neutron equivalent)

**Upper Chip Peeling Portion**

**Before irradiation**

**After irradiation**

No obvious damage was observed !!
even though the dose level is threshold to create Si displacement defects.

Test chip for process condition tuning is used for evaluation. The chip has damages but still good area and is enough to evaluate glue damage.
• An SOI chip base 3D chip stacking process has been proposed.
• Major technologies of the process are Au μ-bump to connect front sides of two chips, and through BOX via to connect bonding pads instead of generally used through silicon via.
• From feasibility study of Au μ-bump technology, Au cylinder shape bump was selected because of Au deposition throughput and less mechanical damage.
• Using this 3D technology, prototype detector was manufactured and images of β-ray track from $^{90}$Sr are successfully demonstrated.
• High pixel yield as over 99% is also confirmed.
Thank you for kind attention.