MuPix10: First Results from the Final Design

Heiko Augustin on behalf of the Mu3e pixel team
Physikalisches Institut Heidelberg

Vertex2020
07.10.2020
Mu3e

- Search for the cLFV decay $\mu^+ \rightarrow e^+e^-e^+$
  ($\nu_{SM}$: BR $< 10^{-54}$)
- Current limit (SINDRUM)
  BR $< 10^{-12}$ @ 90% CL
- Sensitivity goal:
  1 in $10^{16}$ decays
- Up to $10^9$ decays per second
- Suppress background below sensitivity level

Backgrounds
- Internal Conversion
- Accidental
The Mu3e Detector

- 1 Tesla Magnetic field
- Helium Atmosphere

- Good vertex and time resolution (100 μm & 500 ps)
- Good momentum resolution (0.5 MeV)
- Continuous Beam! No trigger!
- Online reconstruction and selection

- $10^8$-$10^9$ decays per second
- $p_{\text{max}} = \frac{m_\mu}{2} = 53$ MeV
  - Multiple Coulomb Scattering

07.10.2020

MuPix10
The Mu3e Detector

Pixel detector requirements:

<table>
<thead>
<tr>
<th>Pixel Size</th>
<th>Time Resolution</th>
<th>Material Budget</th>
<th>Efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>80 x 80 μm²</td>
<td>&lt; 20 ns</td>
<td>0.1% X₀/layer</td>
<td>&gt; 99 %</td>
</tr>
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</table>

Mu3e TDR [arXiv:2009.11690]

- $10^8$-$10^9$ decays per second
- $p_{\text{max}} = m_\mu / 2 = 53$ MeV
  - Multiple Coulomb Scattering
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- Continuous Beam! No trigger!
  - Online reconstruction and selection
High Voltage - Monolithic Active Pixel Sensors

- In-pixel electronics
- Monolithic design: Detection and Readout combined in one chip
- Commercially available processes: AMS 180nm (6M) TSI 180nm (7M)
- Chips are thinned to 50 μm

- Low ohmic substrates (10-200 Ωcm)
- High voltage > 100V
- Deep N-well diode
- ~ 30 μm depletion
- Charge collection via drift
MuPix History

- Small prototype development culminates in MuPix7
- Scaling successful with MuPix8
- Foundry change necessary after MuPix9
- New foundry TSI with same base process (IBM 180nm)
- Large scale prototype MuPix10 and ATLASPix3 successfully produced with TSI

ARXIV:2002.07253
MuPix Architecture

- Clear separation of analog and digital electronics
- 2 comparator design
- Tuning and masking available
- Priority encoder / column-drain readout
- Chip sub-dived into 3 matrices → 1 Data link each + 1 multiplexed link
The MuPix Principle

- Deposited charge amplified by in-pixel amplifier
- Source follower drives the signal to the periphery
- Digitisation in periphery
- Timestamp sampling
- Readout statemachine manages column-drain readout
- Data is send out via a 1.25 Gbit/s differential link
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Latest Results - MuPix8

Raw time resolution

- Delay correction: 14 ns
- Timewalk correction: 6.5 ns

[arXiv:1905.09309]
A MuPix Module

- Chips glued and SpTAB-bonded to flexprint
- No additional components!
  - $1.15\% X_0$ per layer
- Minimize dead space between the chips
  - Only $11\,\mu m$ dead silicon outside the guardring
- Power consumption limited to 400 mW/cm² (Sensors+Flex)
The Flexprint Environment

- 2 layer aluminum polyimide flexprint (LTU)
- Provides:
  - Power & HV
  - Differential Signal I/O
- Only 1 supply voltage, but no LDO-regulators!
  - Minimise I/O
- Flex design rules define PadOut
MuPix10 Design

- Module ready!
  - Pad Out compatible with flex
  - Chip size defined by mechanics
- Complete on-chip biasing:
  - triple redundant memory
  - bias and voltage DACs
- 1.2V voltage regulator
  - MuPix10 can be used for Module production
The MuPix10

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel size [µm²]</td>
<td>80 x 80</td>
</tr>
<tr>
<td>Sensor size [mm²]</td>
<td>20.66 x 23.18</td>
</tr>
<tr>
<td>Active size [mm²]</td>
<td>20.48 x 20.0</td>
</tr>
<tr>
<td>Pixel matrix</td>
<td>256 x 250</td>
</tr>
<tr>
<td>Thickness [µm]</td>
<td>50</td>
</tr>
<tr>
<td>Substrate [Ωcm]</td>
<td>200-400</td>
</tr>
<tr>
<td>Data links</td>
<td>3+1</td>
</tr>
<tr>
<td>Data speed [Gbit/s]</td>
<td>1.25</td>
</tr>
<tr>
<td>Time-of-arrival [bits]</td>
<td>11</td>
</tr>
<tr>
<td>ToT [bits]</td>
<td>5</td>
</tr>
<tr>
<td>TS binning [ns]</td>
<td>8 (option for 1.6)</td>
</tr>
</tbody>
</table>
MuPix10 timeline

- December 2019: Submission to TSI
- March 2020: Wafer delivery
  Send for post-processing
- March → May 2020: Lock down in France and Germany
- Mid of May 2020: Receive first chips
In-house Picking

- Diced Wafers delivered on tape (Company OPTIM)
- Equipment:
  - Vaccum chuck
  - Vaccum pick-up tool
  - Patience
- 3 thicknesses: 625, 100 and 50 um
- Picking yield very high: >98%
- Effect on “electrical yield”? • detailed study with probe card is pending
Commissioning & First results

- In the Lab:
  Commissioning and Optimisation with Injection or Sr90 and Fe55
  - Breakdown @ -100V
    → 30-40um depletion

- Testbeam:
  DESY 3 GeV e-
  PSI 350 MeV π+,μ+,e+(,p+)
  → MuPix10 works nicely

Hitmap DESY testbeam
MuPix Telescope

- Co-Development of the DAQ
- Most common setup:
  4 sensor layer (1 DUT)
  coincidence of scintillating tiles
- Evolution of reference plains:
  Mupix6, MuPix7, MuPix8, ATLASPix1,
  ATLASPix3 and now MuPix10
- MuPix10 telescope used!
Tuning & Masking

- Usage of the individual tuning and masking bits
- S-curve based tuning approach
- Data:
  Injection of ~3000 e- (fixed)
  Threshold scanned
- Threshold dispersion:
  Untuned RMS ~240 e-
  Tuned RMS ~75 e-
Tuning & Masking

- Usage of the individual tuning and masking bits
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  Injection of ~3000 e⁻ (fixed)
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  Tuned RMS ~ 75 e⁻
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  - Tuned RMS ~75 e–
Tuning & Masking

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- Data:
  Injection of ~3000 e⁻ (fixed)
  Threshold scanned
- Threshold dispersion:
  Untuned RMS ~240 e⁻
  Tuned RMS ~ 75 e⁻
- Masking works nicely too
Vssa-Regulator

- Integral for module functionality with a single supply voltage
- No detailed study yet
- Dive into the cold water: the regulator works nicely
- Even colder water: MuPix10 was operated successfully with a single supply voltage
  - Power consumption: ~ 220mW/cm²
ToT sampling

- ToT correction desired for offline data analysis
- Not foreseen on MuPix8
  → possible readout problem
  → ToT not fully sampled
- Easy Solution:
  Wait for the pulse to end
  → scrambles the chronology of the data
- Additional complexity for the online sorting
- Better:
  delay every hit by a constant time
  → Chronology conserved
Delay Circuit

- Analogue Delay
  Designed by Alena Weber (KIT)
- Contained in each digital pixel cell
- Delay programmable
- Delay measurable as maximum ToT
- Further idea: Hits with large ToTs do not gain from ToT correction
  → Limit the maximum ToT
  → More precision for low energy depositions
  → Works nicely!!
Signal Line Crosstalk - MuPix8

- Point-to-point connection
- Capacitive coupling to neighbouring lines (increases with length)
- Crosstalk can induce additional hits
  - Not easily distinguishable from charge sharing
  - Additional Readout load
Signal Line Crosstalk - MuPix8

Triple Crosstalk:
hit induced in both neighbouring lines
Crosstalk Extrapolation for MuPix10

- Using the same routing density and scheme
  - Almost 48% crosstalk probability for the longest line
  - Penalty for high row addresses
  - Routing needs to adapt

Triple Crosstalk probability
Routing Optimisation - MuPix10

- Equalize but reduce crosstalk → minimize the length that two lines are neighbouring (¼ of total length possible)
  → ~12% triple crosstalk expected
- Make Crosstalk easily detectable → neighbouring signal lines are not neighbouring pixels
Routing Optimisation - MuPix10

- Equalize but reduce crosstalk → minimise the length that two line are neighbouring (¼ of total length, 2cm)
  - ~12% triple crosstalk expected
- Make Crosstalk easily detectable → neighbouring signal lines are not neighbouring pixels
  - Crosstalk can be removed, possibly already during the data taking
- Even more improvement expected for MuPix11
Summary

- MuPix10 is working nicely!
  - Full-scale
  - Module ready
- New features implemented successfully
  - Delay circuit, routing
- Final Submission: MuPix11 Summer 2021
Mu3e Status

- Mu3e Magnet arrived at PSI and is currently cooling down
- Helium cooling system and tests are nicely progressing (Silicon Heater mock-up)
- Hardware of the readout chain available and heavily tested
End of the year plans

- Long beam time @PSI
- Tests within the magnet
- All sub-systems: Pixel, Tile and Fibre
- Check of important paths of the readout chain
- First 6 chip module (not on flexprint)