Belle II and vertex detector
- The vertex detection in the Belle II experiment is essential for the time-dependent CP violation measurement.
- Currently, the Belle II vertex detector consists of:
  - inner 2-layer Si pixel detector (PXD): DEPFET sensors
  - outer 4-layer Si strip detector (SVD): DSSD sensors
- One big concern for the future operation is harsh beam background from the SuperKEKB accelerator, which can eat up the safety factors of the radiation tolerance of the detectors.
- Moreover, some SVD features can be improved for better physics performance.
  - Material budget, Position resolution in N-strips, Level-1 trigger latency

Development of front-end ASIC

**Requirements on front-end ASIC**
- Readout of binary hit information, to minimize the number of cables.
- Short pulse width < 100 ns, to avoid signal pile-up
- Small noise < 900 e- due to smaller signals from thin sensor
- Fast clock sampling, for good time resolution to separate the beam background hit

**Prototype ASIC: SNAP128A**
- SNAP128 is developed based on ‘SliT’ chips, which are for silicon tracker of J-PARC g-2 experiment.
- 180nm CMOS
- 128ch inputs / chip
- 127MHz sampling of binary hit information after discriminator
- Hit time resolution: ~7.9ns
- Contain 2k-depth memory in each channel
  - Maximum trigger latency : 15.8 μs
- Estimated total power-consumption : 363 mW / chip
- ASIC design is finalized.

**Analog part**
- CSA+PZC / CR-RC shaper / discriminator
- Bi-polar (readout for p- and n-side)
- Optimize the design to achieve a short pulse width and small noise
  - pulse width : 55 ns
  - noise : 640 e- ( @ 12pF)

**Expected noise**

**Expected height of shaper output**

Plan for the next
- The prototype DSSD sensor and SNAP128A will be produced by Mar 2021.
- Using those prototype, test modules will be assembled by the next summer to measure the detector performance.
- From the results, we will decide the final specification of the thin/fine-pitch silicon strip detector.
- Still many things to be done:
  - Detector mechanics, cooling, back-end electronics, so on...
  - The target completion time of the new detector production : in 2026

Thin/fine-pitch Si strip detector
- The vertex detector upgrade is under discussion to improve the radiation tolerance and the performance.
- In our project, we are developing new DSSD detector to upgrade SVD.
- Target hit-rate tolerance : 10 MHz/cm²
- Target detector performance:
  - smaller material budget < 0.7% X₀ / layer
  - Position resolution (θ=0) < 20 μm (TBC with MC)
  - Level-1 trigger latency > 8.0 μs
- Target radiation tolerance: TID : 10 Mrad, NIEL : 2.5 x 10¹⁵ neq/cm²
  - Concept is thin and fine-pitch DSSD for a small material budget, a high rate tolerance, and a good position resolution.

Thin/fine-pitch DSSD development
- The prototype DSSD design:
  - 140 μm thickness (c.f. current DSSD thickness is 320 μm.)
  - 50 μm (p) / 75 μm (n) pitch
  - Reduction of material budget from 320 μm to 140 μm Si : Δ = 0.19% X₀ / layer
  - Very rough estimation of position resolution : 50 μm / √12 = 14.4 μm (p-side)
  - Production company: Micron
  - Sensor mask design is completed.

**DSSD sensor design (Prototype)**

<table>
<thead>
<tr>
<th>Sensor size</th>
<th>Active area</th>
<th>Thickness</th>
<th>Substrate</th>
<th>P-side</th>
<th>N-side</th>
</tr>
</thead>
<tbody>
<tr>
<td>52.6 mm x 59.0 mm</td>
<td>51.2 mm x 57.6 mm</td>
<td>140 μm</td>
<td>N-type</td>
<td>50 μm</td>
<td>75 μm</td>
</tr>
<tr>
<td>Strip pitch</td>
<td>Strip number</td>
<td></td>
<td></td>
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<tr>
<td>1024</td>
<td>768</td>
<td></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

No floating strip. P-side and N-side are orthogonal.