Development of the thin and fine-pitch silicon strip detector aiming for the Belle II upgrade

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The composition of the current Belle II vertex detector:
- inner 2-layer Si pixel detector (PXD) : DEPFET sensors
- outer 4-layer Si strip detector (SVD) : DSSD sensors.

Concerns for future operation
- Harsh beam background from the accelerator
  - eating up the safety factors of the beam-background tolerance
- Some SVD features can be improved for better physics performance
  - material budget, position resolution of N-strip, level-1 trigger latency

The vertex detector upgrade is under discussion to improve those aspects.
In our project, thin and fine-pitch DSSD is being developed as an upgrade of the outer Si strip detector
  • a small material budget, a high rate tolerance, and a good position resolution
The prototype DSSD design:
- **140 um thickness** (c.f. current DSSD thickness is 320 um)
- **50 um (p) / 75 um (n) pitch**

Reduction of material budget by the thinner thickness (320um → 140um):
\[ \Delta = 0.19\% \text{ } X_0 / \text{layer} \]

Very rough estimation of position resolution:
50 \( \mu m / \sqrt{12} = 14.4 \mu m \) (p-side)

Sensor mask design has been completed.
Production company : Micron

### DSSD sensor design (Prototype)

<table>
<thead>
<tr>
<th>Sensor dimension</th>
<th>52.6 mm x 59.0 mm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active area</td>
<td>51.2 mm x 57.6 mm</td>
</tr>
<tr>
<td>Thickness</td>
<td>140 ( \mu m )</td>
</tr>
<tr>
<td>Substrate</td>
<td>N-type</td>
</tr>
<tr>
<td>Strip pitch</td>
<td>50 ( \mu m )</td>
</tr>
<tr>
<td>Strip number</td>
<td>1024</td>
</tr>
<tr>
<td><strong>p-side</strong></td>
<td></td>
</tr>
<tr>
<td><strong>n-side</strong></td>
<td></td>
</tr>
<tr>
<td>Strip number</td>
<td>75 ( \mu m )</td>
</tr>
<tr>
<td></td>
<td>768</td>
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</tbody>
</table>
Prototype ASIC : SNAP128A

- SNAP128A is developed based on ‘SliT’ chips, which are developed for Si tracker of J-PARC g-2 experiment.
  - 180nm CMOS
  - 128ch inputs / chip
  - 127MHz sampling of binary hit information after discriminator
    - Hit time resolution : ~ 7.9ns
  - Contain 2k-depth memory in each channel
    - Maximum trigger latency : 15.8 us
  - Estimated total power-consumption : 363 mW /chip

- ASIC design has been finalized.
The design optimized to achieve a short pulse width and small noise
– important because of the high hit rate and the small signal charge due to the thin sensor

- Pulse width : 55 ns
- Noise : 640 e⁻ @ C_{det} = 12pF
The prototype DSSD sensor and SNAP128A will be produced by Mar 2021.

Using those prototype, test modules will be assembled by the next summer to measure the detector performance.

– From the results, we will decide the final specification of the thin/fine-pitch silicon strip detector.

On the other hand, still many things to be done:

– Detector mechanics, cooling, back-end electronics, so on

The target completion time of the new detector production: in 2026