Production, calibration and performance of the layer 1 replacement modules for the CMS pixel detector

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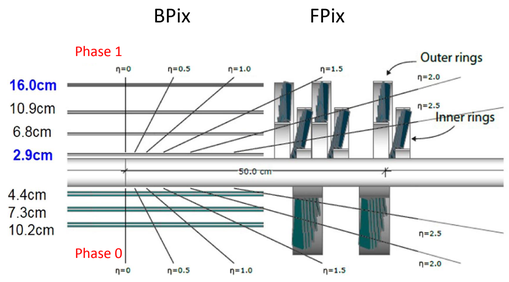
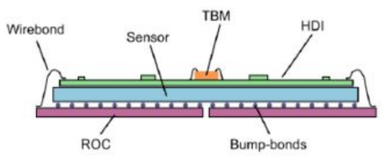
Introduction and motivation

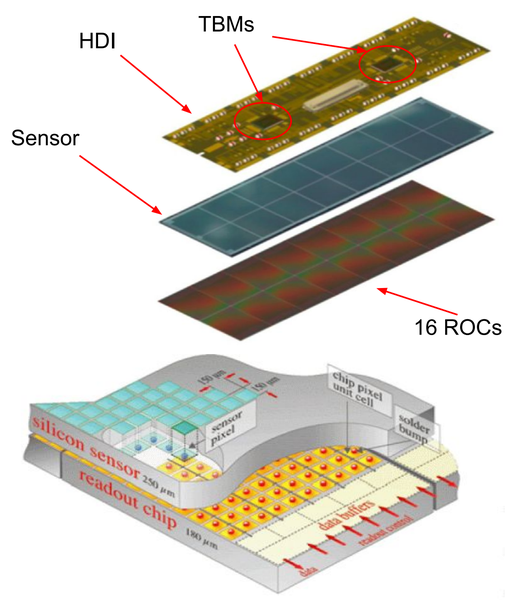
- Current Phase-1 upgraded pixel detector installed during EYETS 2016/2017
- Due to radiation damage, the innermost layer (L1) of the pixel barrel detector (BPix) would have to be replaced during Run 3 **[1]**
- L1 replacement built now during LS2
  - Also features an improved readout chips
- Joint project of PSI, ETH Zurich, Helsinki Institute of Physics, and RBI
  - RBI team's main task to perform a complete qualification and calibration of 140 pixel modules



L1 module overview

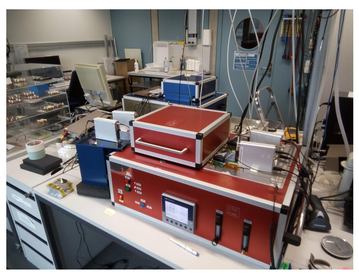
- High-density interconnect (HDI10d)
  - Glued on top of the sensor and wire-bonded to readout chips (ROCs)
  - Routes control and data signals between ROCs and token bit manager chips (TBMs)
  - Routes high-voltage to the sensor
- Sensor
  - "Sandwiched" between HDI and ROCs
  - Connected with ROCs through bump-bonds (bottom image)
- Read-out chips (PROC600 v4)
  - 16 chips at the bottom of the module
  - "Reads" signals from sensor, processes them and sends to TBM





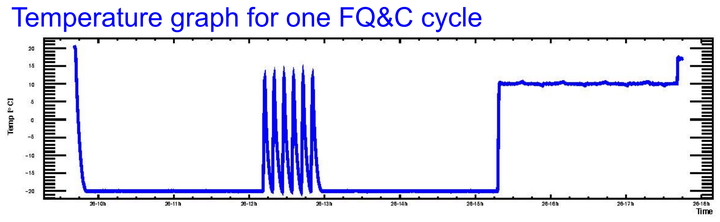
Test setup and procedures

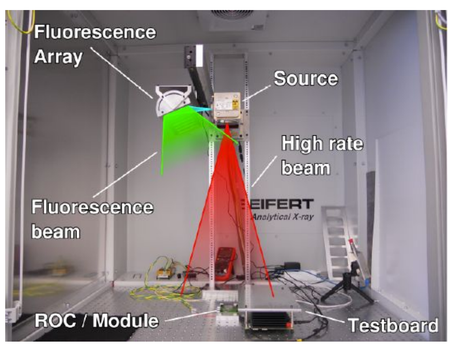
Cold box setup at PSI



- Modules electrically tested and calibrated (up to 4 modules tested in parallel in a temperature and humidity controlled environment)
- **IV** curve taken after each **FQ&C**
- **FQ&C+IV**@-20 °C, 5 **T-cycles** (from -20 to +10 °C), **FQ&C+IV**@-20 °C, **FQ&C+IV**@+10 °C → Takes ~8 hours in total

Temperature graph for one FQ&C cycle



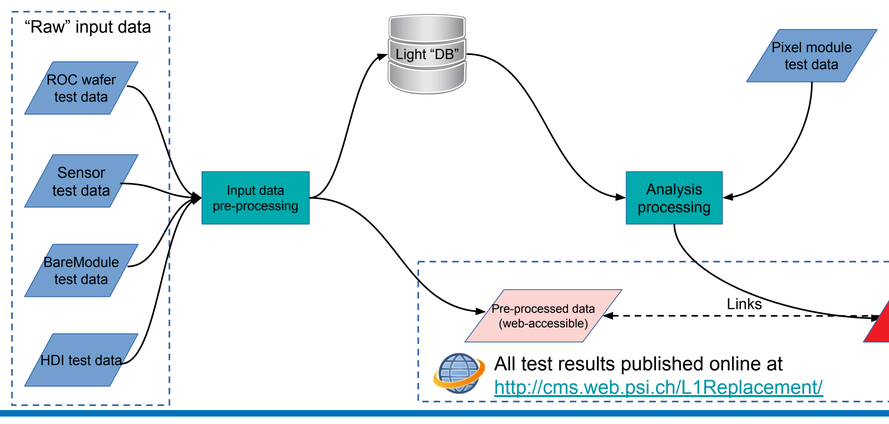


X-ray setup at ETHZ

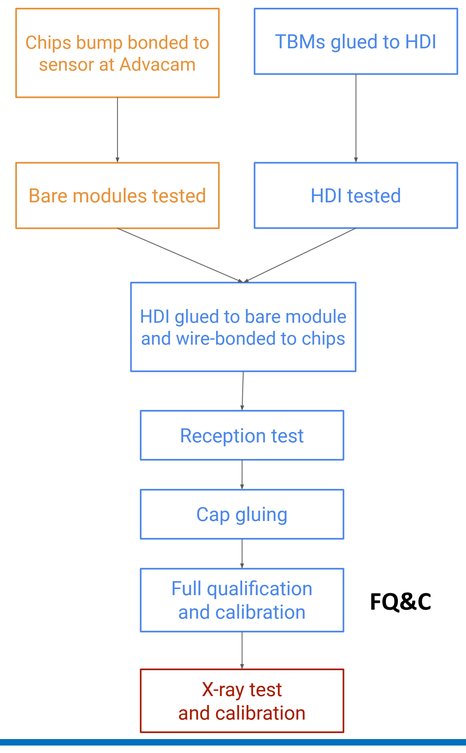
- Pixel hit efficiency at high rates
  - ~65 minutes
- Calibration of Vcal DAC into electrons
  - ~25 minutes

Testing up to 2 modules in parallel. Vcal calibration using 4 fluorescence targets

Data analysis workflow

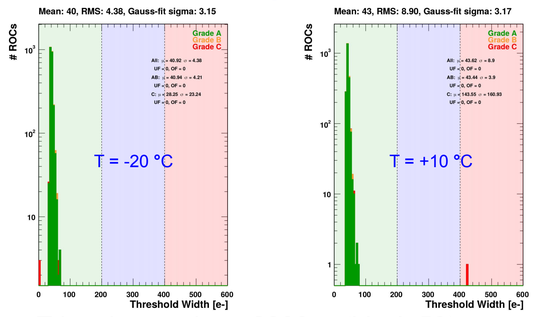


Module testing workflow



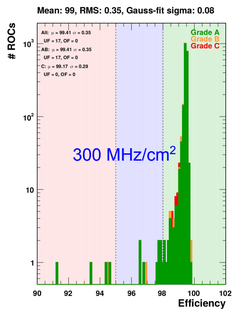
Module performance

Threshold trimming



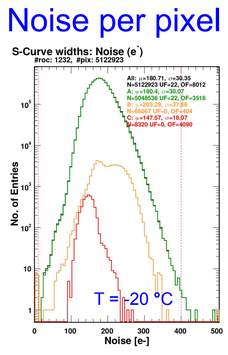
- Trimming to about 2000 e^- (Vcal=50)
- Thresholds uniform within about 40 e^- and stable versus temperature

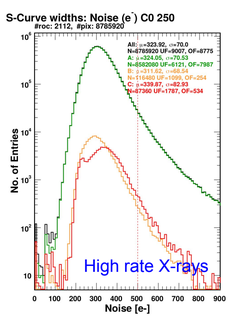
High rate efficiency



- 300 MHz/cm^2 X-ray rate corresponds the expected hit rate on L1 at the LHC
- Modules not installable if hit efficiency <95%
- Great majority of ROCs have hit efficiency above 98% (target for PROC600)

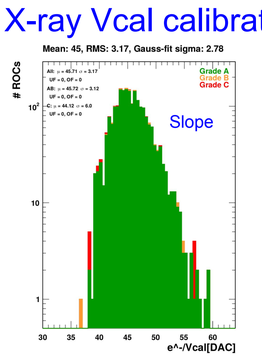
Noise per pixel

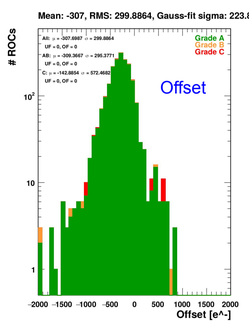




- Mean of about 200 e^- and small tail
- Under X-rays, higher noise with longer tail, rate of noisy pixels still low (~1-2%)

X-ray Vcal calibration





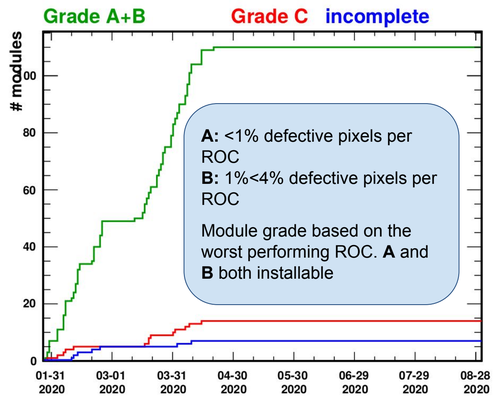
1 VCal [e^-] = (45.7 x VCal [ADC] - 309) e^-

- Very narrow distribution of slopes, allows using just one value for all ROCs

Production yield

Goal: production of 96 installable modules + 20% spares

Cumulative production graph

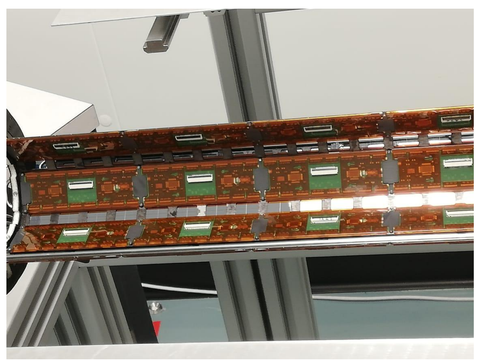


Grading overview

	Grade			
	A	**B**	**C**	**Total**
Full qualification	13	110	3	126
High rate test	87	24	12	123
Failed at reception (incomplete)	/	/	/	5
Faulty after assembly	/	/	/	10
Final	8	102	14	141

Yield=(**A**+**B**)/**Total**=110/141=**78%**

Mounted L1 modules



- Production and testing campaign successfully completed
- Final **production yield** of **78%** (**110 installable modules**)
- Modules ranked based on their quality and accordingly assigned to appropriate locations on L1 (highest quality modules in the center)
- Module mounting on the L1 support structure successfully completed

REFERENCES

[1] CMS Technical Design Report for the Pixel Detector Upgrade, CMS Collaboration (A. Dominguez et al.), Sep. 7, 2012, CMS-TDR-011, URL: https://cds.cern.ch/record/1481838

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