



3D-trench Silicon Pixels with 20 ps timing resolution (or even less !)

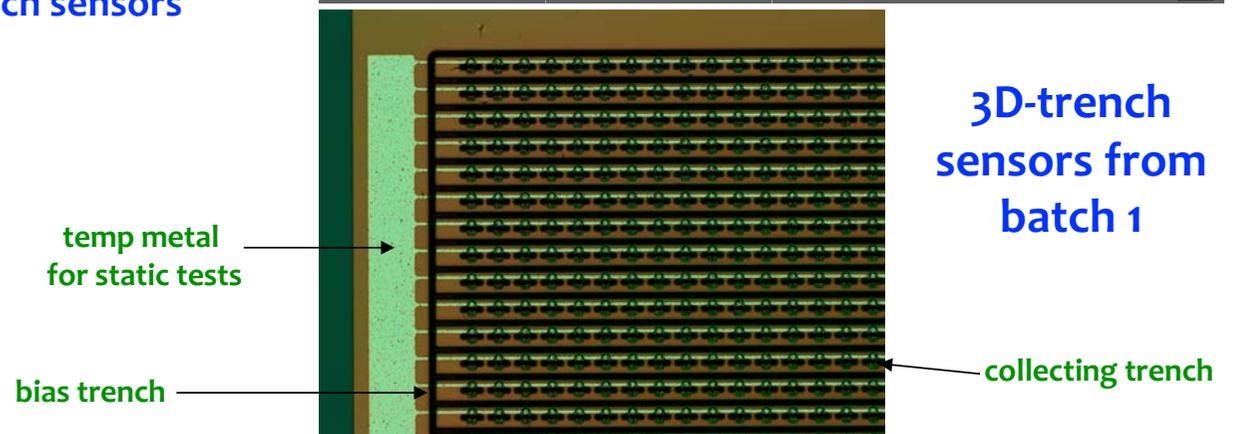
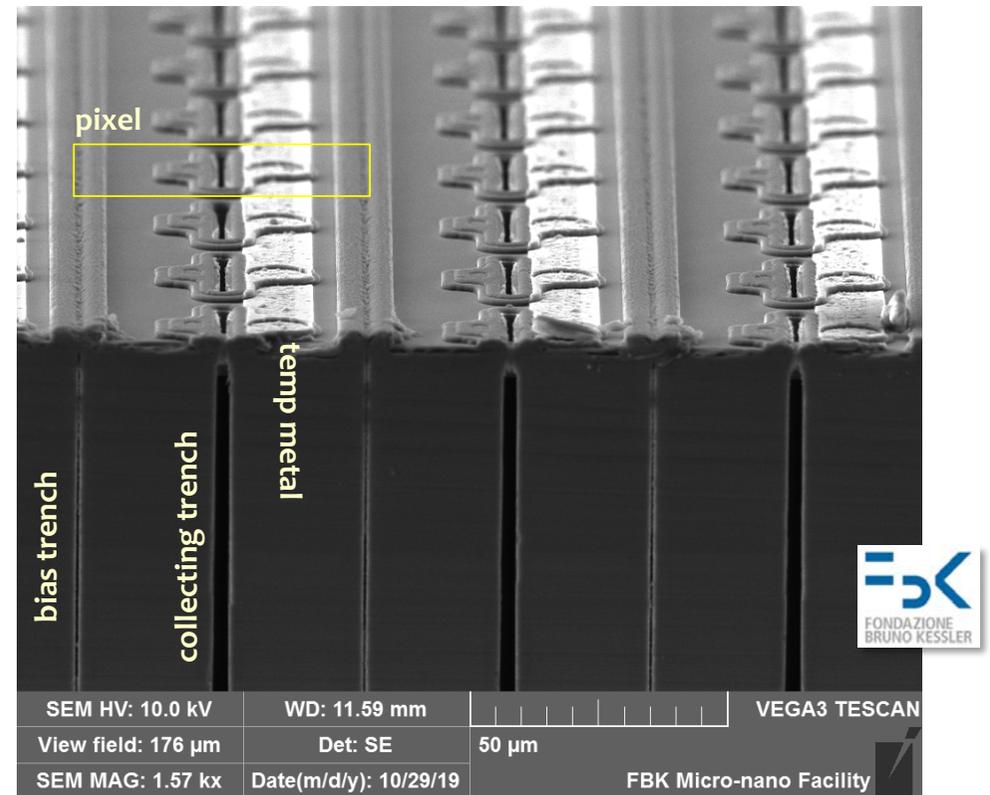
Adriano Lai

INFN – Sezione di Cagliari – Italy



Talk outline

1. Fundamental requirements of future (and next-to-the-future) **vertex detectors**
2. 3D sensors and the **geometric approach**
3. Analysis of **test-beam results from TimeSPOT**: what we have learned
4. The **read-out stage**: Theoretical and implementation limits
5. Read out implementations for fine-pitch sensors with timing: the **Timespot1 ASIC**



The next challenge of tracking in physics at colliders

ATLAS & CMS Phase-II 2026:

Timing layers with 1 timed point: $\sigma_t \approx 30$ ps. $\sigma_s \approx 100\text{--}300$ μm . $F \approx 10^{15}$ 1 MeV $n_{\text{eq}}/\text{cm}^2$. Approaching production stage.

LHCb Upgrade-II (2030s)

$\sigma_t = 50\text{--}30$ ps per hit (pixel) \rightarrow 20–10 ps per track

$\sigma_s \approx 10$ μm (pixel pitch 40–50 μm)

$F = 10^{16}$ 1 MeV $n_{\text{eq}}/\text{cm}^2$ (yearly replacement) to 10^{17} 1 MeV $n_{\text{eq}}/\text{cm}^2$ (no replacement)

FCC-hh (2040s?). Numbers still under discussion

$\sigma_t = 20\text{--}10$ ps per hit (pixel) \rightarrow 10–5 ps per track

$\sigma_s \approx 10$ μm (pixel pitch 40–50 μm)

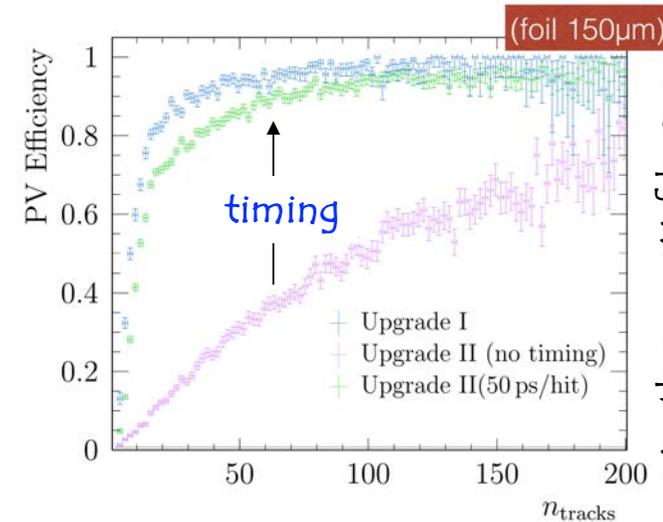
$F = 10^{17}$ 1 MeV $n_{\text{eq}}/\text{cm}^2$ to 10^{18} 1 MeV $n_{\text{eq}}/\text{cm}^2$

FCC Collaboration, "The Future Circular Collider (FCC) Conceptual Design Report," CERN-ACC-2018-0056, CERN-ACC-2018-0057, CERN-ACC-2018-0058, CERN-ACC-2018-0059.

μ -Colliders (2040s?). Starting studies.

Timing absolutely crucial for beam background rejection: $\sigma_t \approx 20$ ps per hit (?)

Rumors, spring 2020



LHCb upgrade-II Wshp, March 2020

The 3-fold pixel[©]

When the vertex detector is concerned, the requirements on space and time resolution **MUST be satisfied simultaneously per single pixel**. Moreover, the pixel of the next generation of vertex detectors **MUST** be very rad-hard.

We can talk of a 3-fold pixel, satisfying the following requirements

Space resolution: $\sigma_s \approx 10 \mu\text{m}$

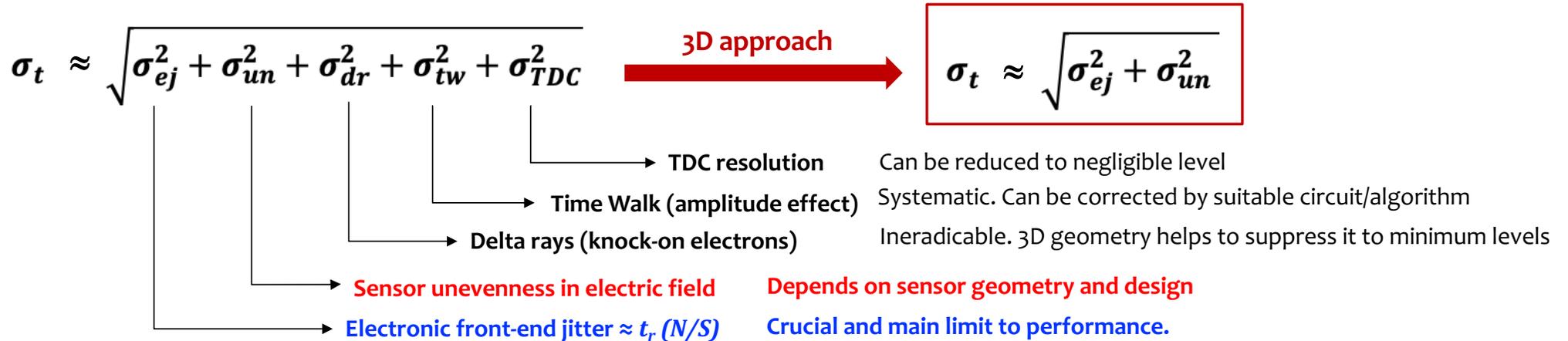
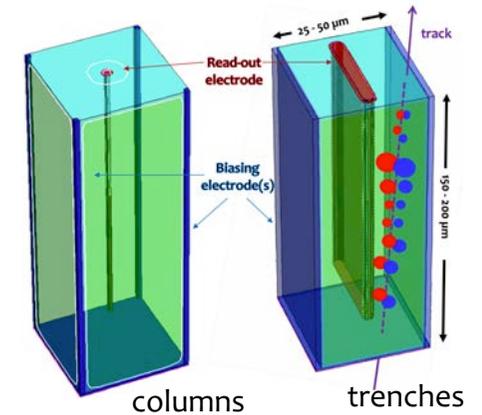
Time resolution: $\sigma_t = 50\text{--}10 \text{ ps}$ (depending on the specific set-up)

Radiation resistance: $F = 10^{17} \text{ 1 MeV n}_{\text{eq}} / \text{cm}^2$

- A “pixel” is a complex system, comprising the sensing part and the read-out (electronics) part. Such properties refer to the system as a whole and development of such 3-fold pixel is a complex development of **high-performance sensor and related electronics**
- The 3-fold pixel as defined above **is still to be conceived and developed**

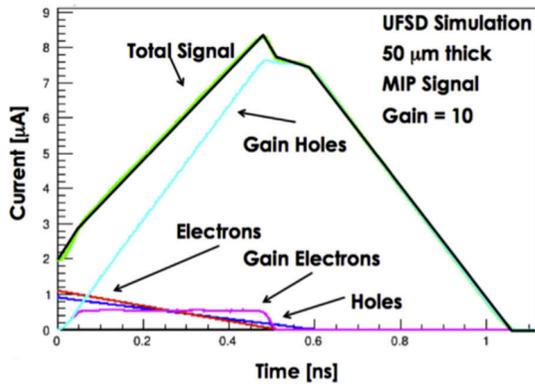
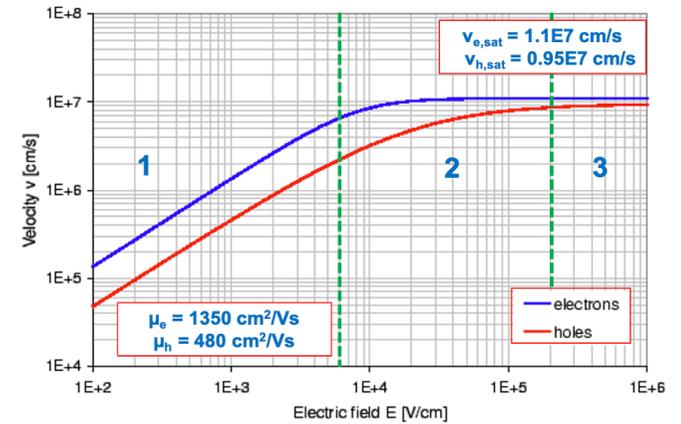
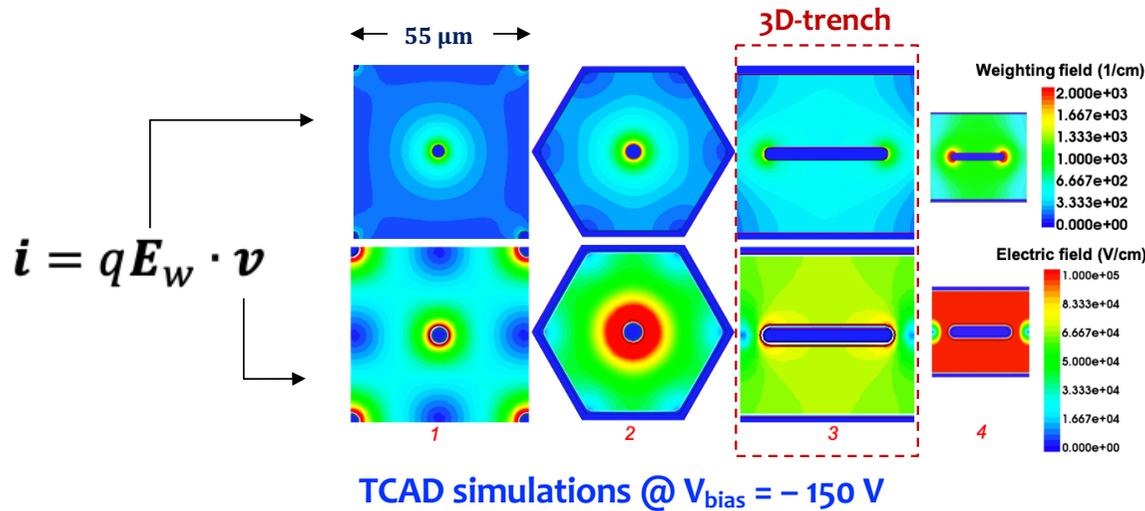
The Geometric approach and 3D technology

Contributions to uncertainty in the time measurement



The possibility to minimize the σ_{un}^2 term **by design** is the decisive advantage of 3D sensors with respect to any planar approach, where the shape of the sensitive volume is basically fixed

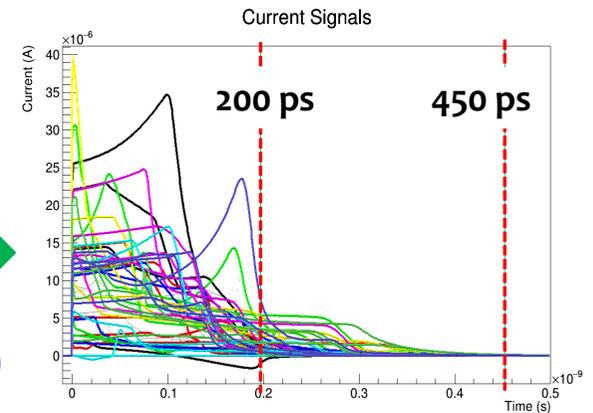
The Geometric Approach: what does it mean



**Ultra
Fast
Silicon
Detector
(LGAD)**

$$\sigma_{ej} = \sigma_n \left[\frac{dV}{dt} \right]_{Thr}^{-1} \approx t_r \left(\frac{S}{N} \right)^{-1}$$

**3D silicon sensor
Trench geometry
average
Charge
Collection
Time
 ≈ 250 ps ($V_{bias} = -100$ V)**

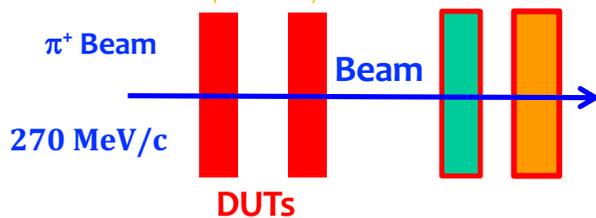
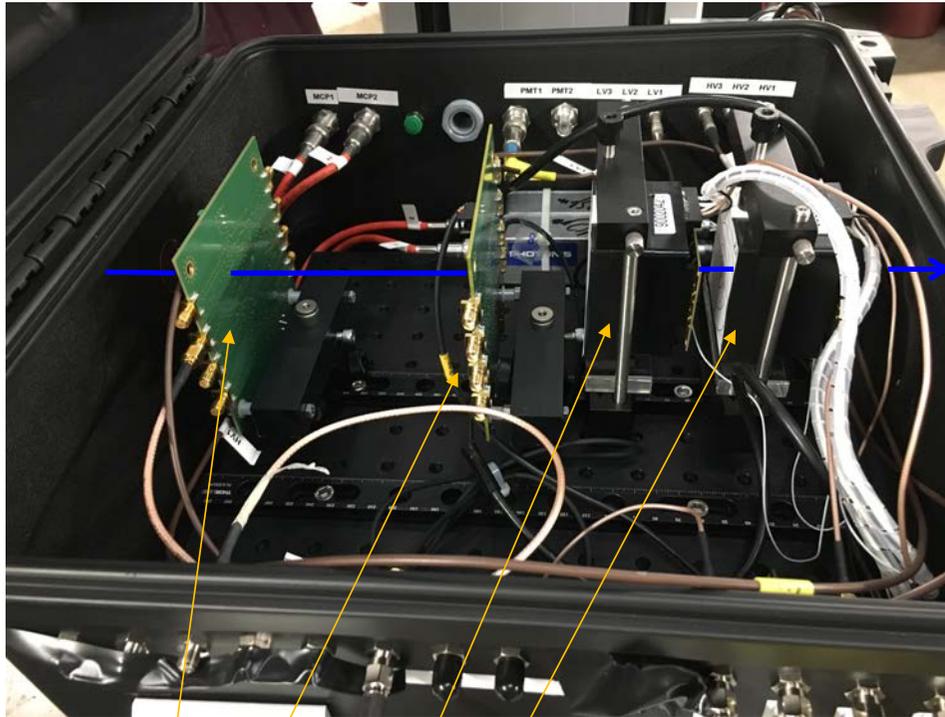


An intrinsically fast sensor requires a current-wise read-out



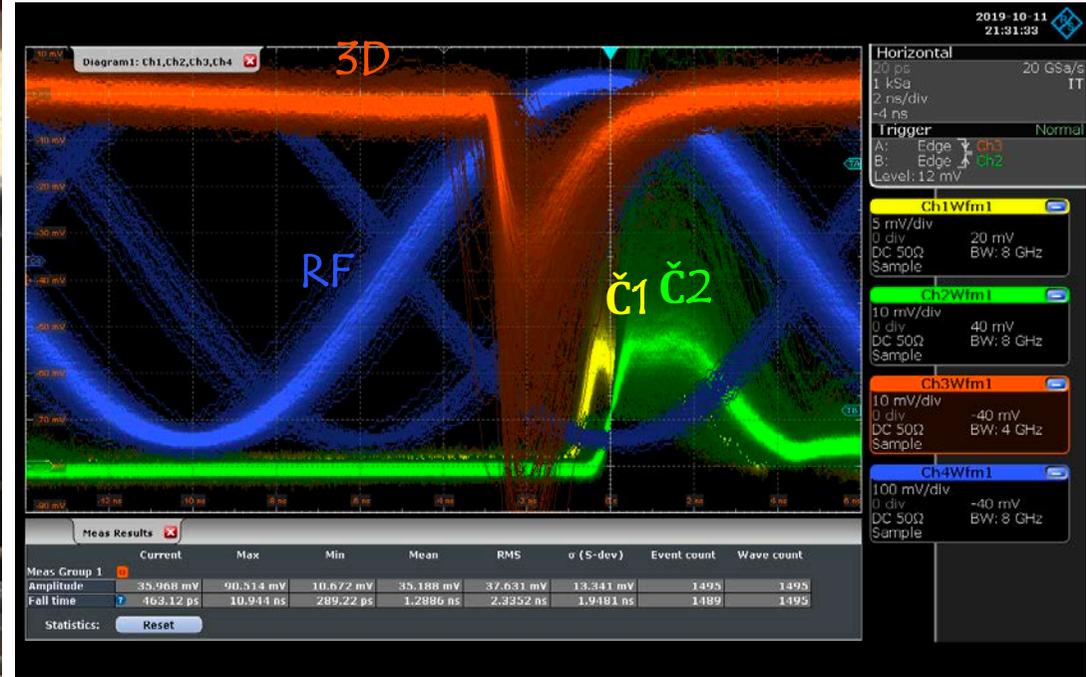
Tests beam @ PSI π M1

October 2019



Time Taggers:
Quarz Cherenkov radiator
+ MCP

$$\sigma_t \approx 15 \text{ ps (each tagger)}$$



acquired signals on a R&S RTP084 8 GHz Oscilloscope, 20 GS/s

Several geometries tested:

Silicon (trench geometries, 55 μ m pitch):

Single pixel, double pixel, pixel strips with 10 or 20 pixels/strip.

Diamond (column geometries, 55 μ m pitch):

Matrix of 800 columns

*Compatible with Timepix family ASICs

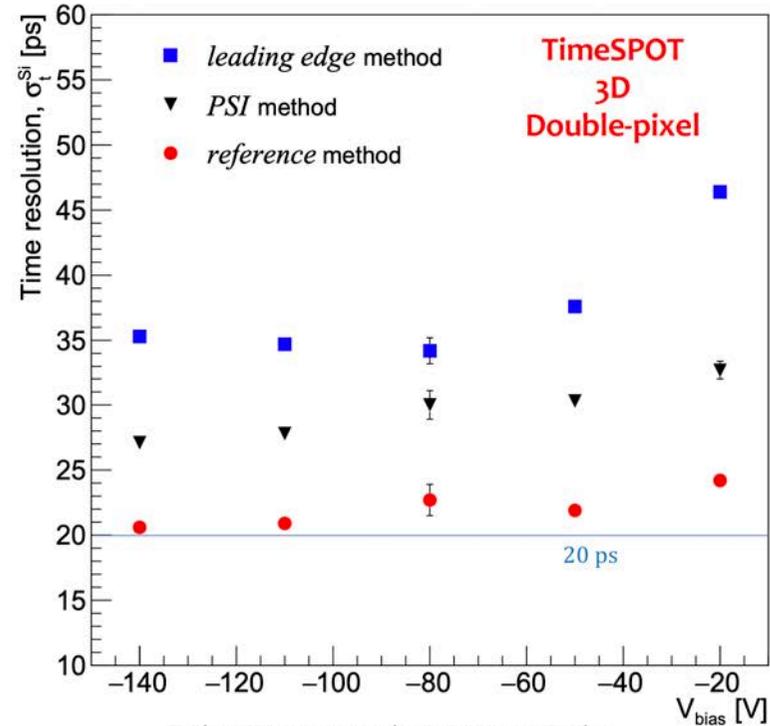
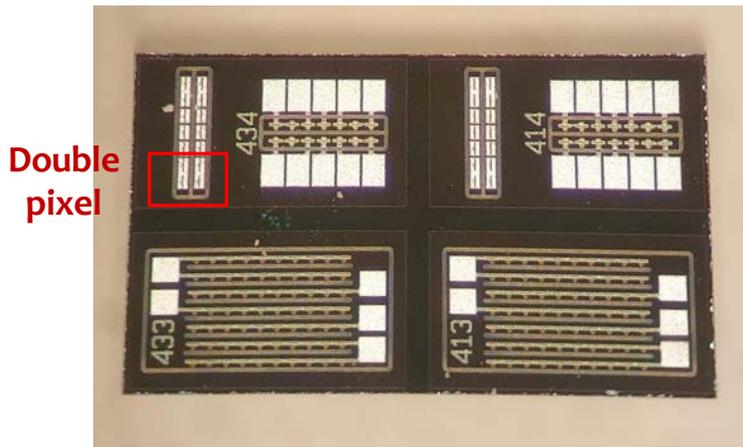
Summary of Test-beam Results on σ_t

Aim:

study the **intrinsic** performance of the 3D-trench pixel

The 3D pixel time resolution is measured at various biases by *subtracting (in quadrature) the time-tagger jitter*:

- **Reference method:** Constant fraction algorithm after differentiation.
- **PSI method:** traditional Constant Fraction Discriminator at 35% max amplitude
- **Leading edge method:** simple leading-edge triggering at fixed threshold with no correction for the time-walk



Each point corresponds to ≈ 20000 samples.
The -80 V set counts 3000 samples

Details on: L. Anderlini et al., *Intrinsic time resolution of 3D-trench silicon pixels for charged particle detection*, JINST 15 P09029 (2020).



Estimate of the geometric term σ_{un}

Measured time resolution vs. signal amplitude scales

$$\text{as } \sigma_t = \sqrt{\left(a^2 + \frac{b^2}{\text{Amplitude}^2}\right)}$$

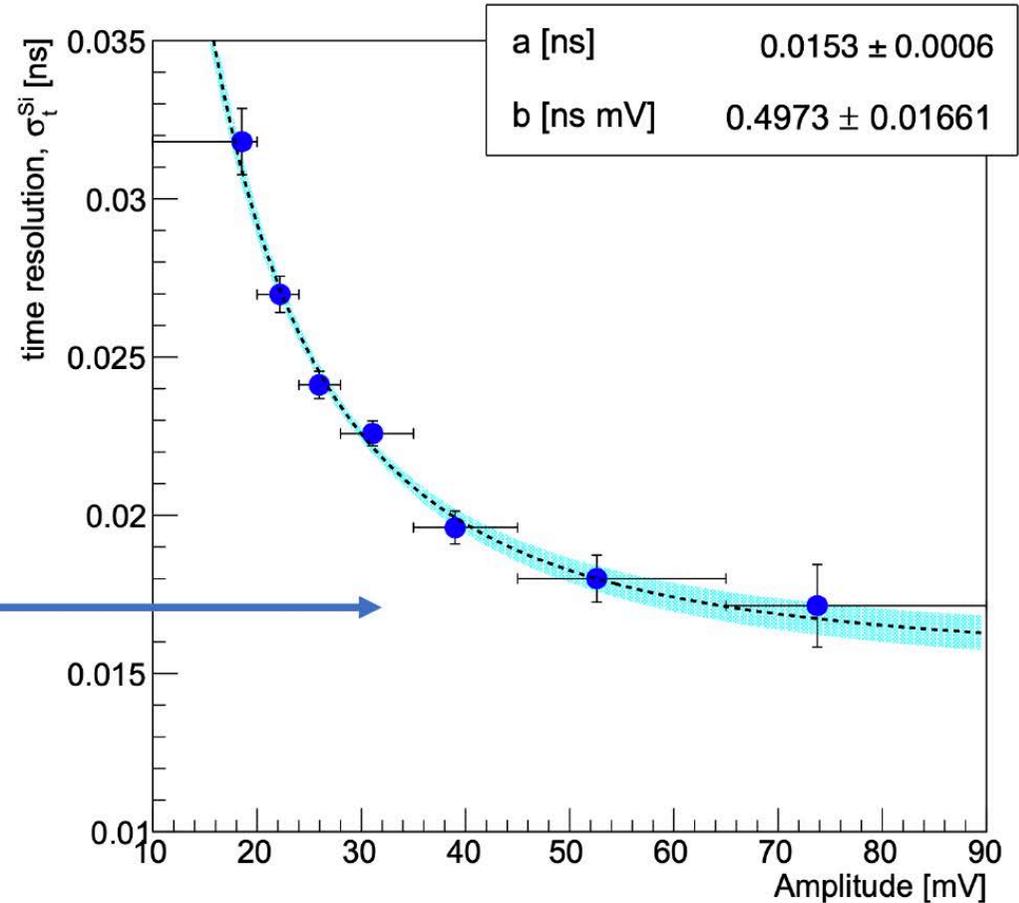
This is in agreement with what we discussed:

$$\sigma_t \cong \sqrt{\sigma_{un}^2 + \sigma_{ej}^2(\text{Amplitude})}$$

Following this approach:

- **a** represents σ_{un} , the intrinsic limit to sensor timing performances
- **b/Amplitude** is the contribution of electronics noise to the time resolution

$$\sigma_{ej} = \sigma_n \left[\frac{dV}{dt} \right]_{Thr}^{-1} \approx t_r \left(\frac{S}{N} \right)^{-1}$$



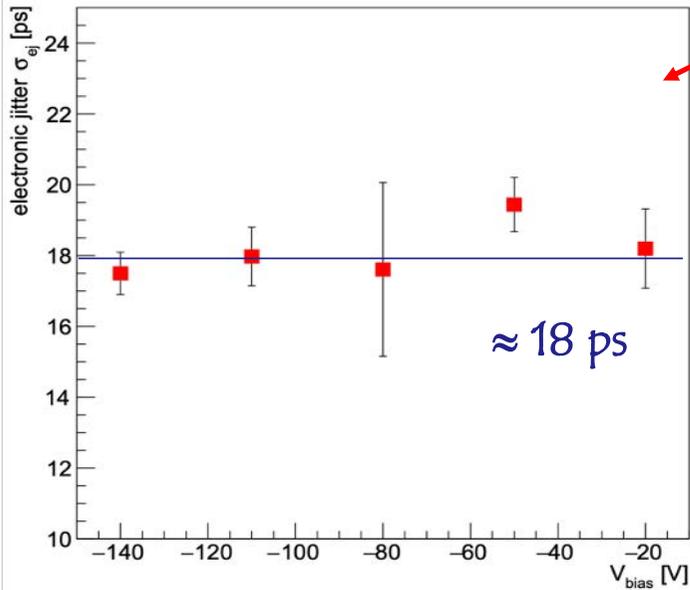
Test-beam results. V_{bias} scan. σ_{ej} VS σ_{un}

Measured performance on 3D-trench pixels



σ_{ej}

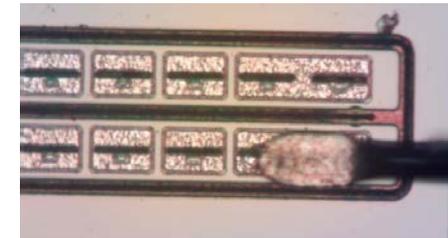
Depends on signal amplitude
independent of V_{bias}



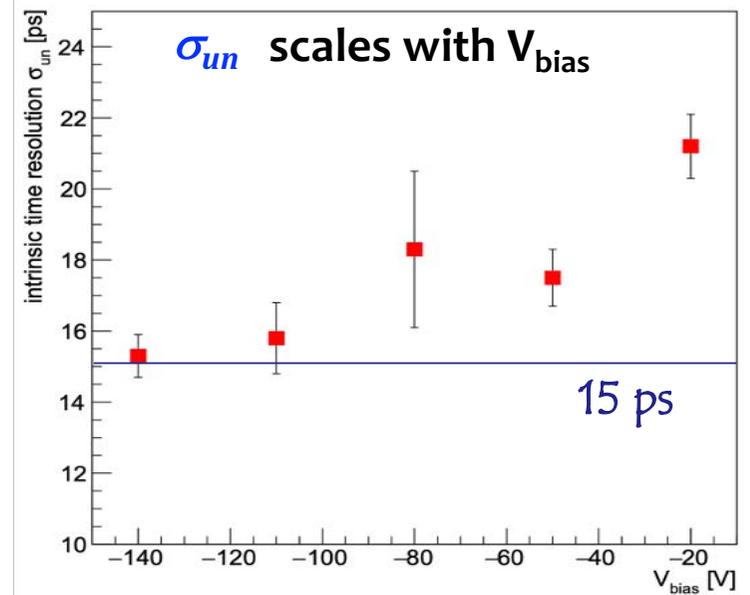
$$\sigma_t = \sqrt{\sigma_{ej}^2 + \sigma_{un}^2}$$

$\sigma_t (V_{\text{bias}} = -140 \text{ V}) = (20.6 \pm 0.4) \text{ ps}$

V_{bias} [V]	S/N	N [mV]	dV/dt [mV/ps]	σ_t^{SI} [ps]
-20	12.2	2.22	0.097	24.2 ± 0.5
-50	13.0	2.24	0.114	21.9 ± 0.4
-80	13.3	2.26	0.121	22.7 ± 1.2
-110	13.6	2.26	0.125	20.9 ± 0.4
-140	13.9	2.25	0.128	20.6 ± 0.4



Double pixel



Intrinsic time resolution of a 3D-trench sensor σ_{un} (right) and contribution of the electronic jitter σ_{ej} (left) vs bias Voltage. Complete σ_t is obtainable as the quadrature sum of the two contributions.

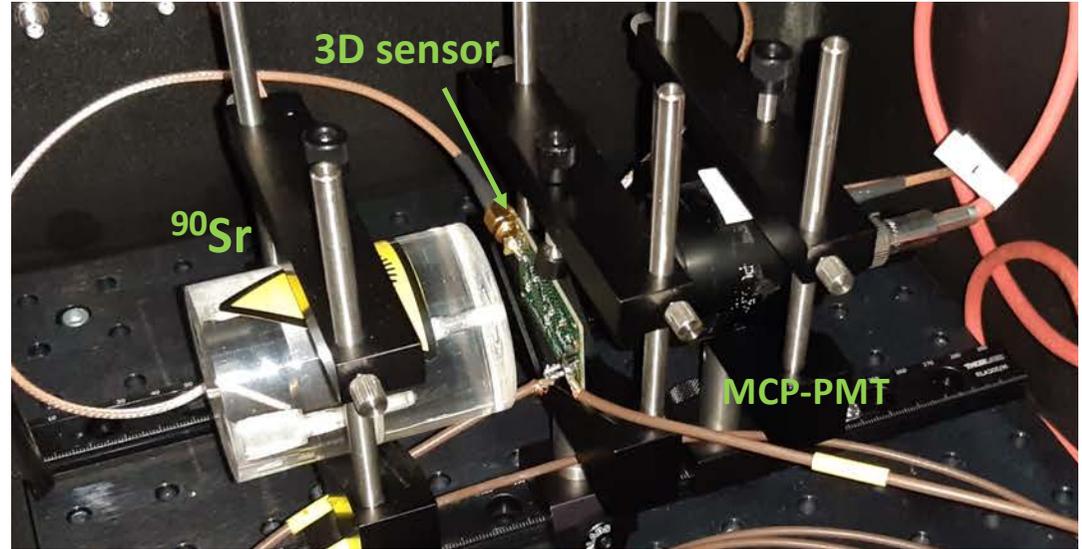
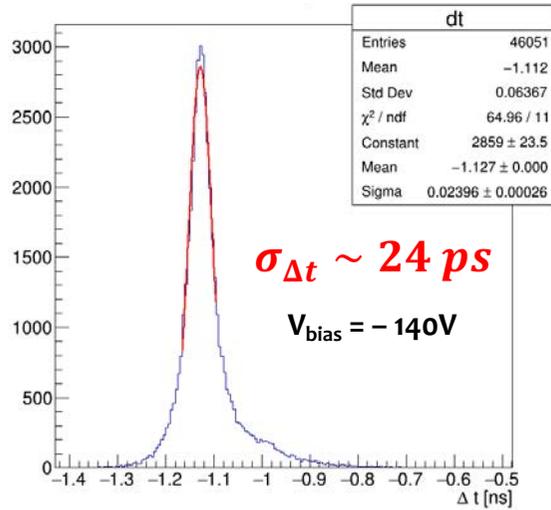
Other measurements: β ^{90}Sr source in the lab

$$\Delta t = t_{MCP} - t_{3D}$$

3D: Double pixel



24 ps includes also the MCP contribution

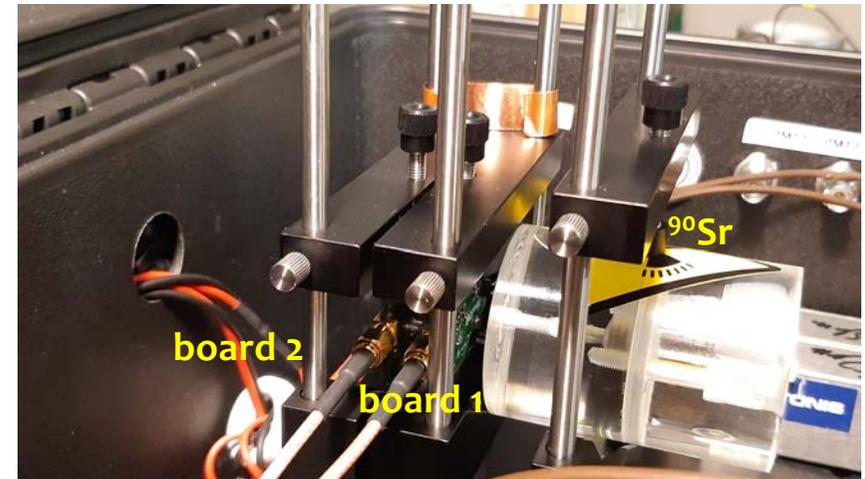
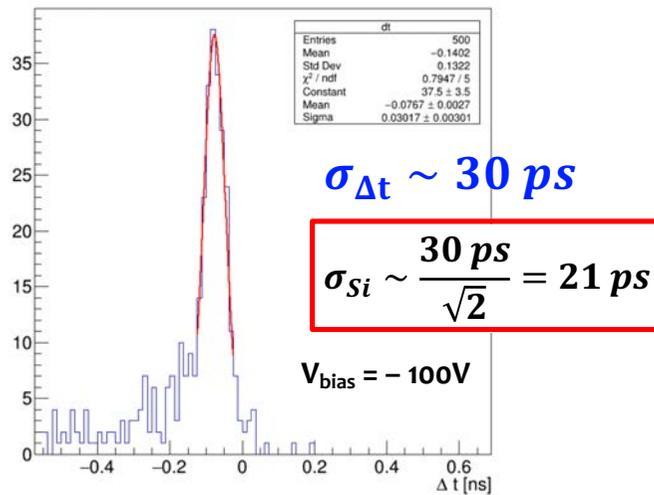
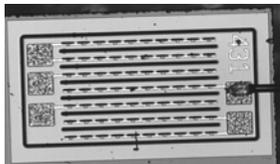


$$\Delta t = t_{3D1} - t_{3D2}$$

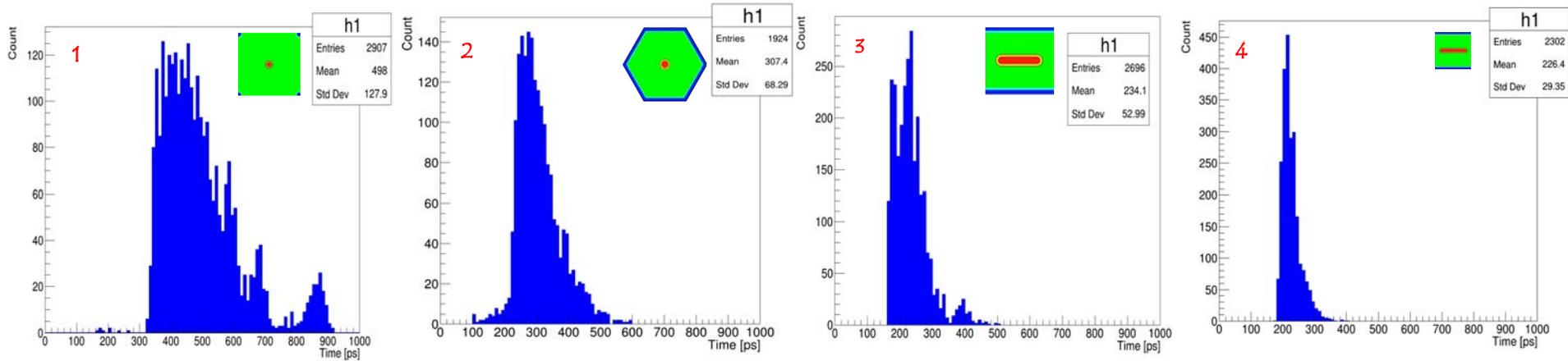
3D1: Double pixel



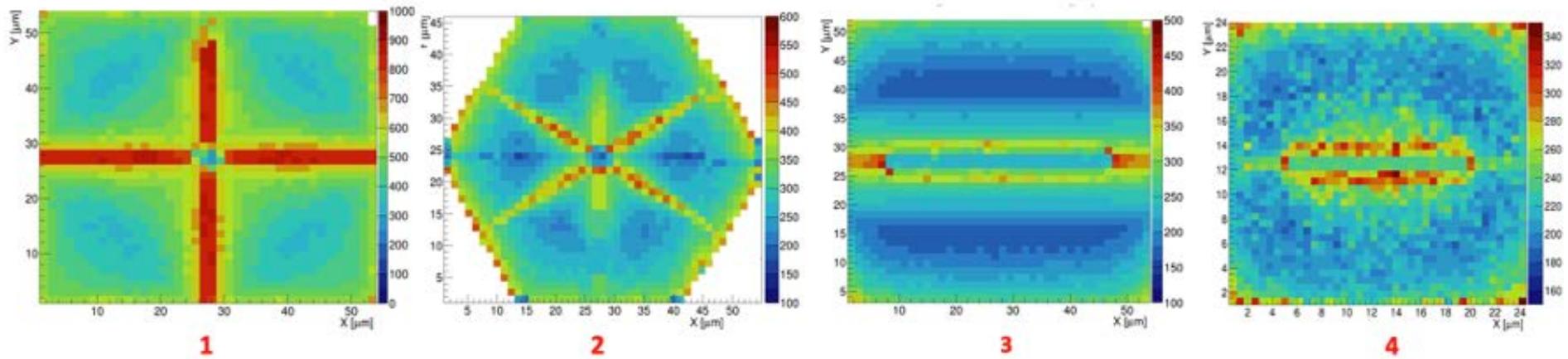
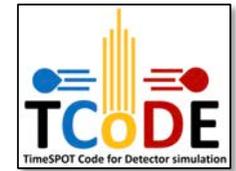
3D2: Strip pixel



The Geometric approach and sensor speed: can we go further?



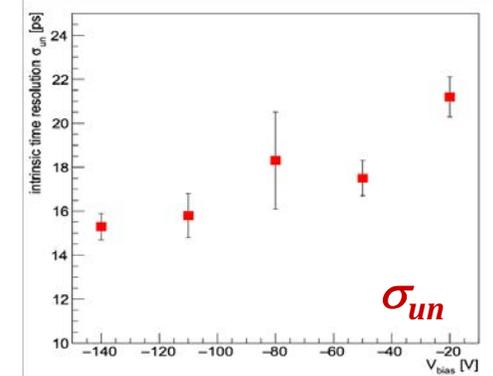
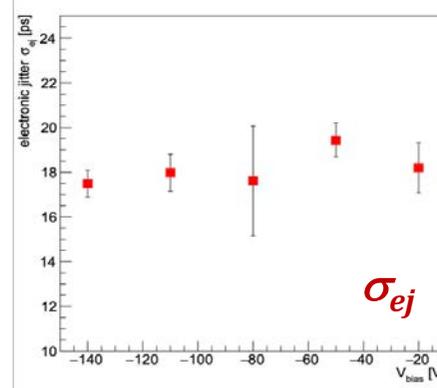
Charge Collection Time distributions for different 3D geometries ($V_{bias} = -150V$)
(total drift times of charge carriers)



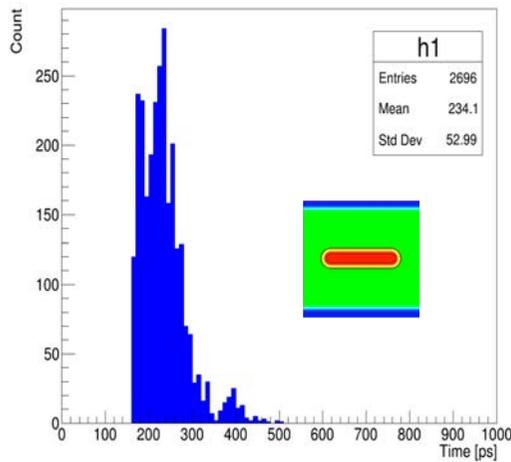
Performance limits to the intrinsic sensor speed

- What is the limiting factor ?
- How does the sensor intrinsic speed translate into final time resolution?

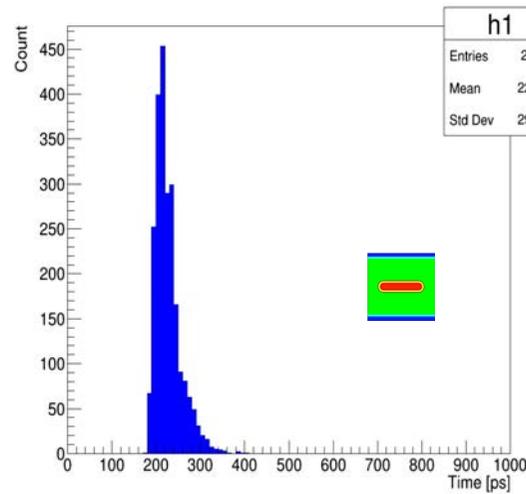
Electronics touches and limits Sensor performance



CCT distributions



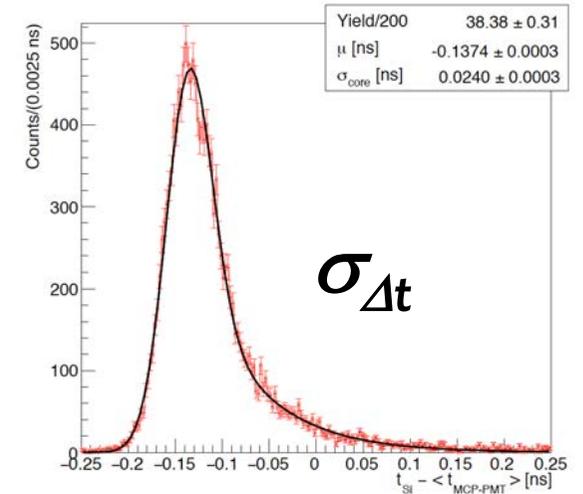
3D-trench
55 μm pitch



3D-trench
25 μm pitch



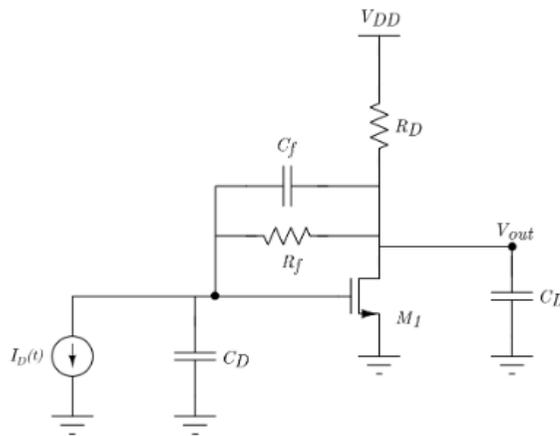
Δt measurement



Front-end solutions

Electronics: possible solutions (discrete components and integrated)

Trans-Impedance-Amplifier with shunt-shunt feedback (FB-TIA).



Simplified schematic of the FB-TIA amplification stage

According to the FB parameters used, this scheme can range from an integrator (Charge Sensitive Amplifier) to a fast Current-Sensitive front-end. The role of the specific transistor technology used is also decisive, especially when very high speed is pursued (Si-Ge vs CMOS).

We can consider two extreme cases as examples⁽¹⁾:

A) CSA-TIA, when the amplifier peaking time $\tau \gg t_c$

It can be demonstrated⁽¹⁾ that in this case

$$\sigma_t = \frac{\partial t_{thr}}{\partial t_c} \sigma_{tc} \approx \frac{1}{2} \left(1 - \frac{V_{thr} \tau (1 + G_0)}{Q_{in} R_f G_0} \right) \sigma_{tc} \approx \frac{1}{2} \sigma_{tc}$$

B) Fast-TIA, when the amplifier peaking time $\tau \approx t_c$

It can be demonstrated⁽¹⁾ that in this case

$$\sigma_t = \frac{\partial t_{thr}}{\partial t_c} \sigma_{tc} \approx \frac{\tau}{2} \sqrt{\frac{V_{th}}{I_0 R_m}} \frac{\sigma_{tc}}{t_c} \approx \left(\frac{1}{2} \frac{\tau}{t_c} \sqrt{\frac{N}{S}} \right) \sigma_{tc}$$

⁽¹⁾ A. Lai and G.M. Cossu, High-resolution timing electronics for fast pixel sensors, to appear on JINST, arXiv:2008.09867

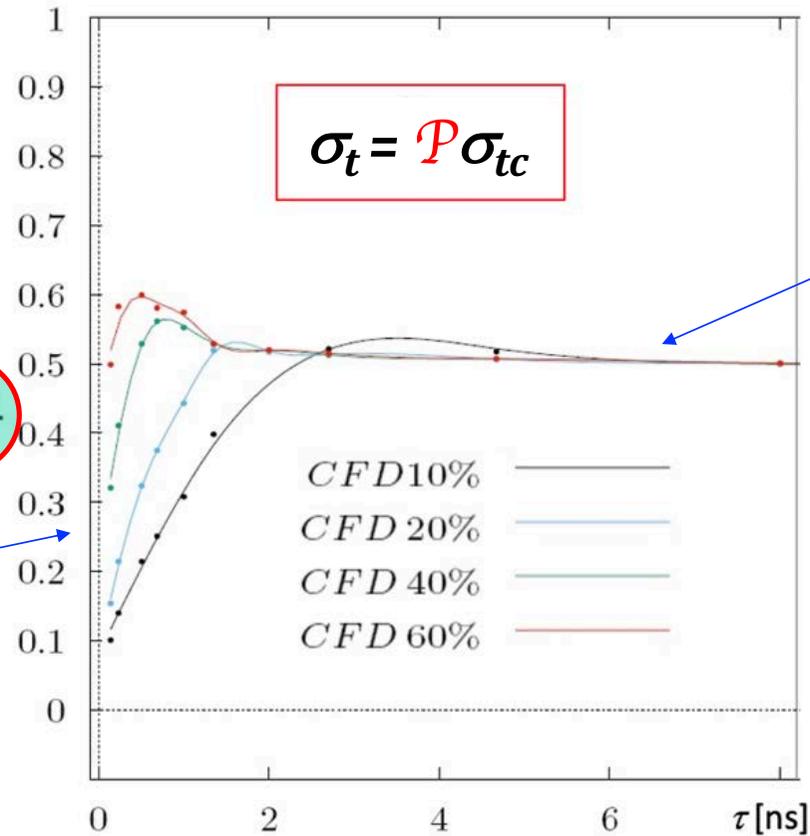
Front-end solutions: theoretical limits

Timing propagation coefficient \mathcal{P}
 (σ_t/σ_{t_c} ratio)
 or
 fraction of CCT standard deviation propagated to σ_t

$$\frac{\partial t_{thr}}{\partial t_c}$$

Fast-TIA
 For $\tau \ll t_c$
 \mathcal{P}

can be considerably less than 1
 Resolutions below 10ps can be theoretically reached



\mathcal{P} (= Derivative of time at threshold t_{thr} with respect to average CCT t_c , aka time centroid) vs the amplifier peaking time τ , at $t_c = 250$ ps for various CFD fractions.

CSA-TIA
 For $\tau \gg t_c$
 \mathcal{P}

tends to $\frac{1}{2}$.
 In the case of a 3D-trench pixel, this corresponds to a range between 15 ps (25 μm pitch) to 25 ps (55 μm pitch), see slide 10.

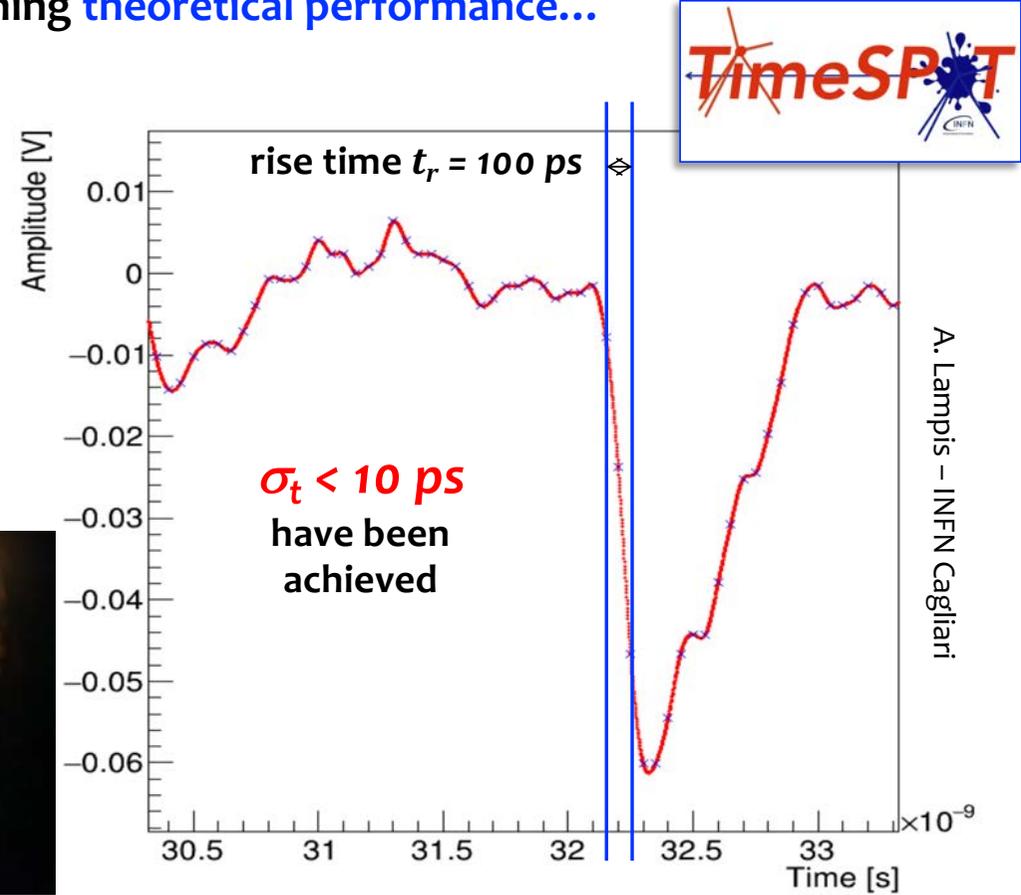
To reach $\tau \approx 100$ ps, the choice of feedback parameters is not sufficient. High performance transistor stages are mandatory as well

⁽¹⁾ A. Lai and G.M. Cossu, High-resolution timing electronics for fast pixel sensors, to appear on JINST, arXiv:2008.09867

Front-end solutions: implementation limits. 1) Si-Ge

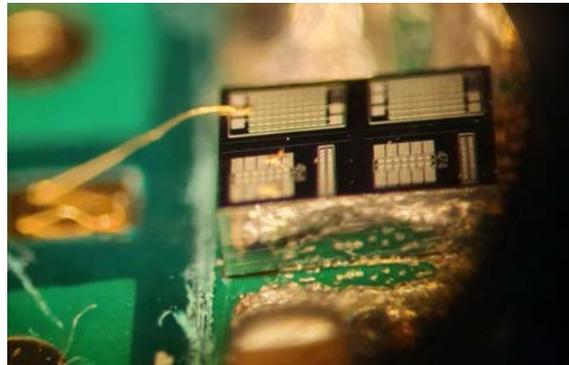
Discrete components **BJT Si-Ge** allows almost reaching theoretical performance...

G. M. Cossu – INFN Cagliari



... Drawbacks:

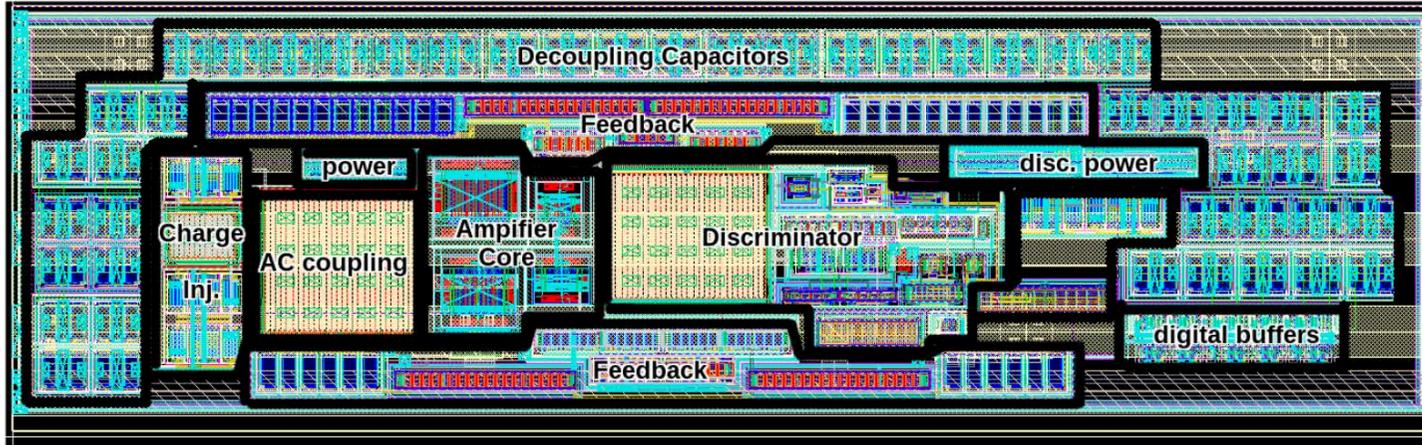
1. High consumption (mW/channel)
2. No integration (few wire-bonded channels)



Integrated **130 nm BiCMOS (Si-Ge)**:

best performance in speed, relatively scarce integration capabilities (not 3-fold)

Front-end solutions: implementation limits. 2) CMOS



TimeSPOT1 (2020)

Amplifier and Leading Edge Discriminator with offset compensation

Cell size: 50 x 15 μm^2

Nominal Power and High Power Simulations

A new scheme: CSA inverter input stage, which sums-up the g_m 's of 2 input (N and P) MOS

- t_r reduction (<2 ns wrt ≈ 12 ns of telescopic cascode, previous solution)
- BW increase + negligible Gain reduction by GBWP effect
- Time jitter reduces by increasing power and do not saturates as in previous version

	Schematic		Layout	
	Nominal	HP	Nominal	HP
Power				
Slew-Rate [mV/ns]	380	540	250	360
RMS noise [mV]	5.0	4.9	3.9	3.8
Jitter [ps]	13.2	9.1	15.6	10.5
Power per channel [μW]	18.2	31.5	18.6	32.9

Programmable consumption

HP stands for High (or maximum) Power

Time-to-Digital-Converter (TDC)

If the “resolution potential” at the sensor level is in the range of 10 ps, also the integration of a TDC having suitable performance is a challenge.

Designing a TDC having some ps of time resolution is not a terrible thing

It could become so when strong limitations in area and power consumption are there. This is the case of the 3-fold pixel (slide 4).

Not many solutions «on the market»:

TDCpix (NA62 GigaTracker, 130nm CMOS) is not a pixel TDC (resolution \approx 150 ps)

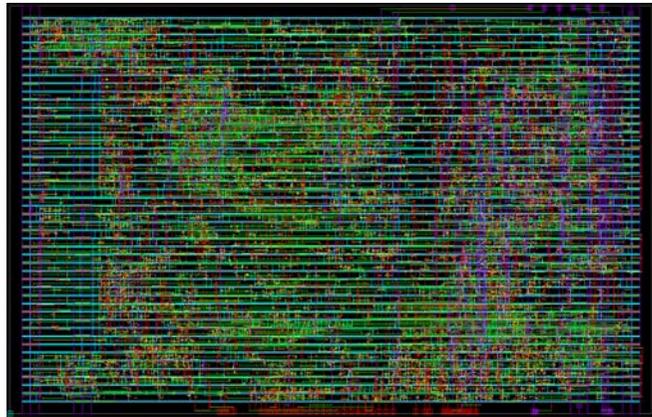
Timepix4 (Medipix, 65nm CMOS): 1 TDC for 8 pixel channels, LSB resolution 195 ps, front-end 60 ps for $> 10 \text{ ke}^-$, under test. General purpose, not HiLumi oriented

Timespot1 (TimeSPOT, 28nm CMOS): **submitted**. Samples back beginning 2021 TDC for 3-fold pixels. Reduced matrix test ASIC (32x32 channels), 1 TDC per pixel, simulated post-layout resolution \approx 10 ps LSB.

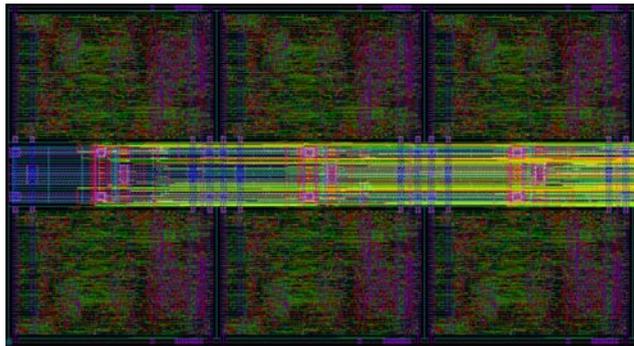
All-digital approach, exploit the natural technology scaling more efficiently.

Power increase is necessary.

TDC for 3-fold pixels: Synthesizable Vernier (Timespot1)



Cell size: 50 x 31.5 μm^2



Post-layout simulated performance

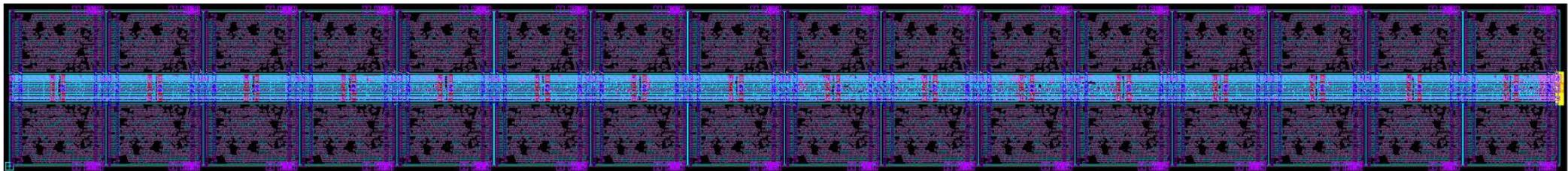
	Internal Pwr (uW)	Switch Pwr (uW)	Leak Pwr (uW)	Tot Pwr (uW)
IDLE	12.2	4.8	3.7	20.7
Calibration	338	211	3.7	552
DAQ 3MHz	101	69.5	3.6	175
DAQ 1MHz	40.4	25.3	3.7	69.3
DAQ 500kHz	26.6	15.2	3.7	45.5
DAQ 100kHz	15.1	6.9	3.7	25.7

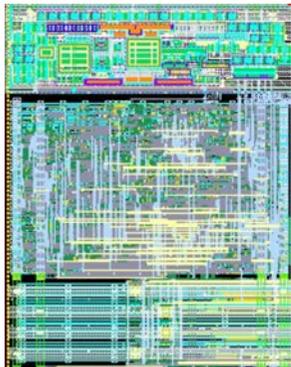
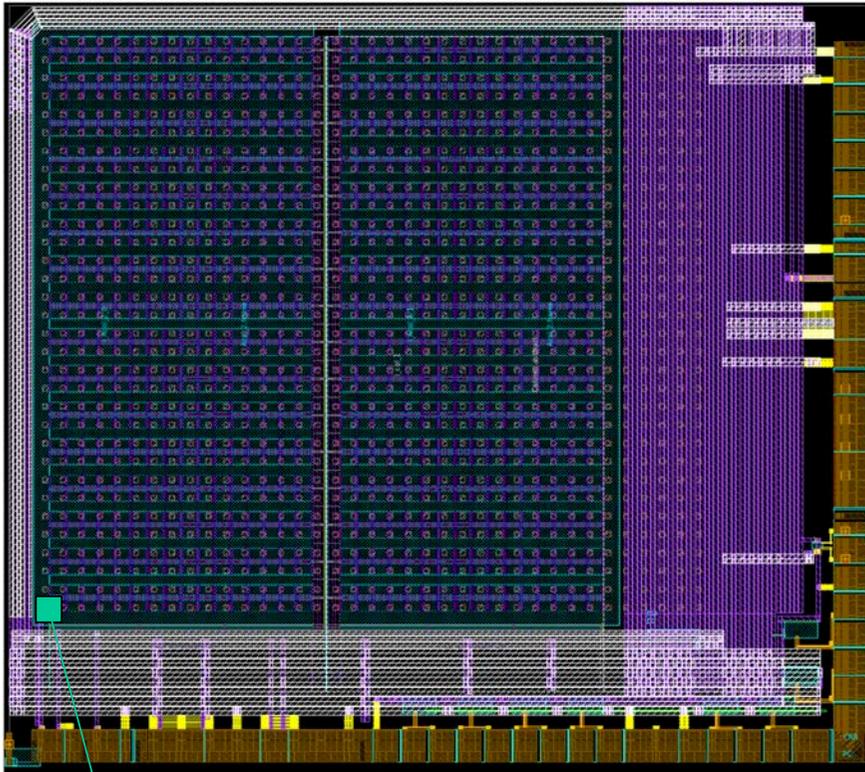
ToA	LSB (ps)	std. sev. (ps)	TOT	LSB (ns)	Bits
MIN	6	2	MIN	0.75	8
TYP	12	3,74	TYP	1.10	8
MAX	12	4	MAX	1,18	8

Time of Arrival

Time over Threshold

Full row size: 800 x 80 μm^2





32 x 32 pixel read-out matrix
To be bonded on 3D sensors, Batch #2
TSV-ready matrix

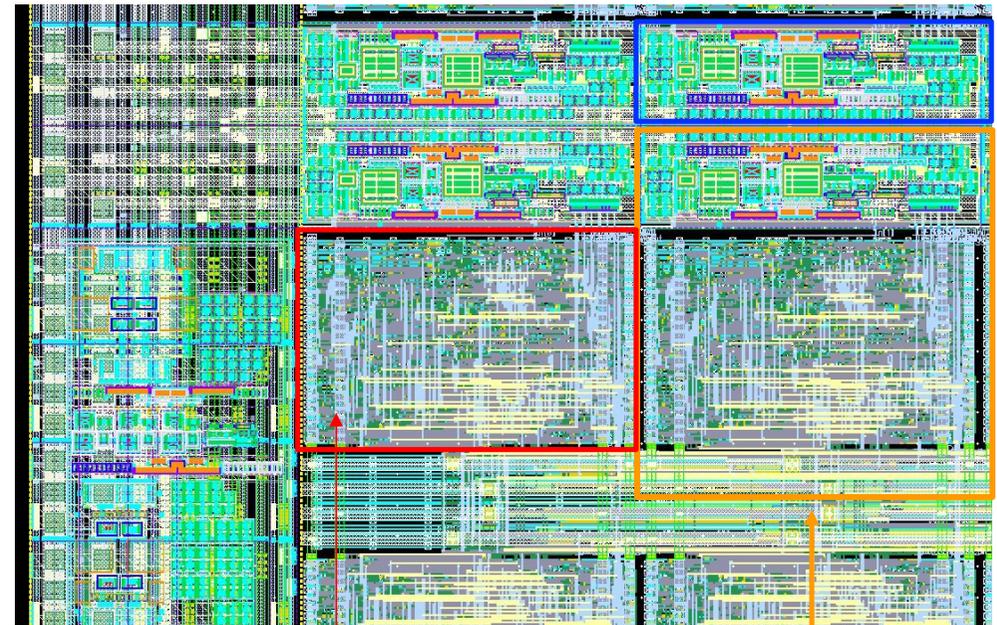
Pixel size: $50 \times 55 \mu\text{m}^2$
Pixel pitch: $55 \mu\text{m}$
1 TDC/pixel

Timespot1 ASIC

Presently under submission



Analogue cell size (CSA amplifier and Leading Edge discriminator): $50 \times 15 \mu\text{m}^2$



Vernier TDC
 $50 \times 31.5 \mu\text{m}^2$

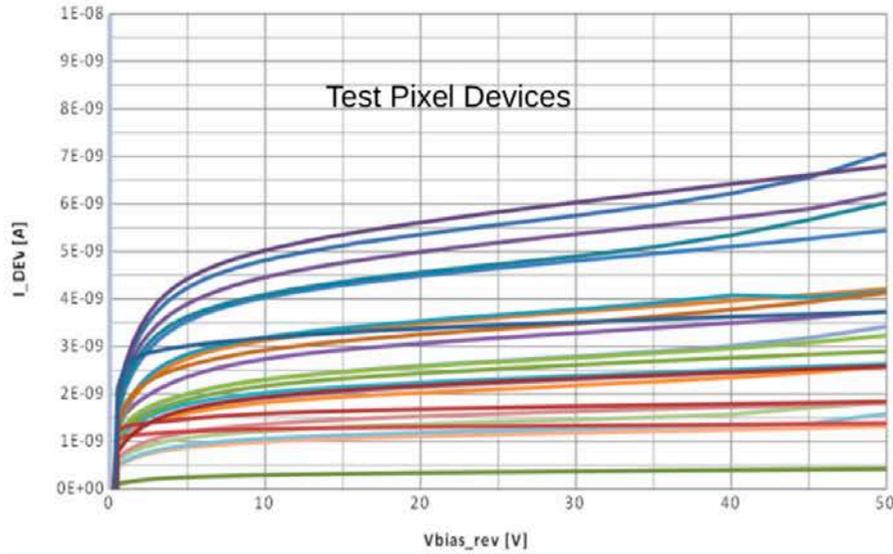
full pixel $50 \times 55 \mu\text{m}^2$

Conclusions and Outlook

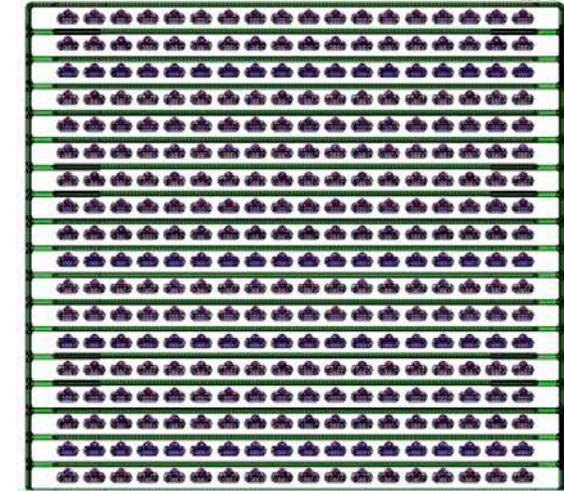
- The challenge for the conception and implementation of a **3-fold pixel device** is of vital importance for the future of HEP in the next 10-20 years
- The 3D **geometric approach** appears as a technology having all the due credentials to reach the target: high space resolution, very high time resolution and un-matched radiation hardness
- The real **bottleneck** of the 3-fold pixel is now the front-end and read-out electronics
- Compared to the given requirements, the **28-nm CMOS technology** is at its technological limit in performance
- **Si-Ge technologies** would allow exploiting better the super-fast sensors but **lacks adequate integration** capabilities and radiation hardness
- An additional issue: speed implies **consumption**. Power must be dissipated using dedicated micro-cooling techniques.

a few more
INSIGHTS

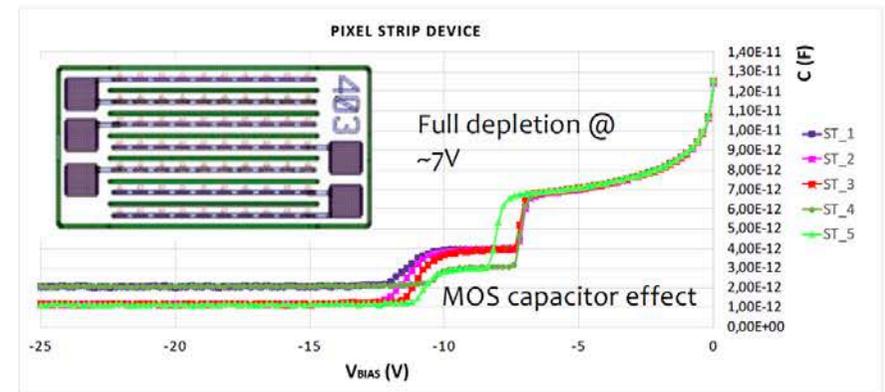
Electrical characterization of Batch#1



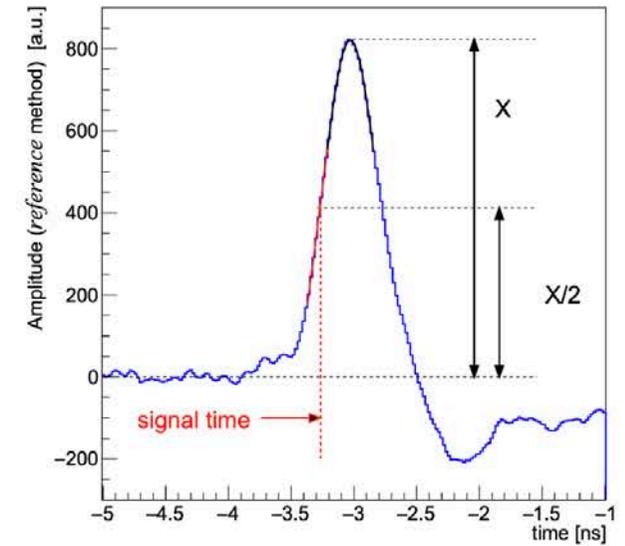
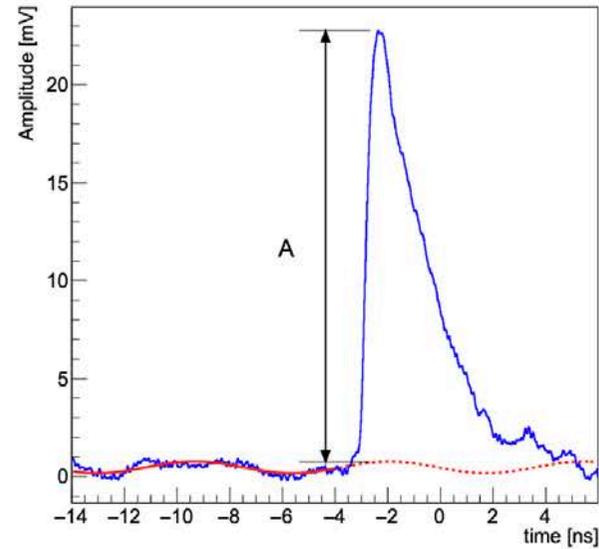
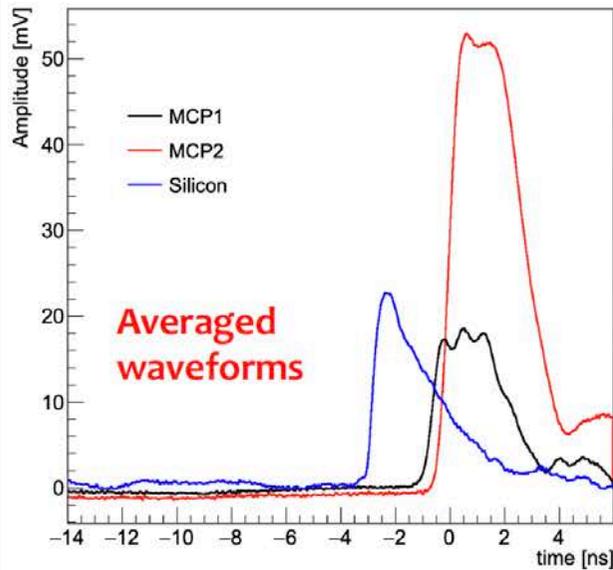
IV-curves on 18x18 pixel matrices (pixels connected with temporary metal):
~10 pA/pixel – good!



Measured capacitance **~100 fF/pixel**,
in agreement with simulation



Waveform processing: the “reference” method



- For each sensor waveform:

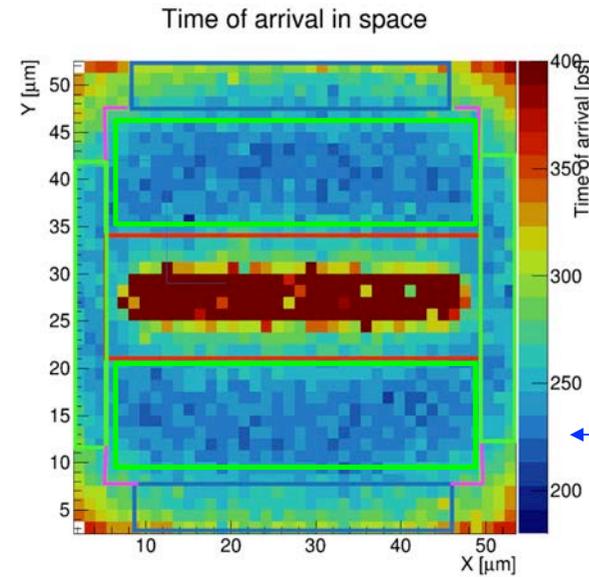
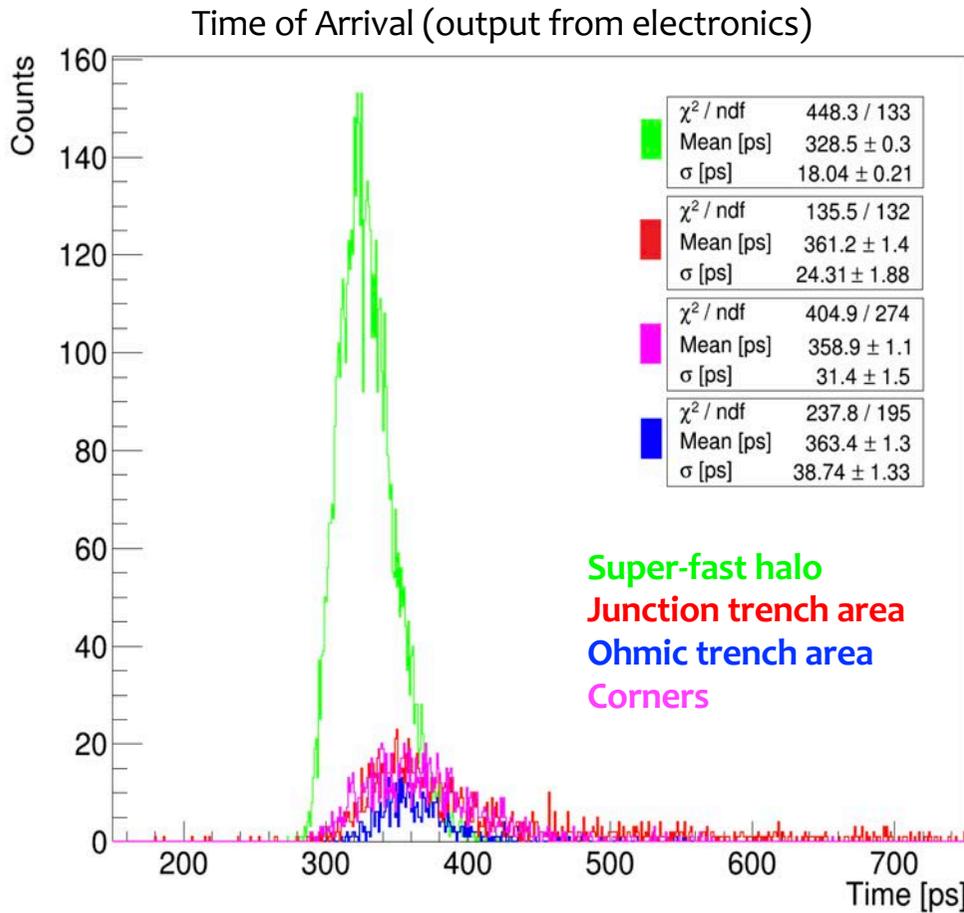
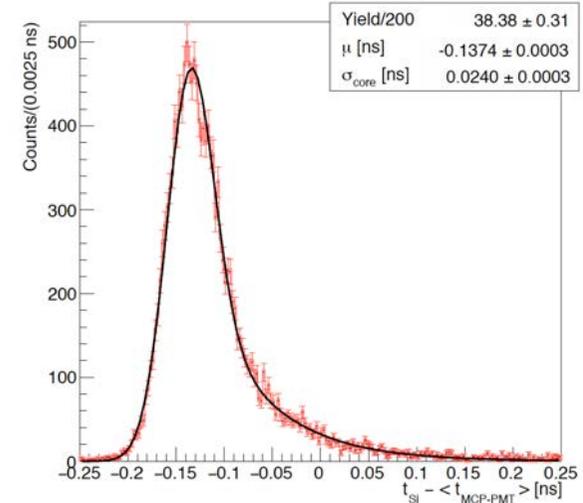
- Signal baseline (red-dashed line) is evaluated on an event-by-event basis
- The signal amplitude **A** is measured (w.r.t. baseline)
- **Reference method**: subtract each waveform from a delayed (by $\sim 1/2$ of the signal rise time) copy of itself, then **trigger at X/2 height** (on a signal linear interpolation from 20% to 80% of X)

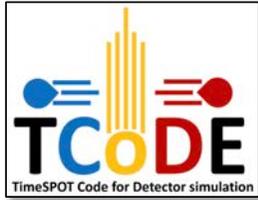
About tails

Tails basically depend on:

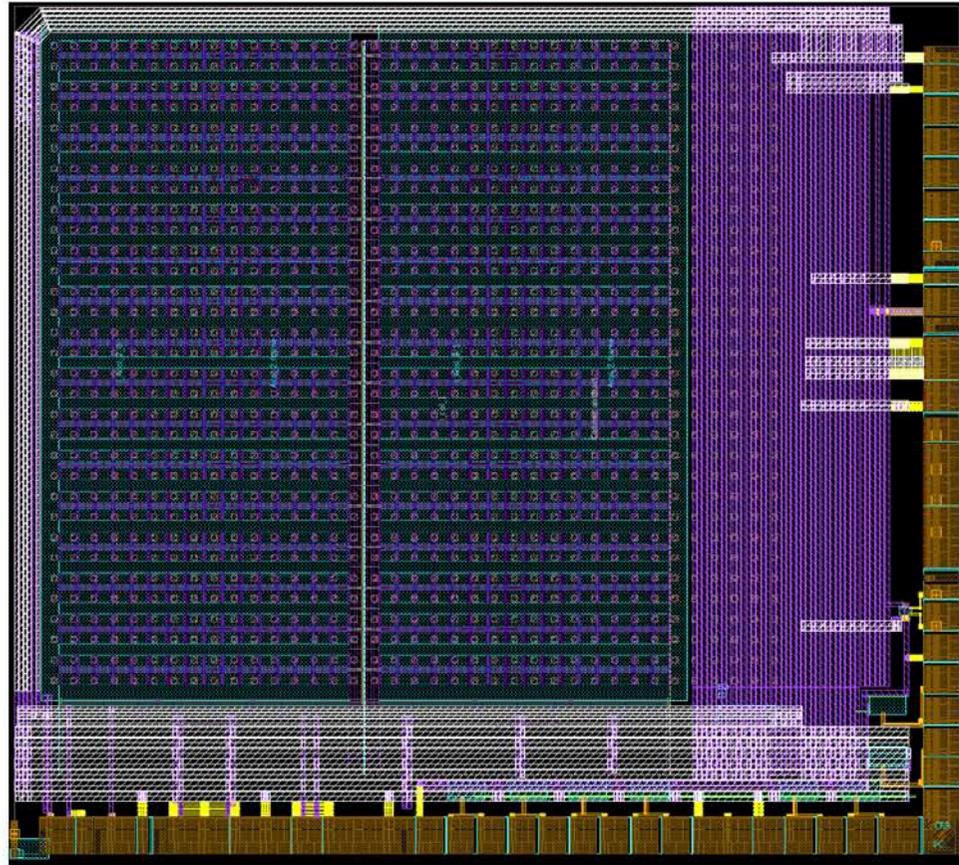
1. e/h asymmetry in drift velocities before saturation regime
2. Low-field spots

They can be suppressed by increasing the E field and reducing the pixel size
 Please notice that such **tails are irrelevant in a multi-hit tracking system**





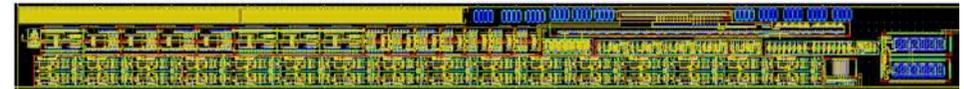
Induced current signals convoluted with Front-end transfer function



PLL and End-of-Column logic

Timespot1 architecture and read-out speed:

- 2 blocks, 512 channels each
- Floorplan at the block level is TSV ready
- Analog column (bias and services) on the left, digital read-out on the right
- I²C access for configuration and status read-out
- Each block transmits data from 512 channels via 4 LVDS drivers (640 MHz DDR each → 1.28 Gb/s)
- 10 Gb/s maximum data throughput
- Custom read-out protocol
- Average event rate per each LVDS driver is 26 MHz
- Full ASIC average rate ≈ 213 MHz (≈ 200 kHz/channel, dominated by output interface)



PLL 40 MHz → 640 MHz

Simulation of TDC data extraction by EoC logic

