VERTEX 2020 Virtual !

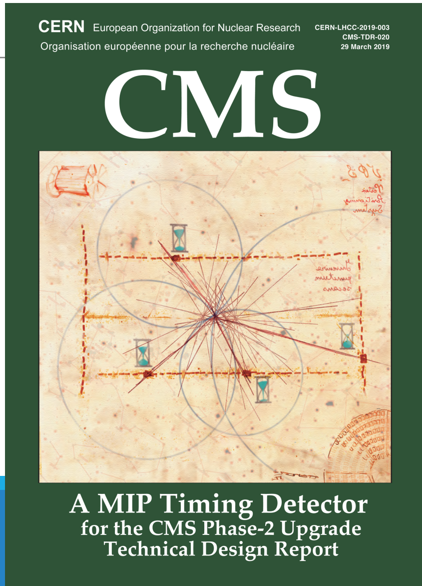
October 5-8, 2020

INFN
Istituto Nazionale di Fisica Nucleare

Precision Timing with the CMS MTD Endcap Timing Layer for HL-LHC

V. Sola – INFN Torino

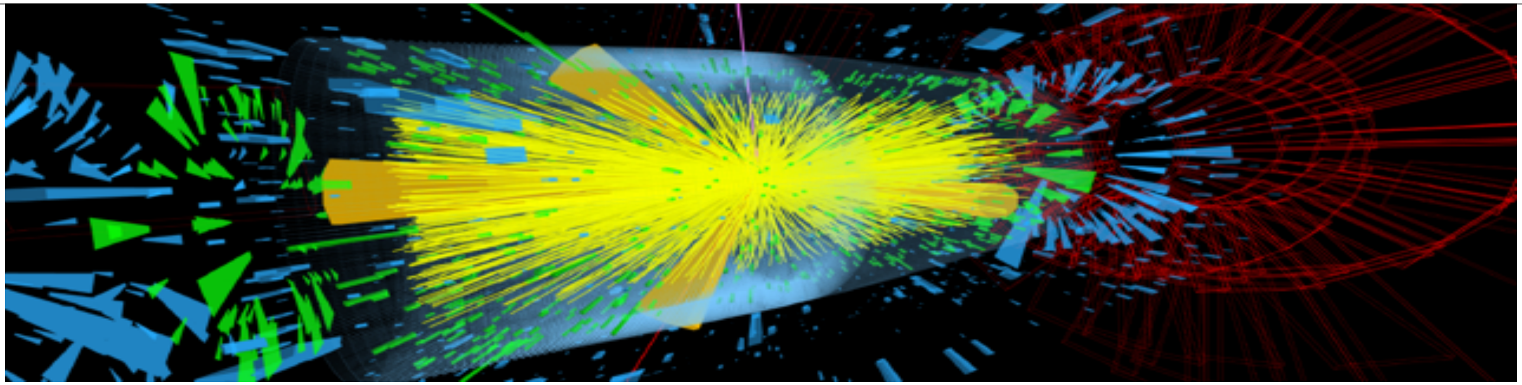
on behalf of the CMS Collaboration


CERN European Organization for Nuclear Research
Organisation européenne pour la recherche nucléaire
CERN-LHCC-2019-003
CMS-TDR-020
29 March 2019

CMS

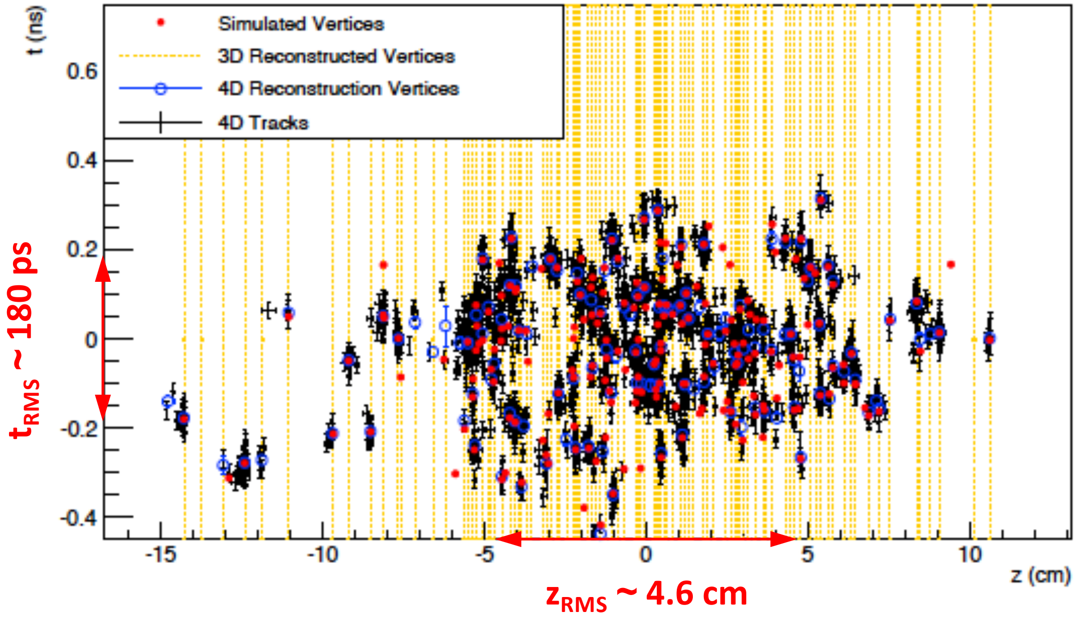
A MIP Timing Detector for the CMS Phase-2 Upgrade Technical Design Report

A HERMETIC MIP TIMING DETECTOR FOR CMS



Simulation of a VBF H → ττ in 200 pile-up pp collisions

200 pp vertices



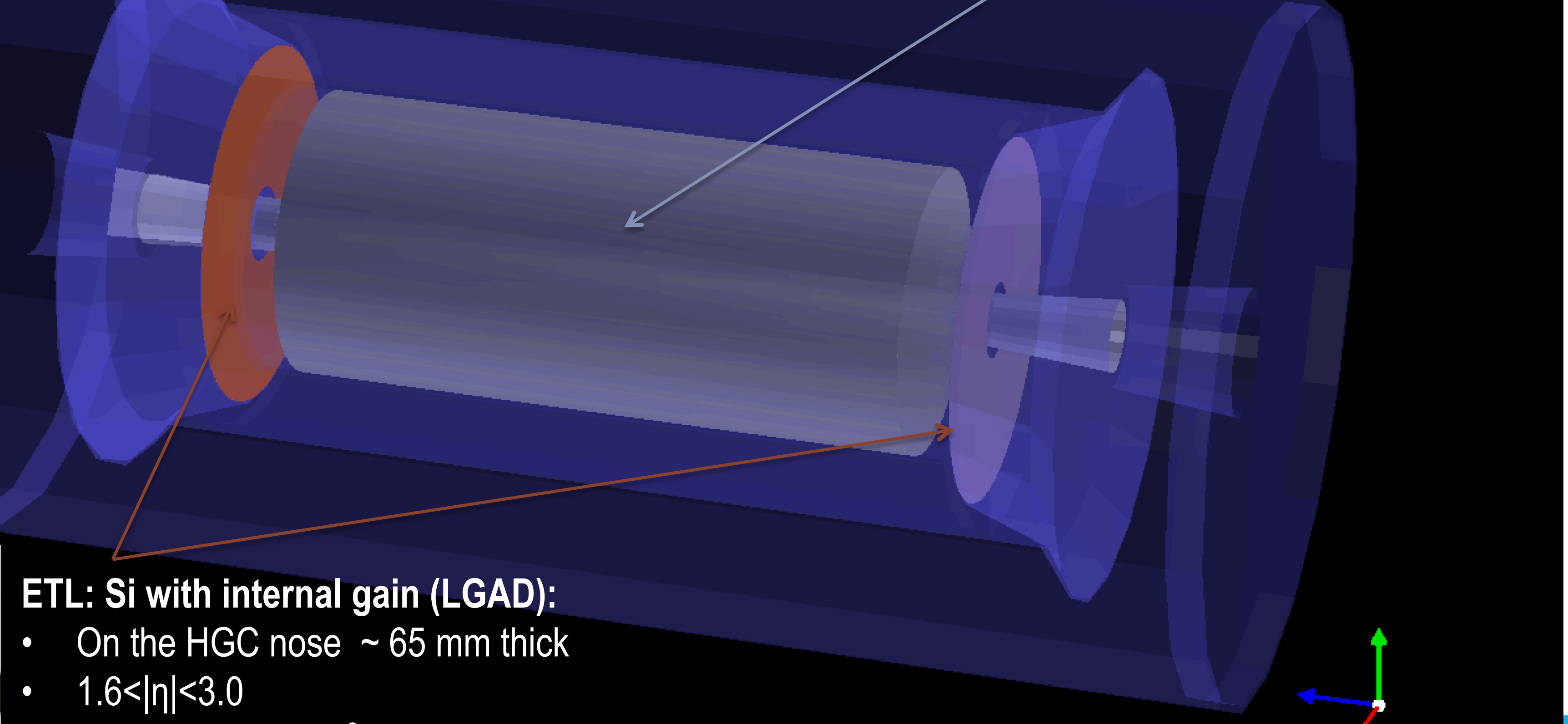
Conditions at HL-LHC very challenging
→ at the edge of tracker performances

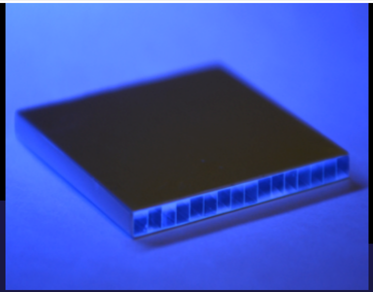
Spread of ~180 ps in time collisions
→ slices of 35 ps will reject a factor of 5 more pile-up

⇒ With 35 ps time resolution, instances of vertex merging are reduced from 15% in space to 1% in space-time, as in LHC operation

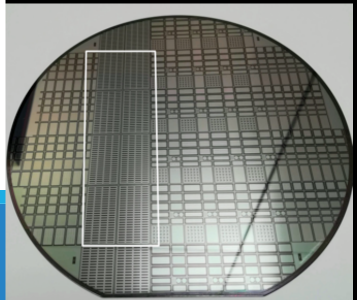
MIP TIMING DETECTOR AT A GLANCE

A vertex detector in time domain at 3 m from the interaction point





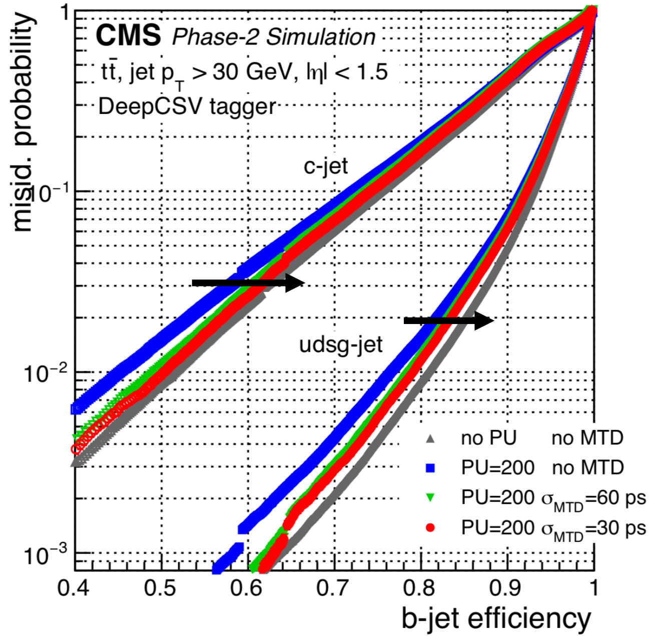
BTL: L(Y)SO bars + SiPM readout:
- TK/ ECAL interface ~ 45 mm thick
- $|\eta|<1.45$ and $p_T>0.7$ GeV
- Active area ~38 m^2 ; 332k channels
- Fluence at 3 ab^{-1}: $2x10^{14}$ n_{eq}/cm^2

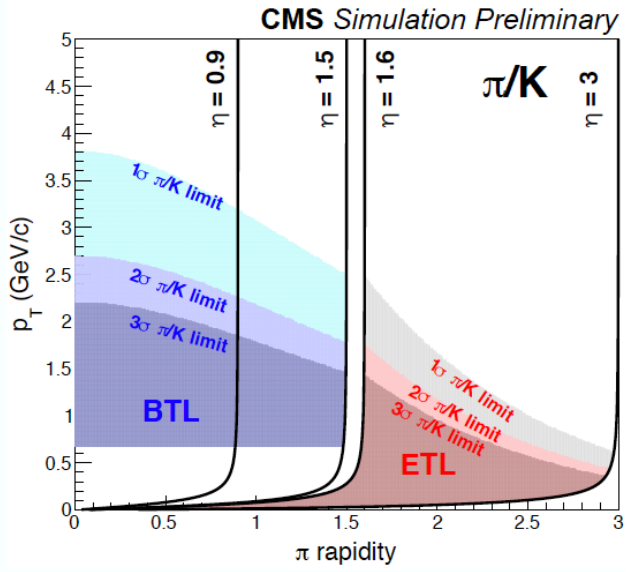


ETL: Si with internal gain (LGAD):
- On the HGC nose ~ 65 mm thick
- $1.6<|\eta|<3.0$
- Active area ~14 m^2; ~8.5M channels
- Fluence at 3 ab^{-1}: up to $2x10^{15}$ n_{eq}/cm^2

PHYSICS IMPACT

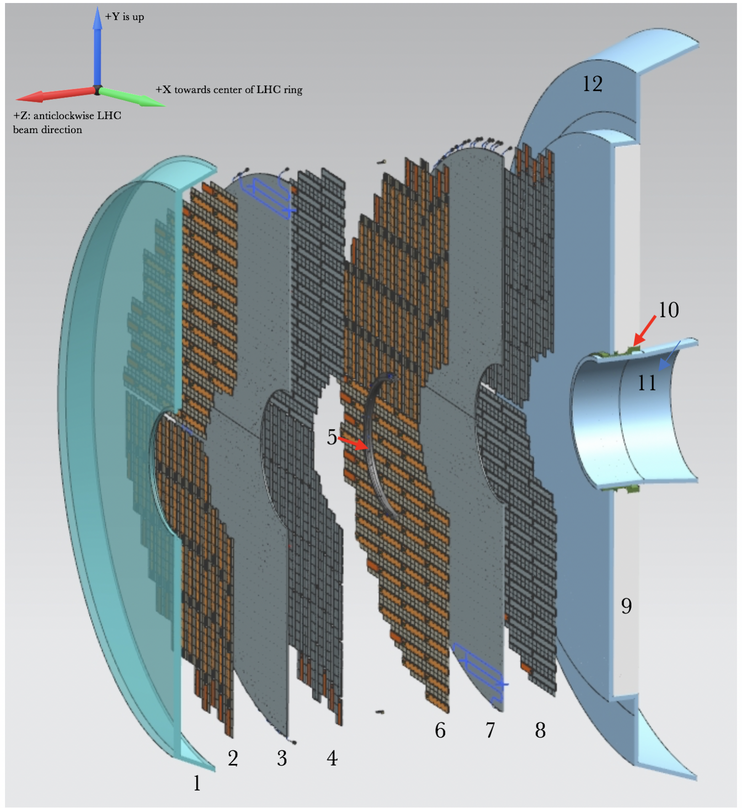
- **Improved reconstruction performance**
  - higher b-tagging efficiency
  - improvement in identification and isolation of photons and leptons
  - better rejection of fake jets due to pile-up
- **10%-20% gain in S/√B for many Higgs decay channels**
  → +20-30% effective luminosity
- **Velocity measurement (TOF) for low p_T hadrons**
  → better π/K and K/p discrimination
- **4D vertex reconstruction of primary and secondary vertices**
  → provides a close kinematic for Long Lived Particles decaying within MTD





THE ENDCAP TIMING LAYER – ETL

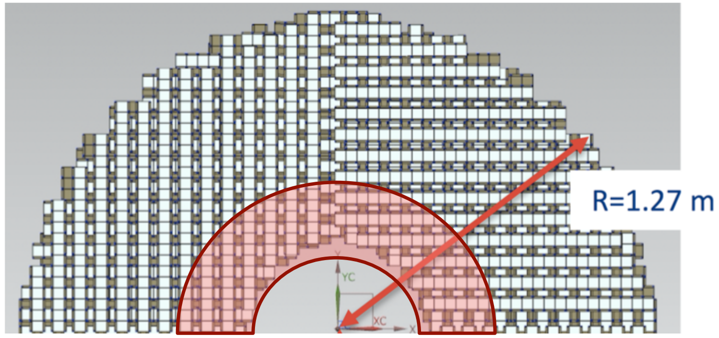
- Two disks of LGAD sensors per side
  - two measurements needed for target time resolution
  - double-sided sensor layers for large geometrical acceptance (85%/disk)
- For $\mathcal{L}_{int}$ = 3000 fb^{-1}, expected fluence ranges from 1.5×10^{14} n_{eq}/cm^2 to 1.6×10^{15} n_{eq}/cm^2 at high $|\eta|$
- Designed to be removable in case of needed maintenance/repairs during technical stops



Less than 8×10^{14} n_{eq}/cm^2 for 70% of ETL

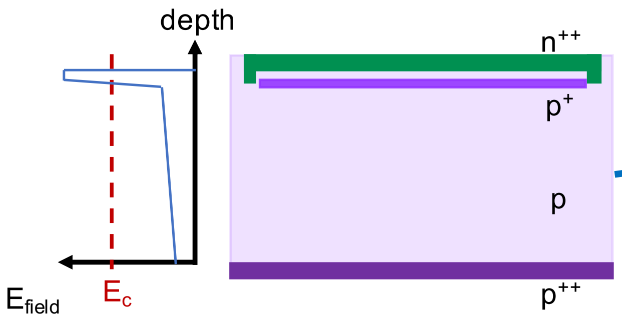
Less than 1×10^{15} n_{eq}/cm^2 for 88% of ETL

Only 12% of ETL above 1×10^{15} n_{eq}/cm^2

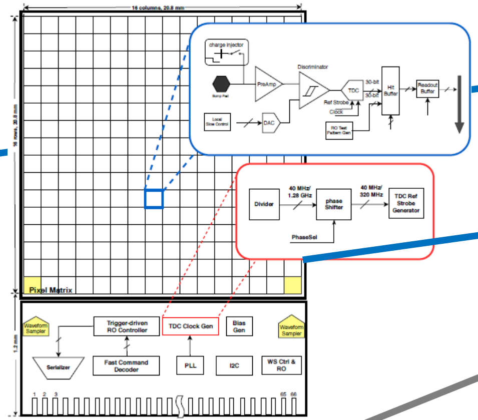


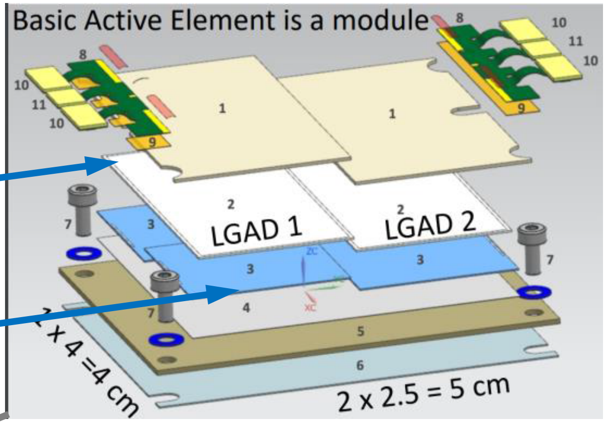
THE ETL DESIGN

LGAD sensors – 16×32 array, 1.3×1.3 mm² pixels



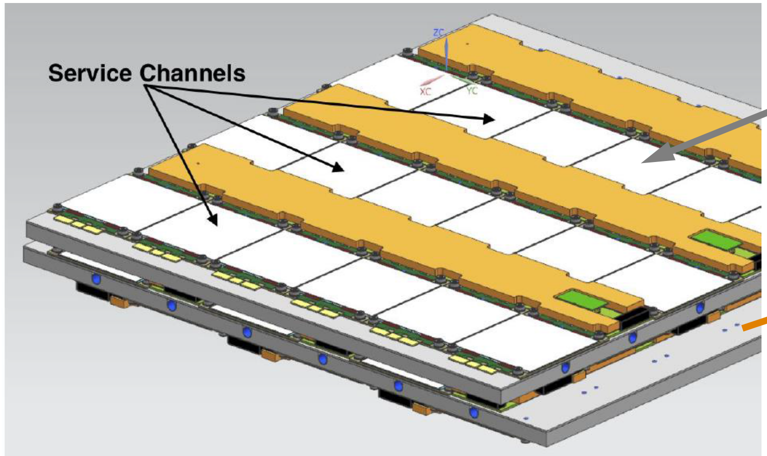
16×16 pixel ETROC bump-bonded to LGAD

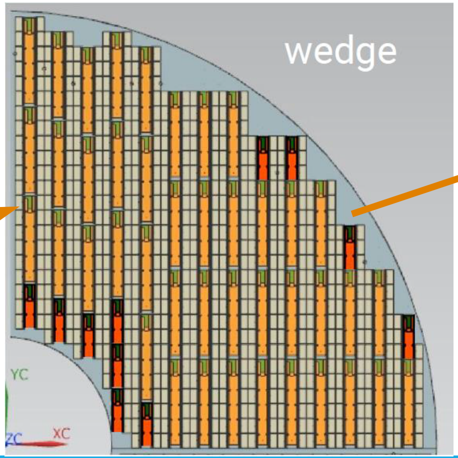


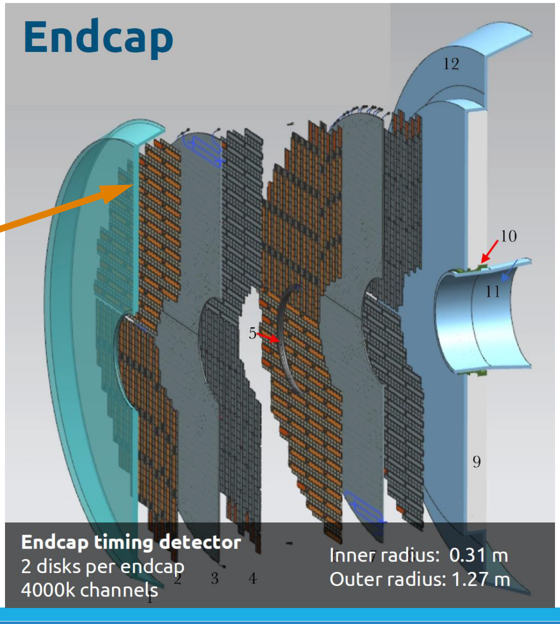


Module with 2 sensors & 4 ASIC

Support disk equipped on both sides

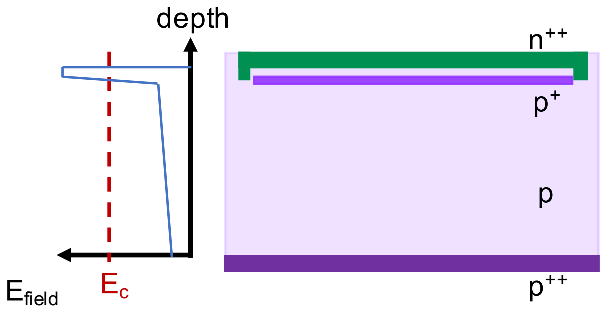


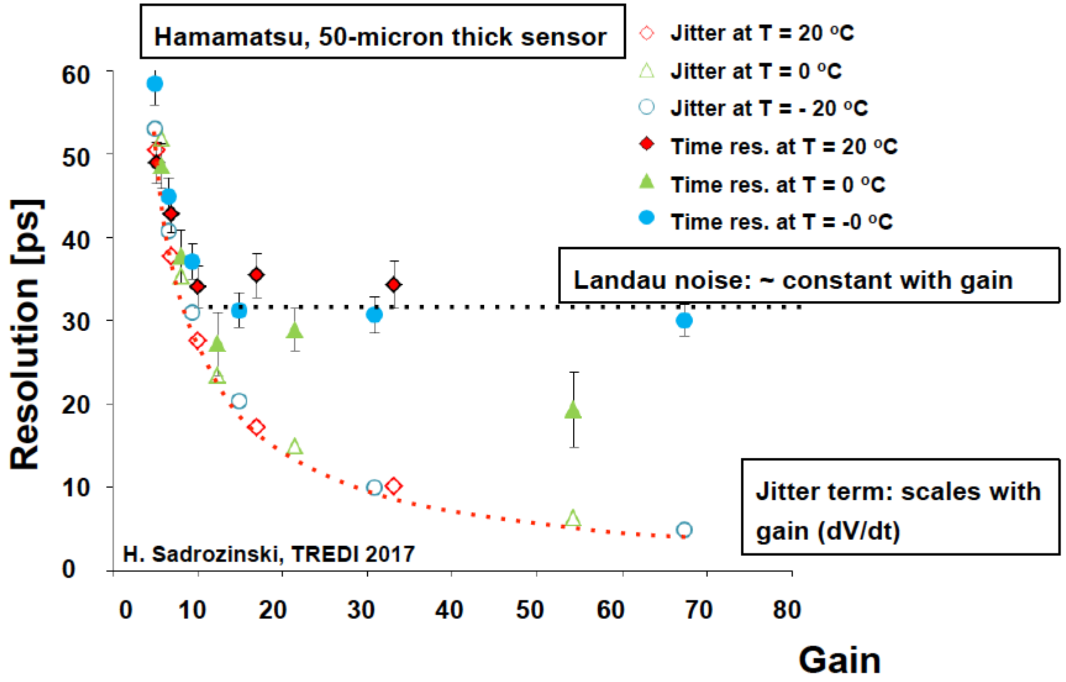




ETL SENSORS

- **50 µm thick planar silicon sensors based on Low-Gain Avalanche Diode (LGAD) technology**
  - charge multiplication for $E \gtrsim 300$ kV/cm
  - gain layer through p-type implant
  - signal gain ~ 10-30
- **Sensor requirements**:
  - small pad capacitance
    → pad size ~ few mm²
  - large production yield
    → limited size sensors
  - good radiation tolerance
  - optimize no-gain region between pixels
    → maximize fill factor while maintaining pad isolation to maximize efficiency





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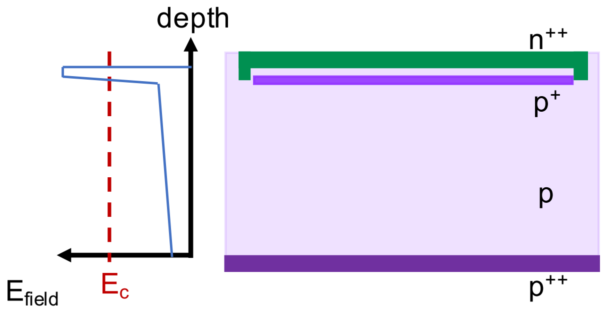


➢ **Sensor requirements**:
- ▻ small pad capacitance
  $\longrightarrow$ pad size ~ few mm^2
- ▻ large production yield
  $\longrightarrow$ limited size sensors
- ▻ good radiation tolerance
- ▻ optimize no-gain region between pixels
  $\longrightarrow$ maximize fill factor while maintaining pad isolation to maximize efficiency

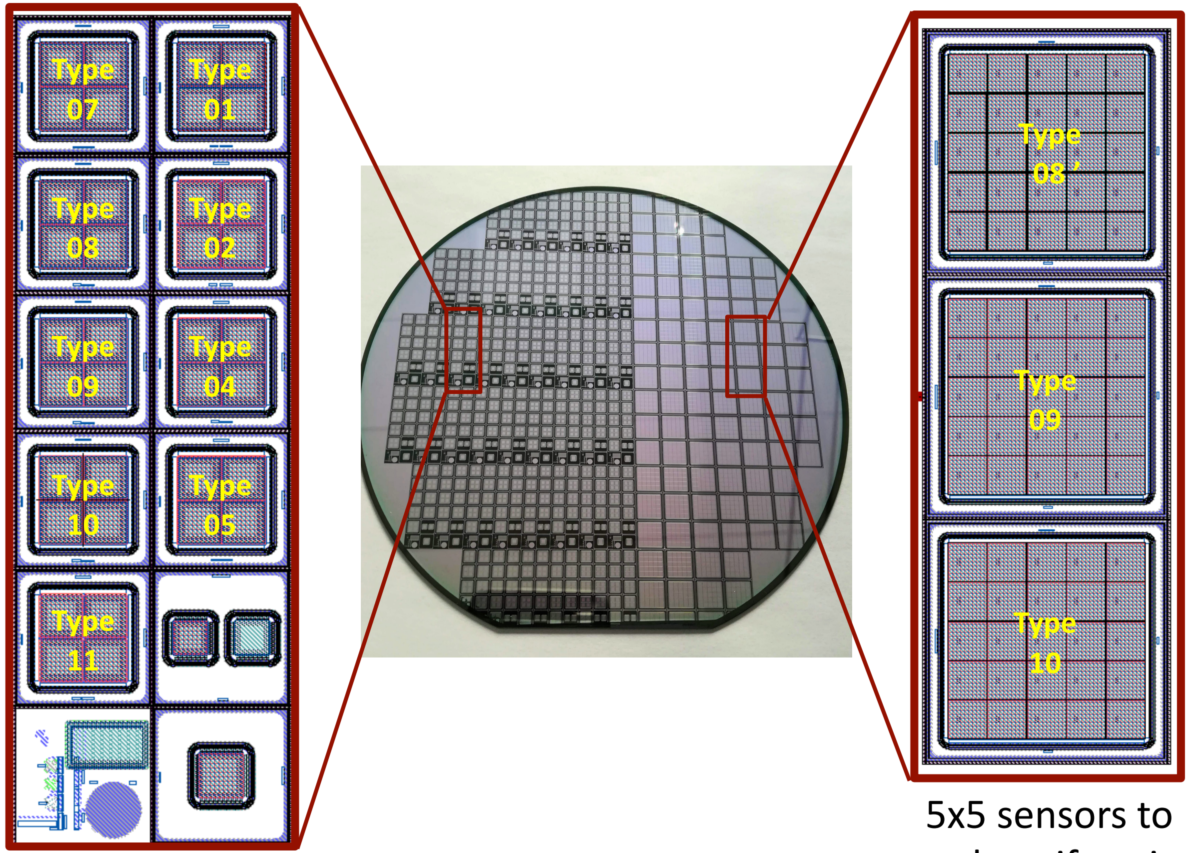
FBK & HPK released new LGAD sensor productions on Summer 2020 to accomplish ETL requirements

2 NEW PRODUCTIONS FOR ETL – FBK UFSD3.2

17 wafers to finalise studies on **gain layer design** and **inter-pad strategy**

- ▻ 2 different wafer thickness: 45 and 55 μm
- ▻ 2 different gain layer depth: shallow and deep
- ▻ 4 different split of gain layer dose
- ▻ 4 different splits of Carbon co-implanted in the gain layer volume, to enhance rad-hardness
- ▻ 2 different strategies of gain layer annealing (diffusion)
- ▻ 9 different inter-pad strategies (types)

[Ref for types: https://indico.cern.ch/event/855994/contributions/3637004/]



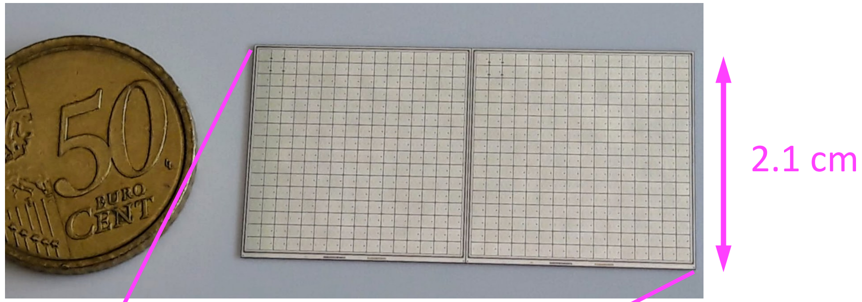
2x2 sensors to investigate different inter-pad strategies

5x5 sensors to study uniformity

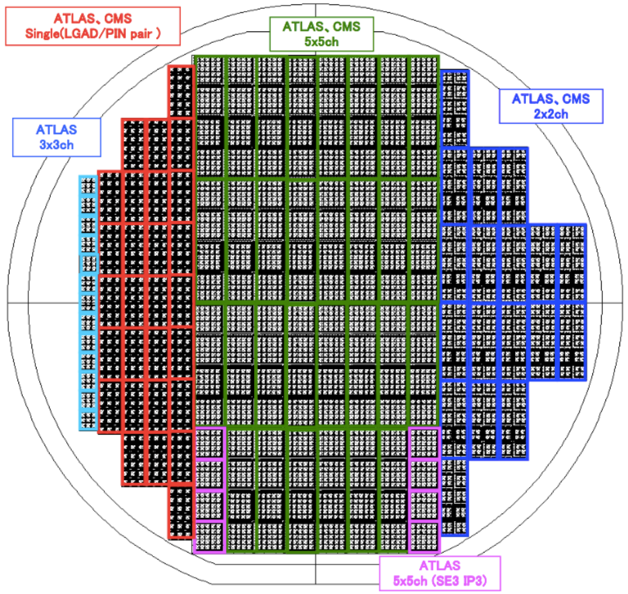
2 NEW PRODUCTIONS FOR ETL – HPK2

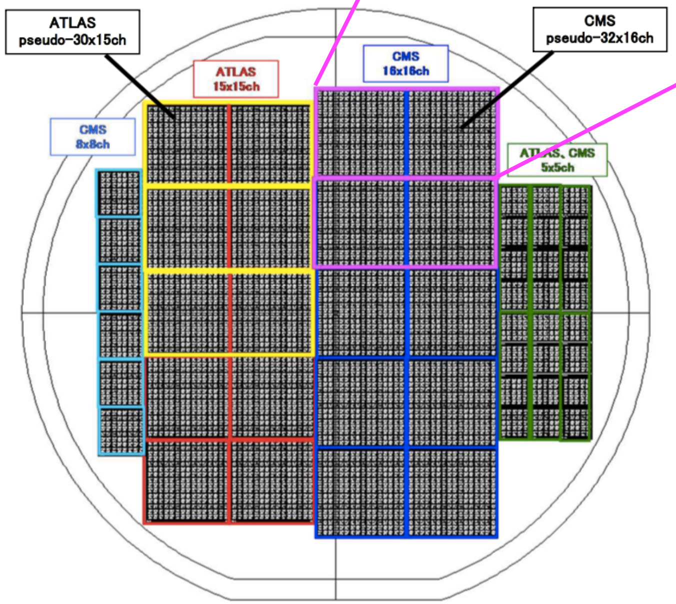
13 wafers to finalise studies **inter-pad strategy** and **uniformity of the production**

- ▻ 2 different wafer layout: small and large
- ▻ 4 different split of gain layer – deep design
- ▻ 2 different edge strategies: 300 and 500 μm
- ▻ 4 different inter-pad strategies: IP3, IP4, IP5, IP7



Small sensors to study inter-pad design, edge termination, and radiation resistance

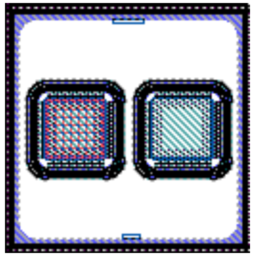




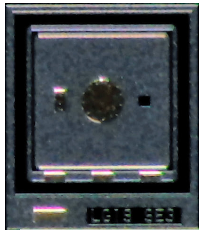
Large sensors,

to study uniformity

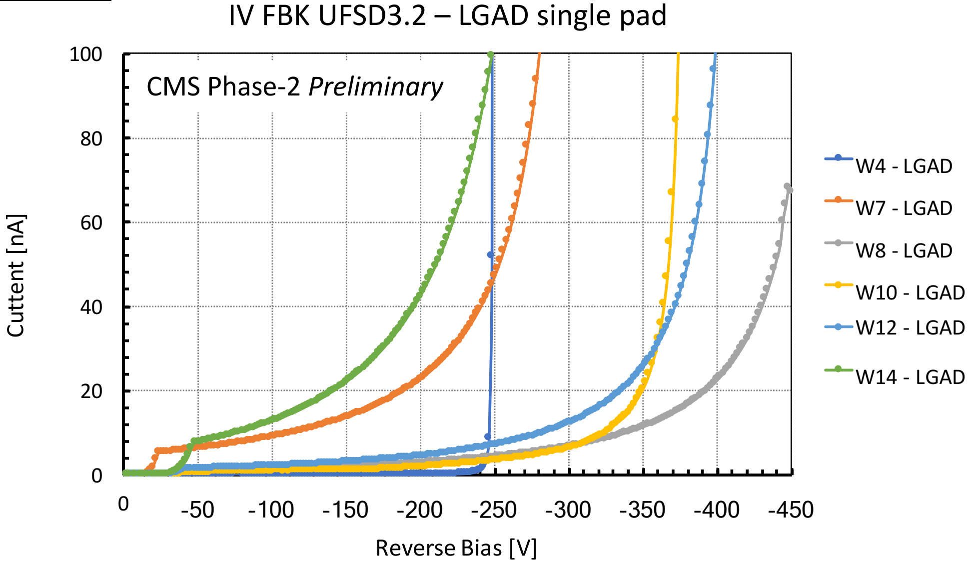
FBK & HPK – IV Characterization

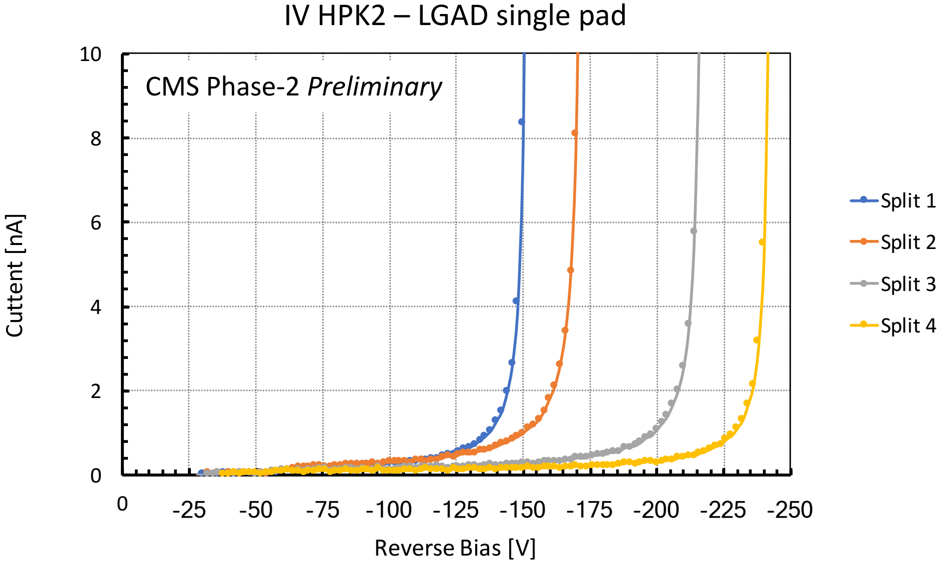


IV from FBK UFSD3.2
LGAD single pad



IV from HPK2
LGAD single pad



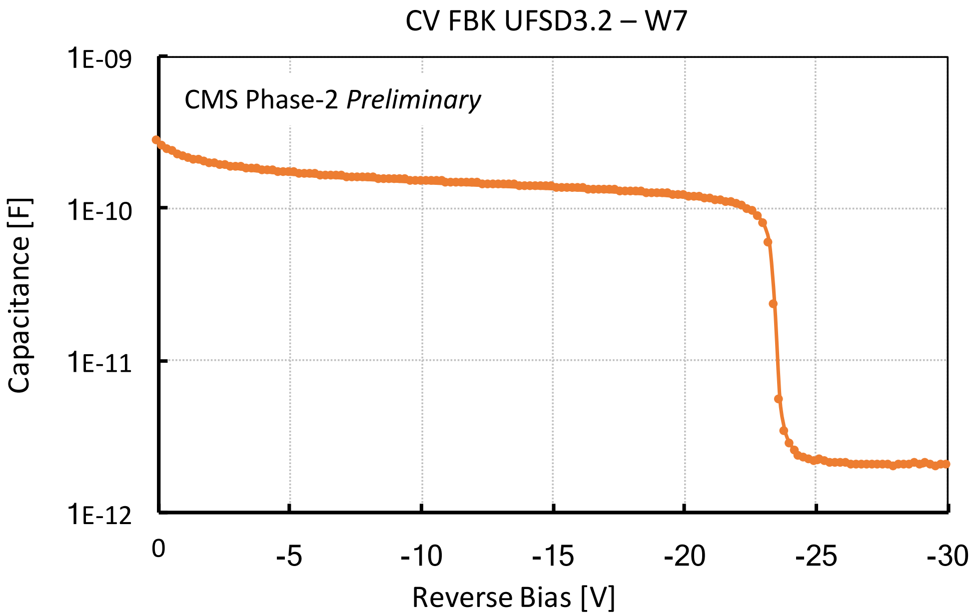


- 3 wafers show optimal gain behaviour (W4, W7, W14)
- 3 gain layer doping can be increased (W8, W10, W12)
- W4 has lower dark current, due to a lower dose of implanted C

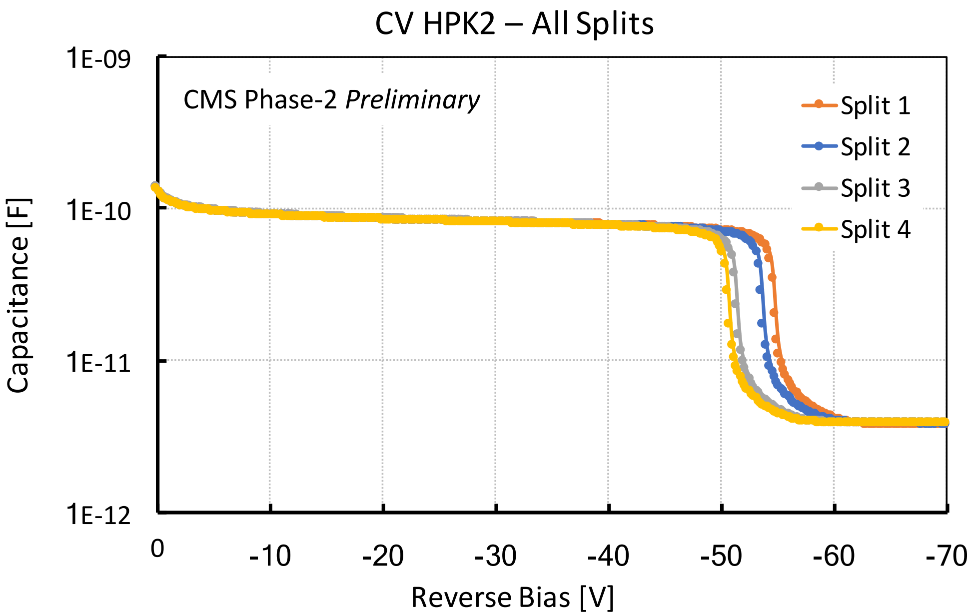
- Breakdown at 200-250 V ideal for ETL design
- Split 3 shows good gain behaviour
- Split 4 is target for ETL timing requirements

FBK & HPK – CV Characterization

CV from FBK UFSD3.2 W7
LGAD single pad



CV from HPK2
All splits



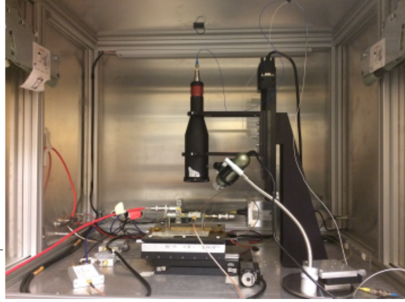
W7 is the replica of W5 from the FBK UFSD3 production, reference wafer on UFSD3.2

→ Gain layer depletion at about 23 V, as expected

Depletion Voltage of the gain layer between 51 and 56 V

→ About 10% difference from split 1 to 4

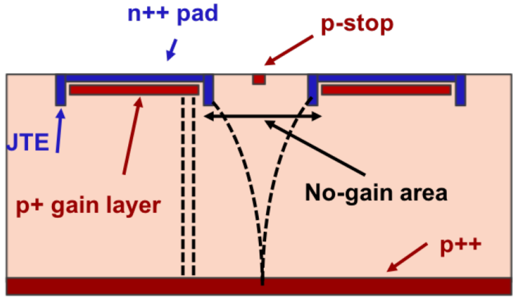
FBK & HPK – Inter-pad Width



Inter-pad width measured using Transient Current Technique (TCT)

The width is obtained scanning two adjacent pads and measuring the collected charge as a function of the laser position

The measured width is a convolution of a step function with a Gaussian ⇒ an s-curve



Type 10 FBK UFSD3.2 & IP3 HPK2 result in a fill factor of ~ 90%

Inter-pad: wider no-gain regions have higher breakdown voltage

→ **Find a compromise between high V_{BD} and narrow inter-pad width**

Inter-pad FBK UFSD3.2
CMS Phase-2 *Preliminary*

Type (IP)	Measured [μm]
4	35-40
8	40-45
10	65-70

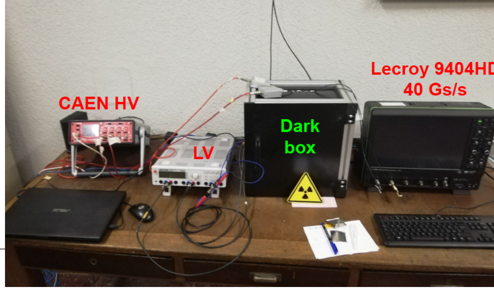
Inter-pad HPK2 – Split 4
CMS Phase-2 *Preliminary*

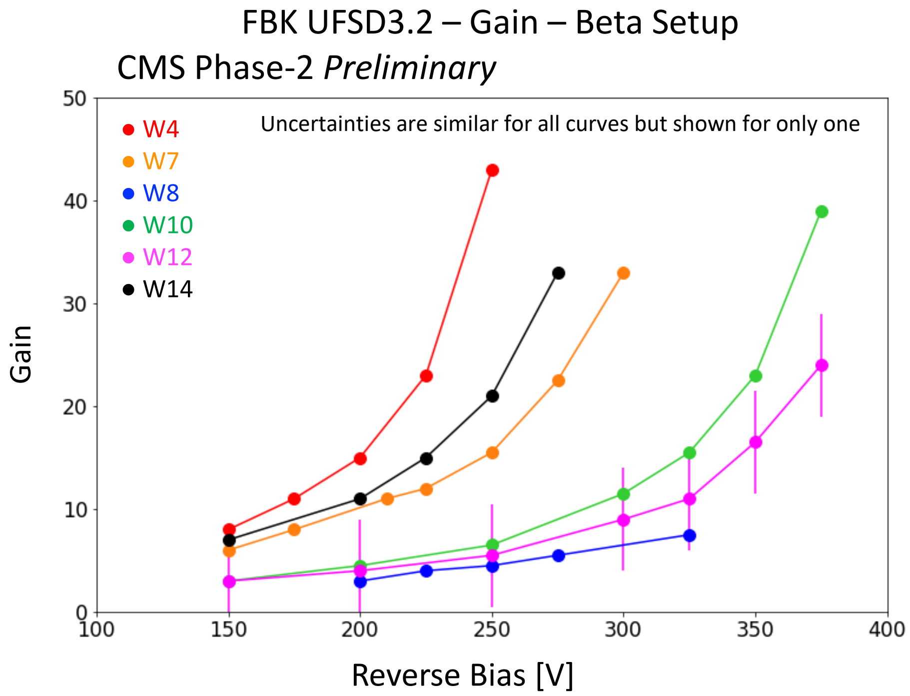
Type (IP)	Measured [μm]
IP3	64
IP4	91
IP5	102
IP7	120

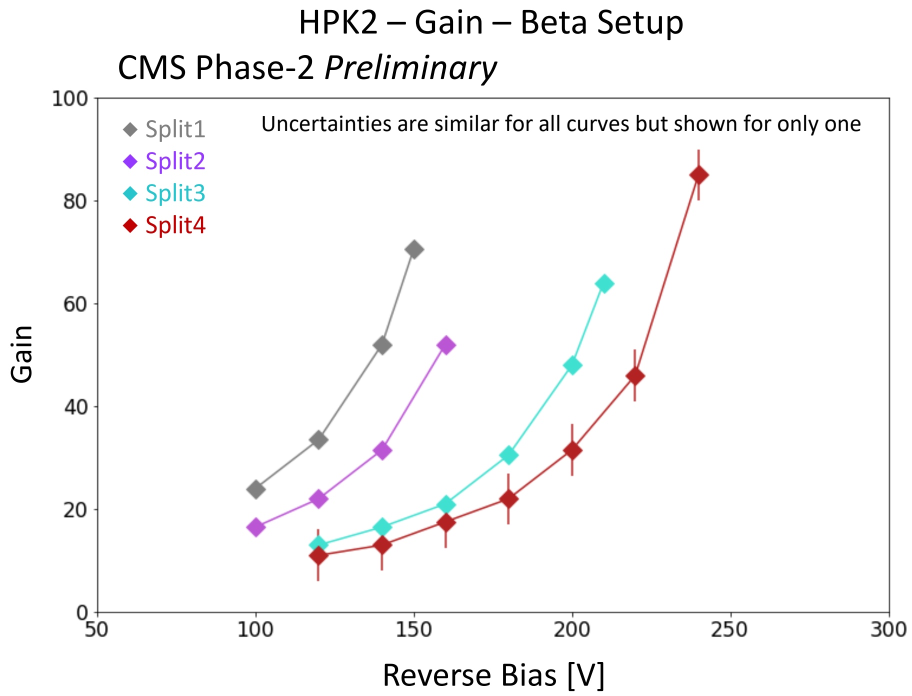
TCT laser parameters:
- f = 1 kHz
- Charge ~ 6 MIP
- Laser spot = 10 μm

Measurements performed at RT
Systematic uncertainty = 5 μm

FBK & HPK – Gain with Bias







Gain = LGAD-charge / PiN-charge

LGAD charge [fC] = area [pWb] / 4700 Ω (4700 Ω is the UCSC board trans-impedance)

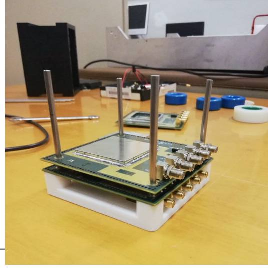
PiN charge assessed assuming nominal thickness (0.65 fC for 55 µm, 0.54 fC for 45µm thickness)

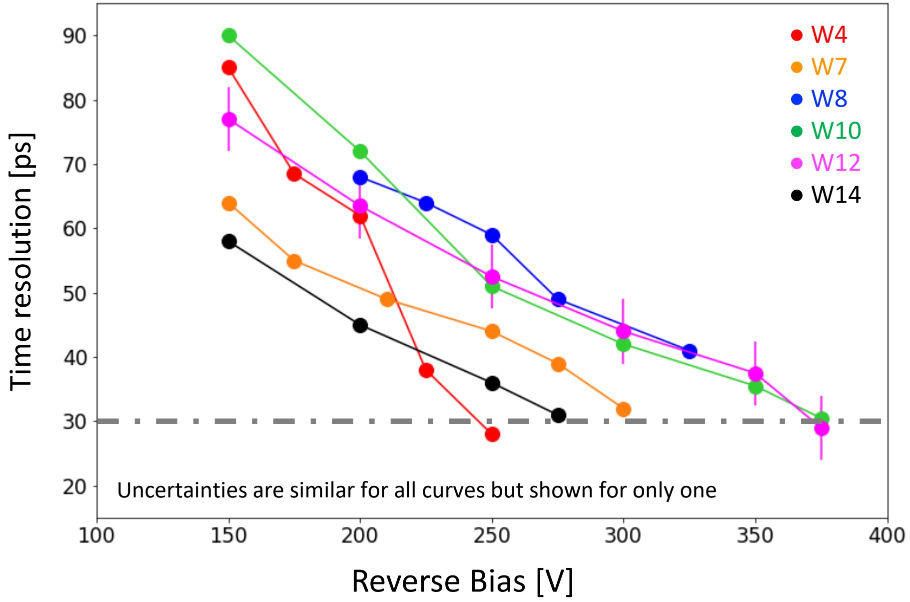
RMS noise = 1.2 - 1.6 mV @ room temperature

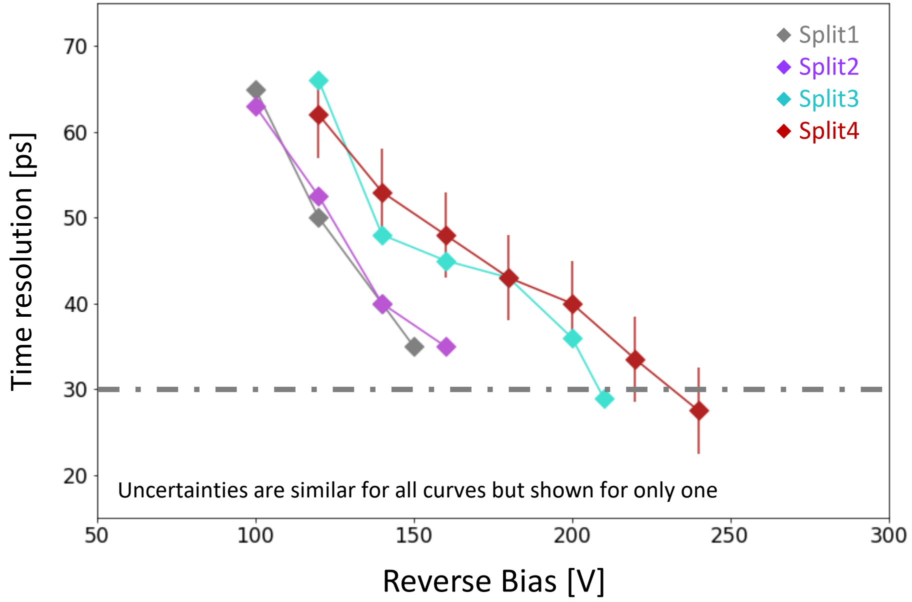
Error bars of ± 5 on gain measurement are shown for FBK W12 and HPK Split 4

All sensors have good gain and low noise

FBK & HPK – Time Resolution with Bias





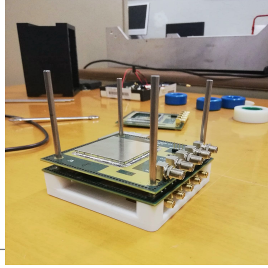


Trigger: HPK3.1 1x3 mm^2 LGAD single pad, σ_t = 33ps @230V
All measurement are performed at room temperature

Error bars of ± 5 ps on σ_t measurement are shown for FBK W12 and HPK Split 4

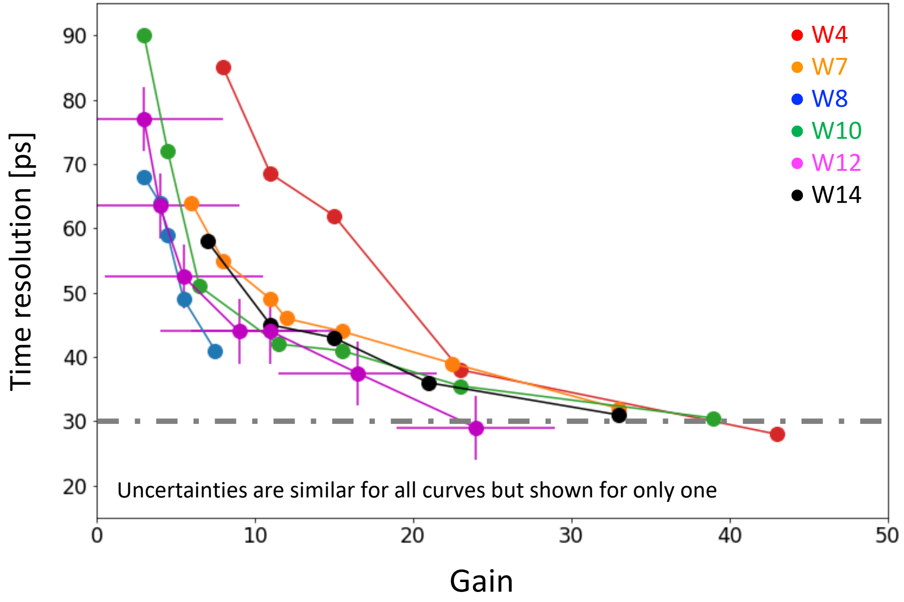
→ **For a given bias, more doped wafers show better time resolution as they have higher electric field to trigger impact ionization**

FBK & HPK – Time Resolution with Gain



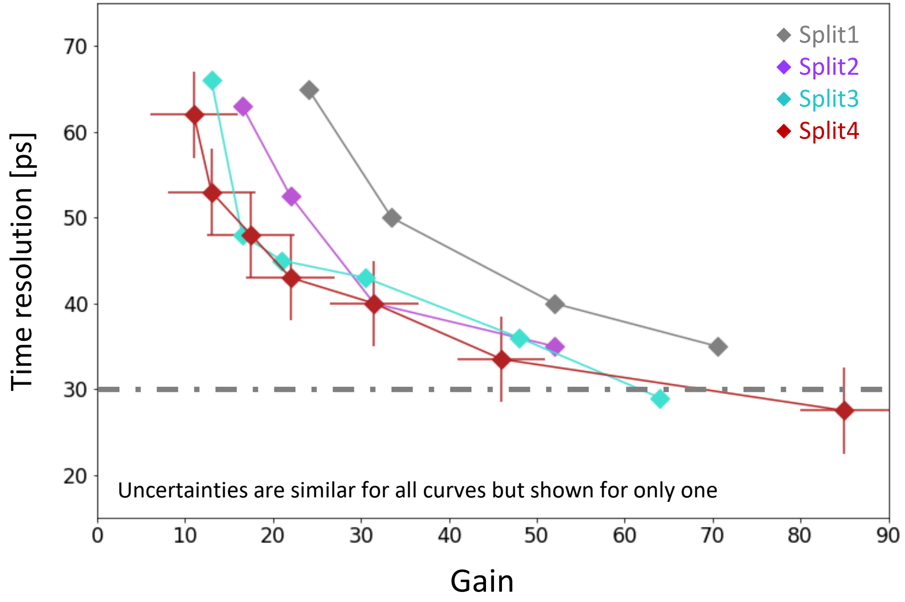
FBK UFSD3.2 – σ_t with Gain – Beta Setup

CMS Phase-2 *Preliminary*



HPK2 – σ_t with Gain – Beta Setup

CMS Phase-2 *Preliminary*



Trigger: HPK3.1 1x3 mm^2 LGAD single pad, σ_t = 33ps @230V

All measurement are performed at room temperature

Error bars of ± 5 on gain and ± 5 ps on σ_t measurements are shown for FBK W12 and HPK Split 4

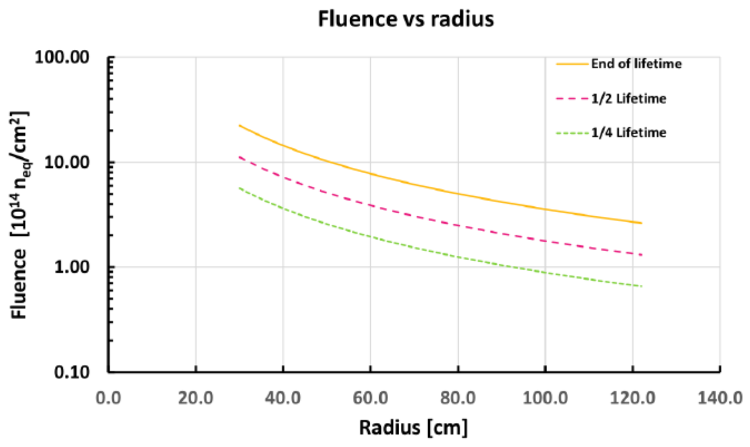
For a given gain, less doped wafers show better time resolution as they are operated at higher bias
→ Higher holes drift velocity results in better dV/dt

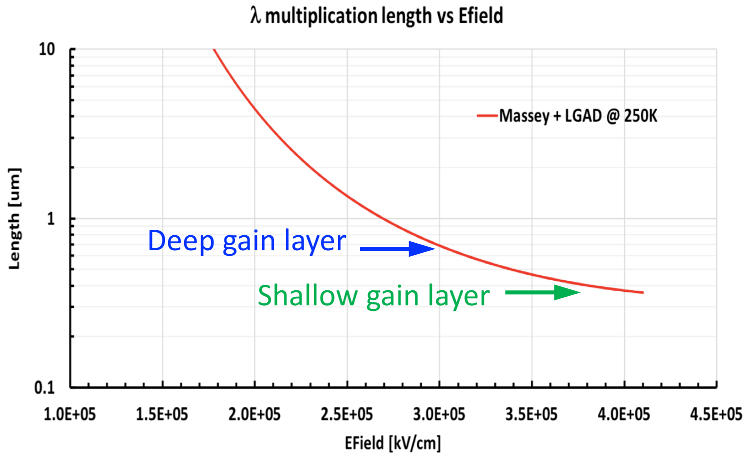
ETL RADIATION TOLERANCE

Different strategies have been adopted to mitigate radiation effects on LGAD sensors:

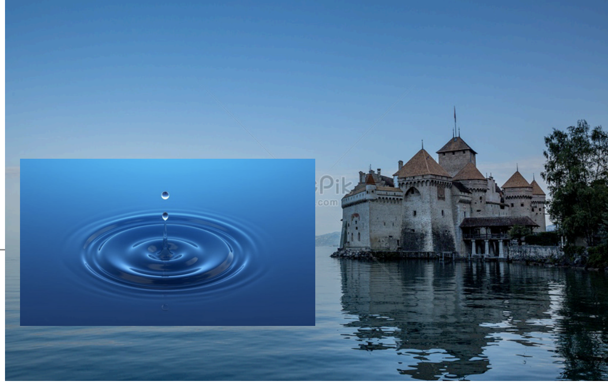
- Carbon atoms co-implanted in the gain layer volume halves the acceptor removal due to radiation
  [M. Ferrero el al., doi:10.1016/j.nima.2018.11.121]
- Deep gain layer design improves the capability of V_{bias} to recover the electric field that has been lost due to acceptor removal
  [N. Cartiglia et al., HSTD12, Hiroshima, Japan (2019)]

Target: get **15 fC** of charge applying a
V_{bias} = 500 - 600 V at $\Phi = 1.5 \cdot 10^{15}\ n_{eq}/cm^2$
⇒ Possible to achieve σ_t ~ 30 ps till the end of life-time





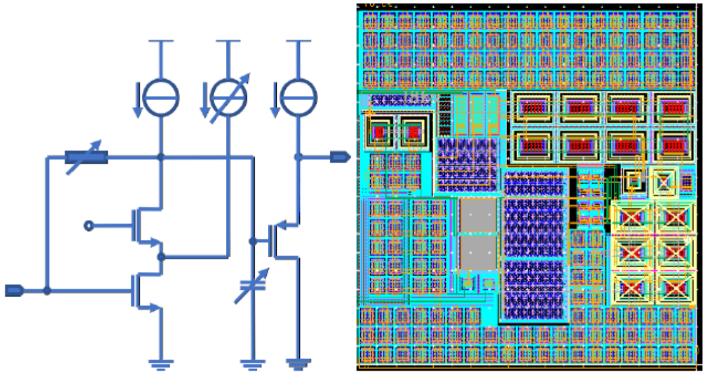
ETL READ-OUT CHIP – ETROC

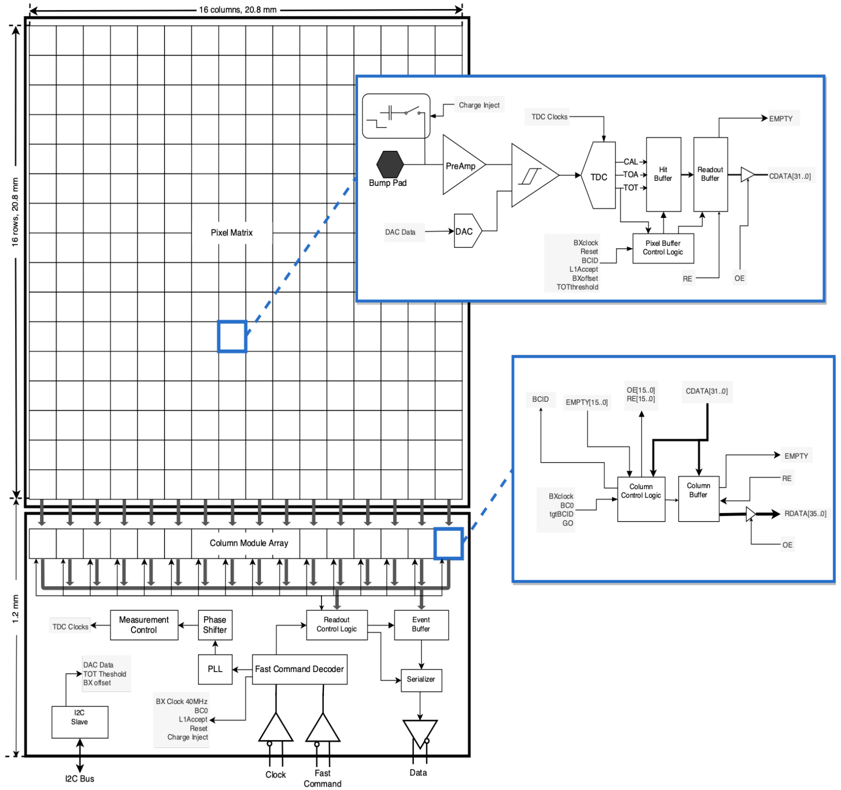


Precision determination of the arrival time of small water drop ripples, with low power < 4mW/channel

- ETROC bump-bonded to LGAD, to handle 16x16 pixels each 1.3×1.3 mm^2
- ETROC process based on TSMC 65 nm technology
- ASIC contribution to time resolution < 40ps
- Deal with small signal size (~ 6 fC, at end of operation)
- Power consumption < 1W/chip, L1 buffer latency: 12.5 µs
- Single TDC for both time of arrival and time over threshold
- Flexible low & high-power amplifier modes

Simplified schematic and layout of ETROC preamplifier

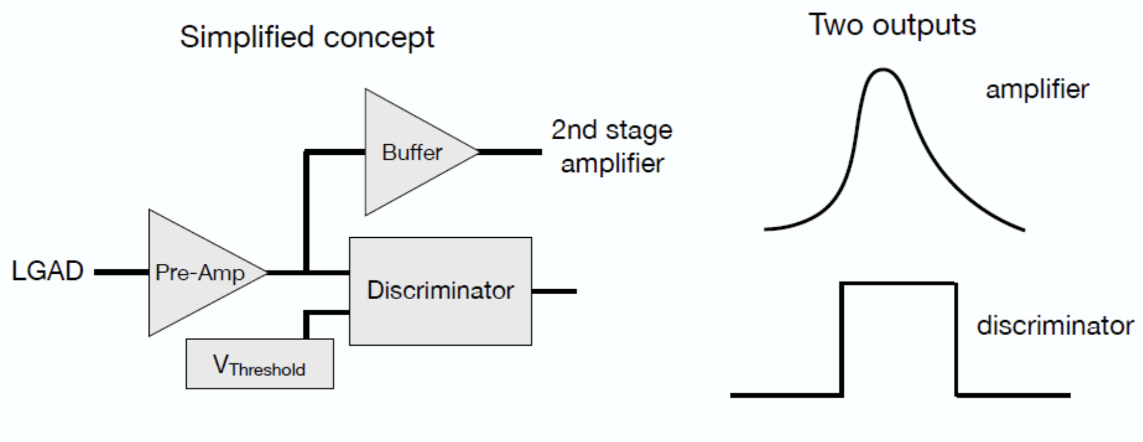


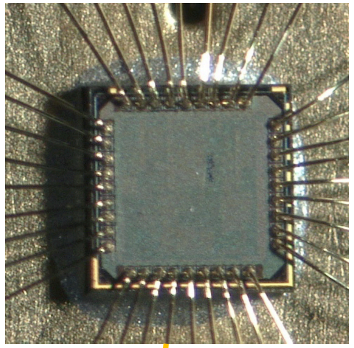


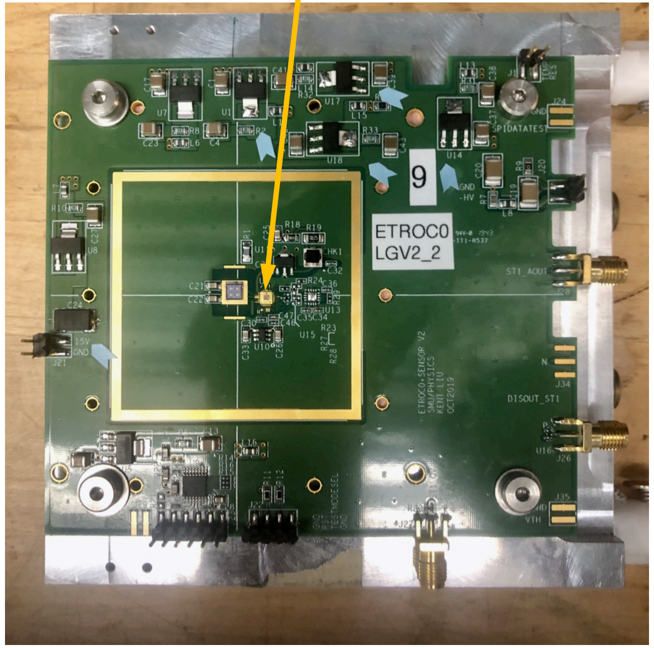
ETROC0

Two data paths designed in ETROC0

- Submitted in Dec. 2018
- Analog front-end
- Tests by far confirmed functionality
- First round beam test early 2020, both data paths tested
  - → *Amplifier output* recorded through internal buffer and external 2nd stage amplifier
  - → *Discriminator output* to study contributions to time resolution from sensor due to Landau fluctuations, and pre-amp & discriminator jitter – design goal σ_t < 50 ps

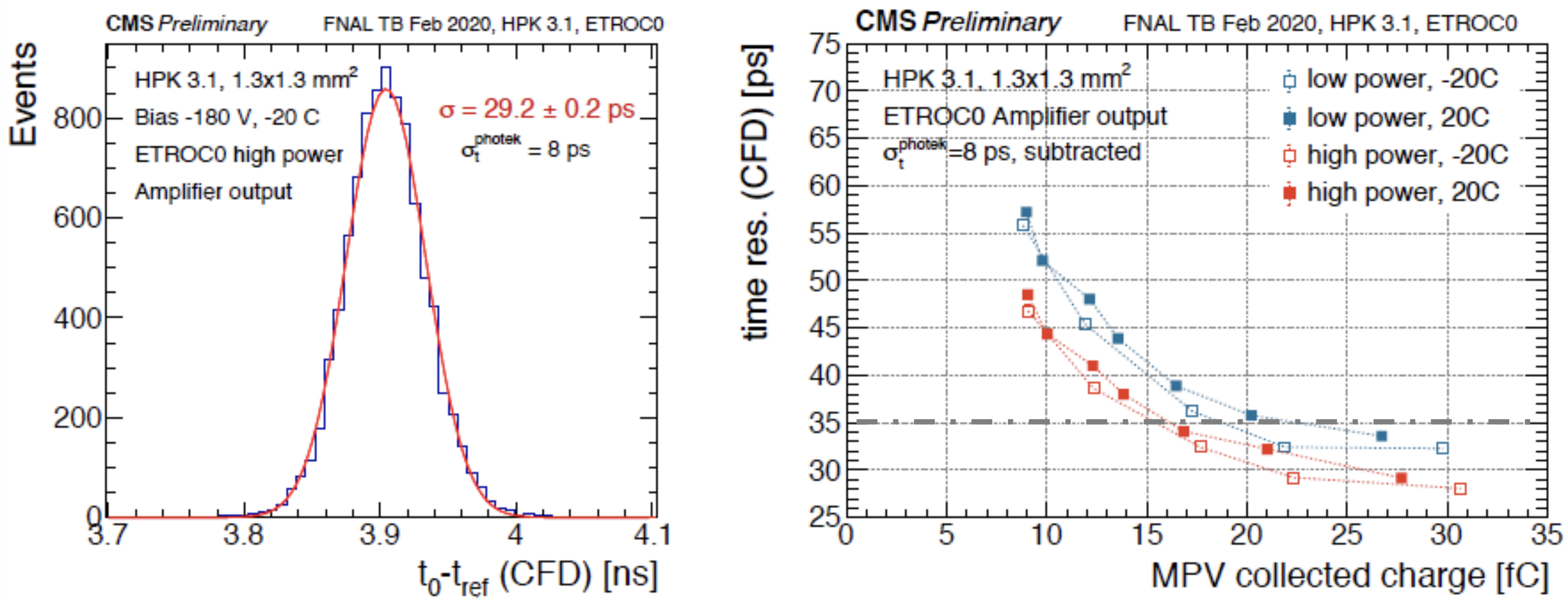






ETROC0 – Amplifier Time Resolution

- Beam test at Fermilab facility
- Timestamp measured with constant fraction threshold of 20%
- Right plot has time reference contribution subtracted

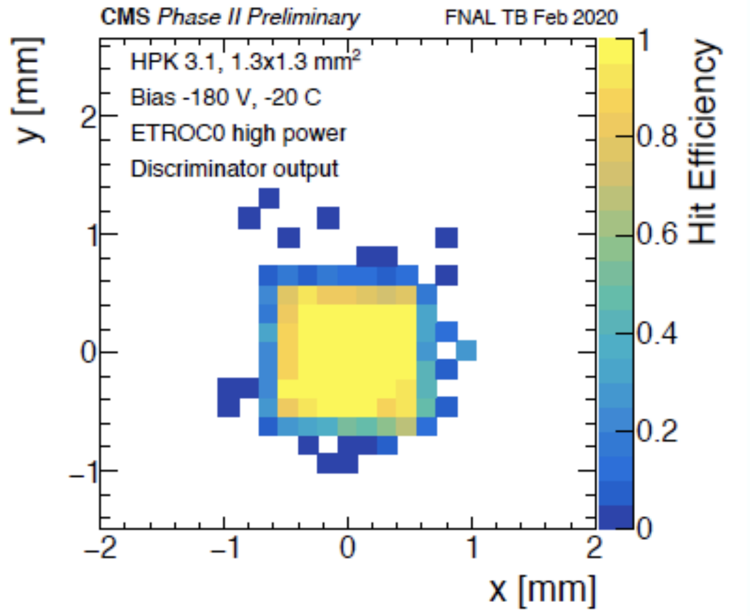


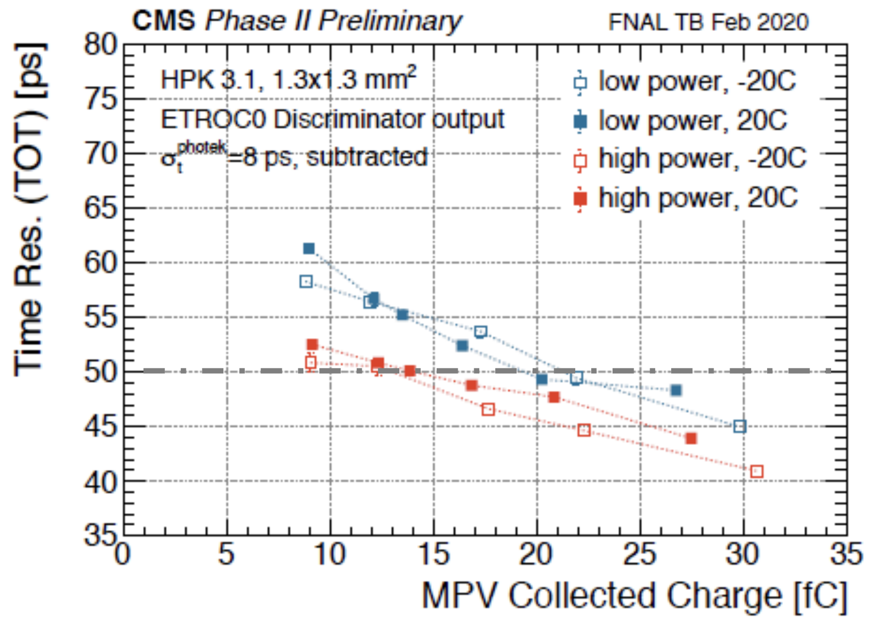
Achieved 30-35 ps time resolution for pre-rad sensors operating above 20 fC

High power mode 5-10% better time resolution than low power

ETROC0 – Discriminator Time Resolution

- Beam test at Fermilab facility
- Time resolution = $\sigma(t_0 - t_{ref}$ after ToT correction)
- Contribution from time reference is subtracted





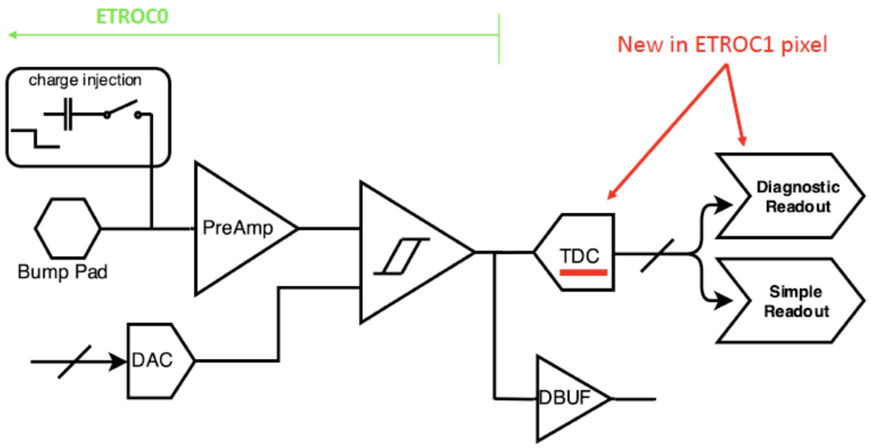
For pre-rad sensors operating above 20 fC ⟶ time resolution of 40-50 ps with 100% efficiency

⟹ Results compatible with design target of 50 ps per hit

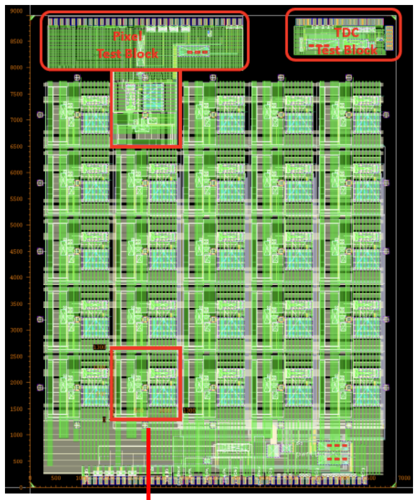
ETROC1

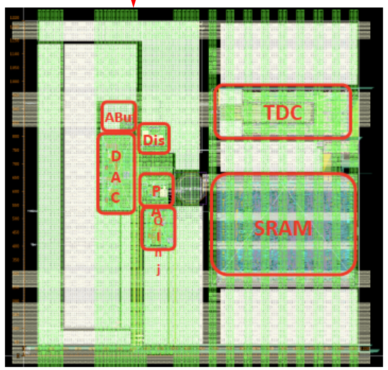
ETROC1 include a TDC brand new design (low power)

- ▻ Submitted in Aug. 2019
- ▻ 4×4 pixel array with full front-end including TDC
- ▻ TDC block works well
- ▻ ETROC0 is used directly in ETROC1
- ▻ TDC requirements
  - → TOA bin size ≲ 30ps, TOT bin size ≲ 100ps
  - → Lower power highly desirable – ETROC TDC design goal < 0.2mW per pixel



ETROC1 Top Layout

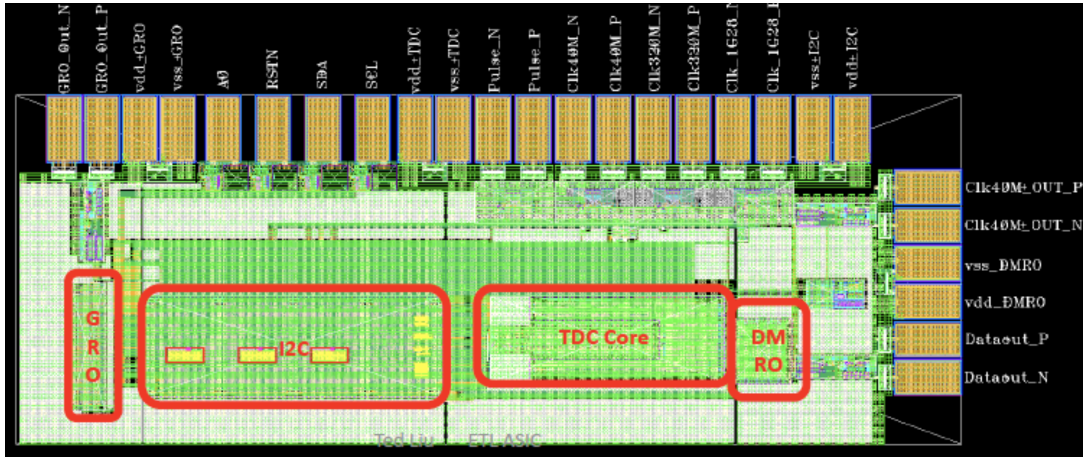


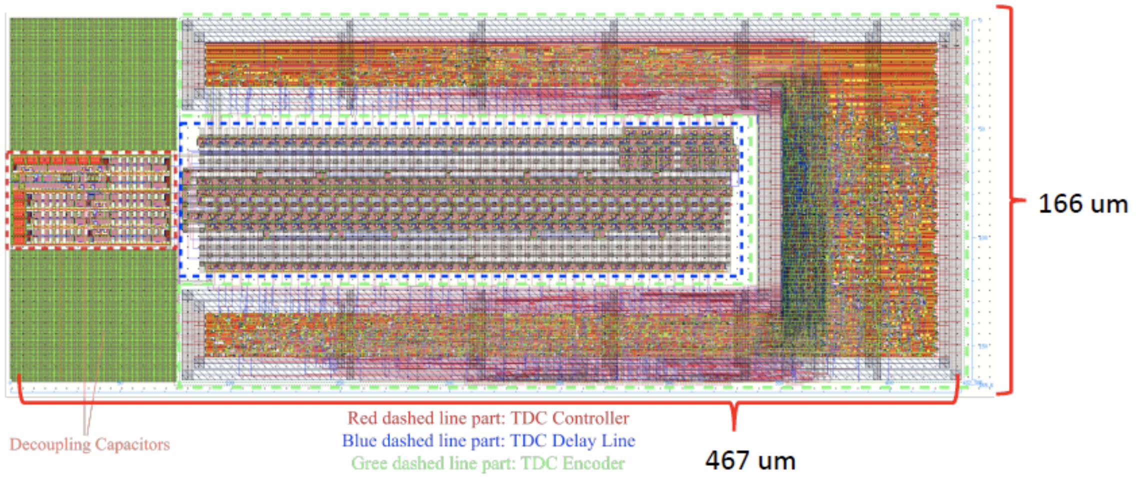


ETROC1 Single Pixel Layout

ETROC1 – TDC Resolution

The TDC has been extensively simulated and improved (~ one year development effort)

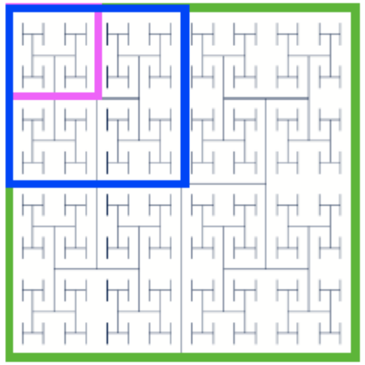




Early testing shows good performances:

- ▻ The measured average TDC bin size is 17.8 ps
- ▻ Excellent timing performance ≤ 6 ps
- ▻ Demonstrated to operate at ultra low-power < 0.1 mW

ETROC2&3 – Ongoing



ETROC0: single analog channel
ETROC1: with TDC and 4×4 clock tree
ETROC2: 8×8, or potentially 16×16, full functionality
ETROC3: 16×16 full size chip

Full-chip clock distribution design advanced
- The textbook H-tree clock distribution

Waveform sampling spec and design developed
- Single channel ADC prototype received last year → **Works well**
- The core 2.56 GS/s waveform sampler submitted in March 2020 → **Waveform sampler testing results are very good**

Much of the supporting circuitries will be based on existing design blocks in 65nm from CERN (lpGBT)

ETROC2: design in progress → **Submission in Q3 2021** (postponed due to COVID)

DAQ &Clock Distribution – Overview

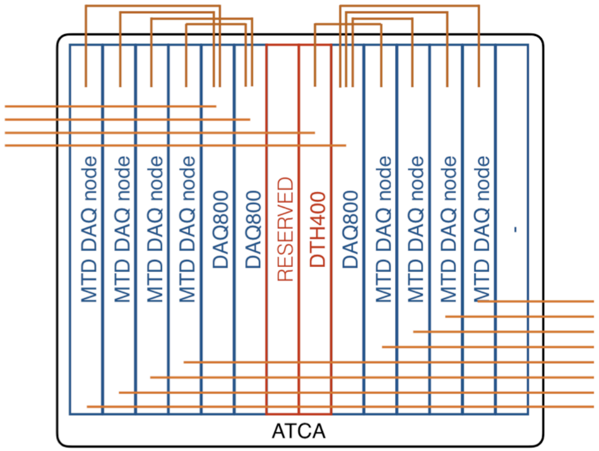
DAQ: < 0.4 Tb/s data rate at 750 kHz L1A

- ETL bi-directional links and data rate: 1600 links; < 1.5 Gb/s / link
- ATCA crates with 6+6 ETL DAQ nodes (e.g. Serenity KUP15)
  - → Being re-visited and optimized now

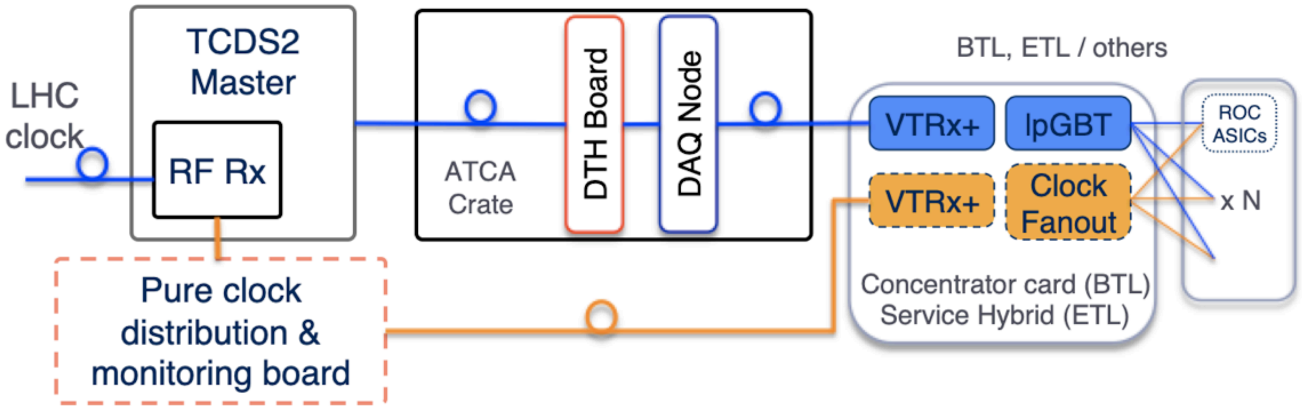
Clock: < 15 ps jitter (channel-to-channel)

- Baseline: Encoded within lpGBT links
- Risk mitigation: “Pure clock path”

Schematic of an MTD DAQ ATCA crate layout



Clock distribution tree



SUMMARY

- ➢ CMS ETL is among the first-generation precision timing detectors
- ➢ Thin double layers between the tracker and the calorimeters
- ➢ ETL is the first large-scale application of LGAD technology
  → Unprecedented size and scope for a timing detector
- ➢ Challenging front-end electronics design
  → Precision determination of the arrival time of small water drop ripples
- ➢ 30-40 ps per track resolution at HL-LHC start, < 50 ps at 3000 fb^{-1}

⇒ Exciting time ahead of us

ACKNOWLEDGEMENTS

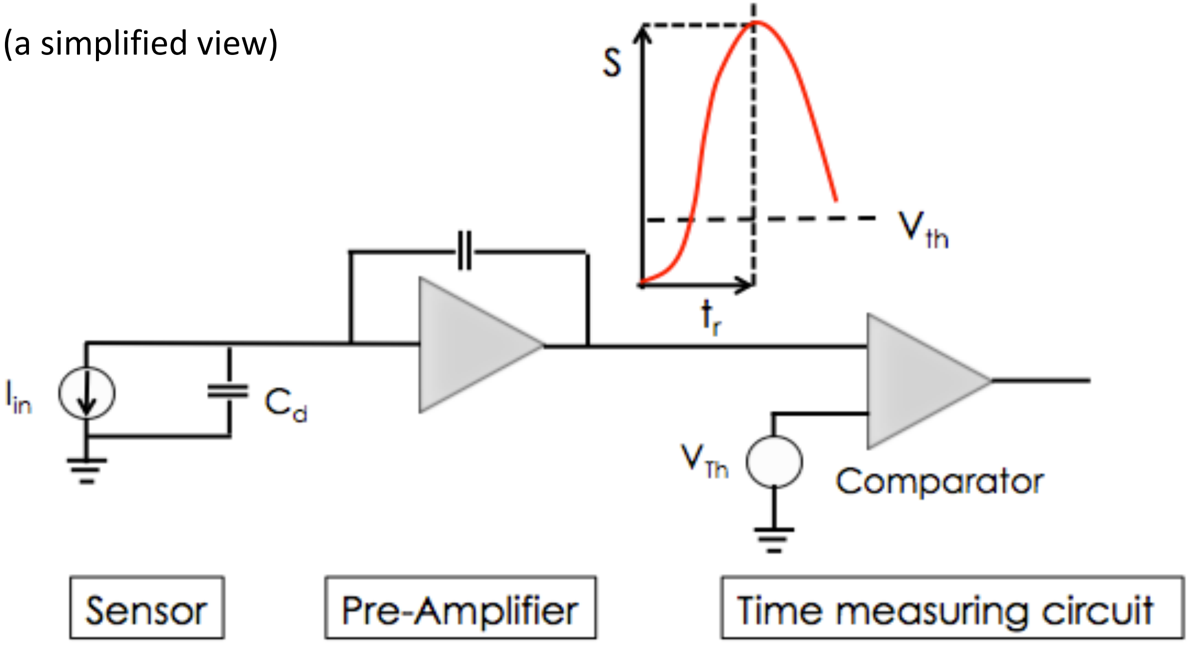
We kindly acknowledge the following funding agencies, collaborations:

- RD50, CERN
- Horizon 2020, grant UFSD669529
- AIDA-2020, grant agreement no. 654168
- MIUR, Dipartimenti di Eccellenza (ex L. 232/2016, art. 1, cc. 314, 337)
- Ministero della Ricerca, Italia, PRIN 2017, progetto 2017L2XKTJ – 4DinSiDe
- Ministero della Ricerca, Italia, FARE, R165xr8frt_fare
- INFN CSN5

BACKUP

A TIME-TAGGING DETECTOR

(a simplified view)



Time is set when the signal crosses the comparator threshold

The timing capabilities are determined by the characteristics of the signal at the output of the pre-Amplifier and by the TDC binning

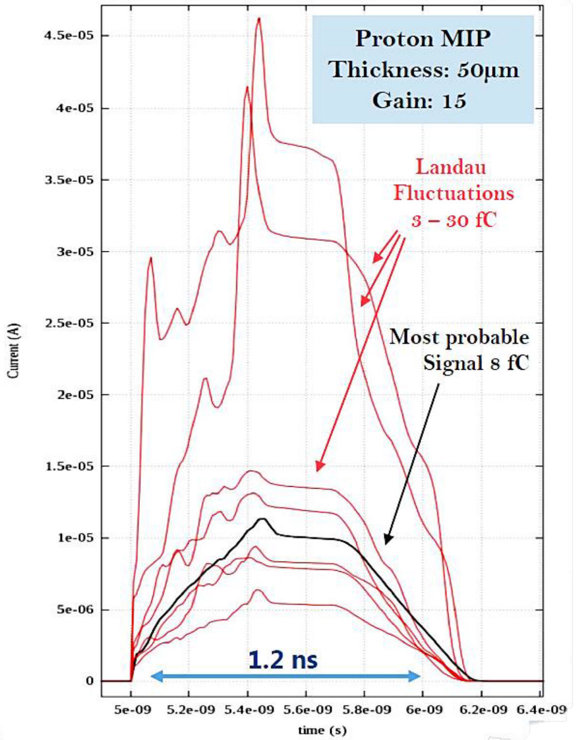
⇒ Strong interplay between sensor and electronics

FAST TIMING - THE INGREDIENTS

For a planar detector geometry $\sigma_t^2 = \sigma_{Current}^2 + \sigma_{Jitter}^2 + \sigma_{Time\,Walk}^2 + \sigma_{TDC}^2$

with a saturated velocity, the σ_t main contributors are **current fluctuations** and **jitter**

Current fluctuations are due to the physics of MIP ionization (Landau fluctuations)

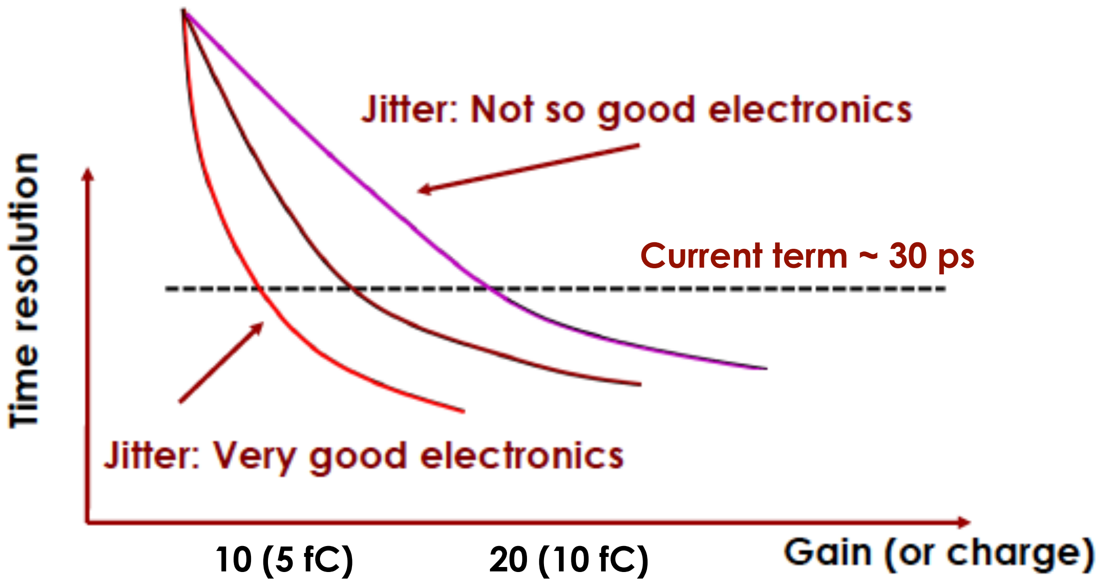


- ✎ Improves with thin sensors
- ✎ Does not depend on the gain

For 50 µm thick sensors contribute ~ 30 ps

→ **Physical limit to time resolution**

Jitter is driven by the electronics



$$\sigma_{jitter} = \frac{N}{(dV/dt)_{V_{th}}} = \frac{t_{rise}}{S/N}$$

SHOT NOISE

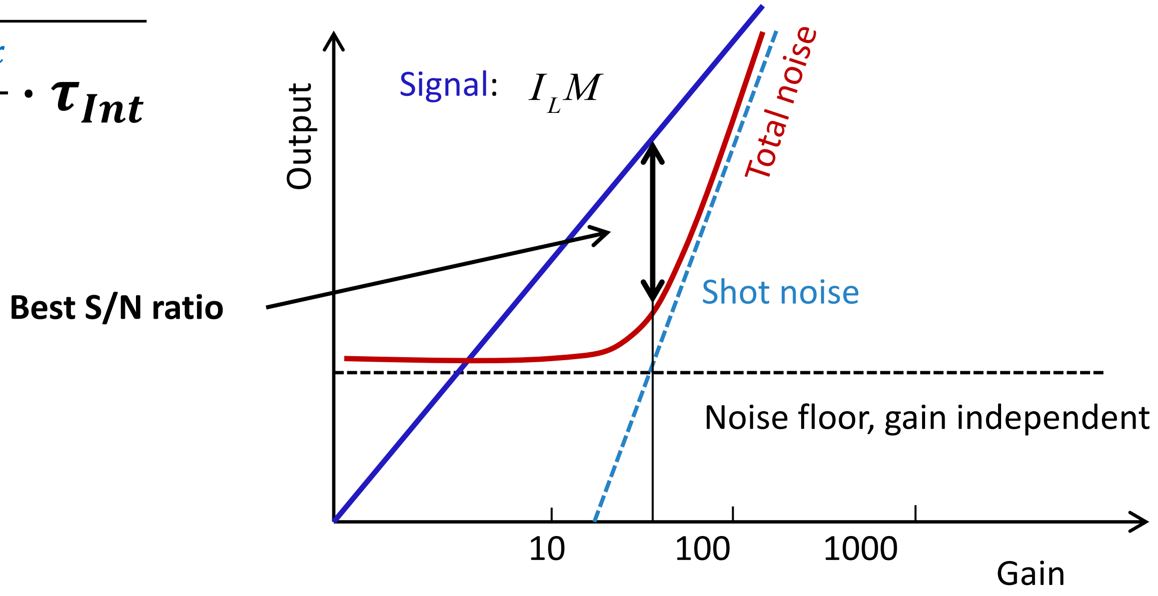
Shot Noise: $ENC = \sqrt{\int i^2_{Shot} df} = \sqrt{\frac{I \cdot (Gain)^{2+x}}{2e} \cdot \tau_{Int}}$

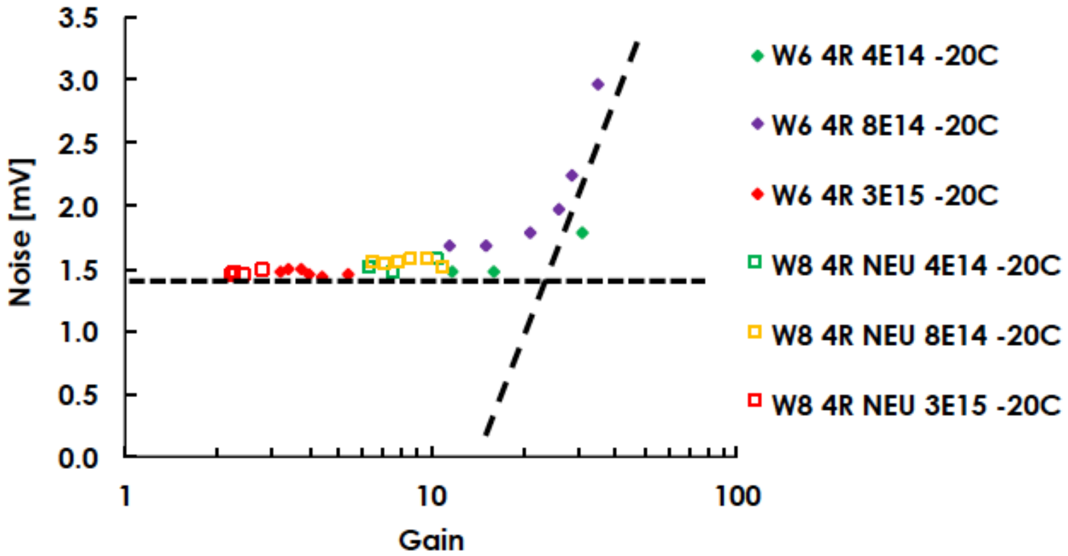
Shot noise increases faster than the signal
→ the ratio S/N becomes worse at high gain

To minimize the shot noise

- **Low gain (G = 10-20)**
- **Cool the detector**
- **Use small pads to have less leakage current**

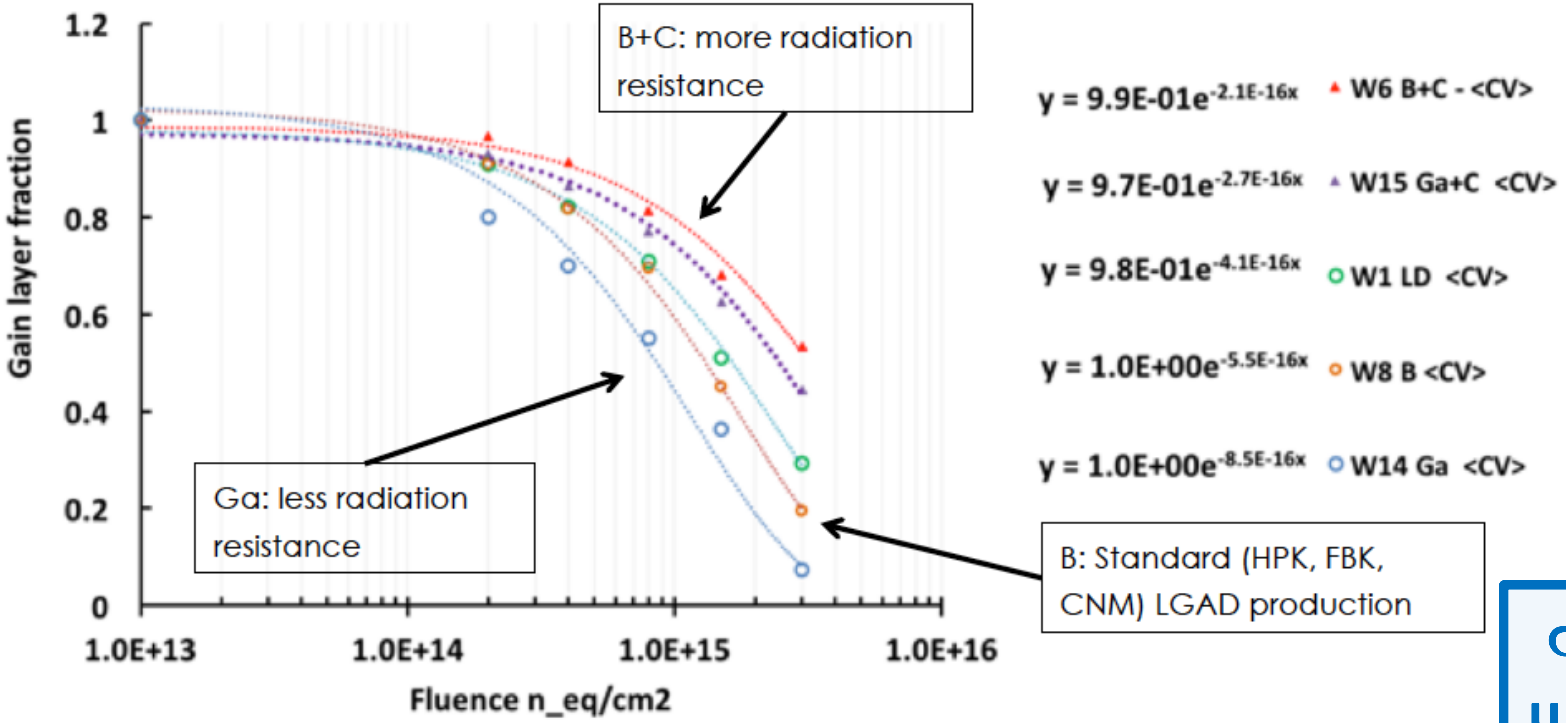
It has been measured that the values of Shot Noise are below the Current fluctuations





LGAD RADIATION TOLERANCE

LGAD suffer for gain reduction due to irradiation
FBK used both Boron and Gallium as gain layer dopant, and added Carbon in the gain layer volume

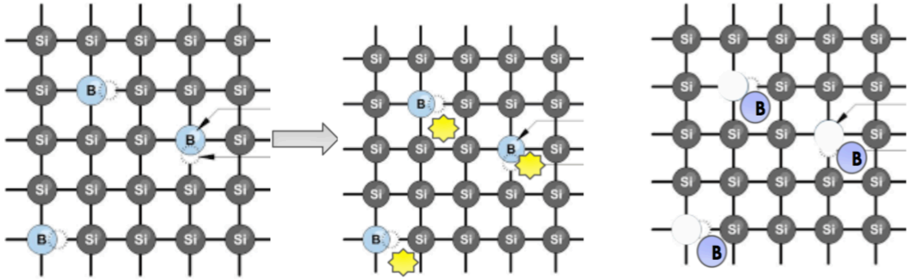


σ_t ~ 30 ps achievable up to $1.5 \cdot 10^{15}$ n_{eq}/cm^2 using Carbon

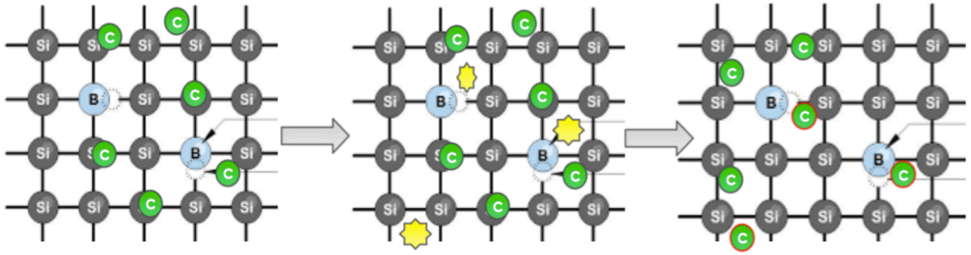
⇒ The usage of Carbon double the radiation hardness of UFSD

Radiation Effects on Boron+Carbon UFSD

➢ Adding Carbon to the Boron implant **halves** the reduction of the gain layer doping due to irradiation



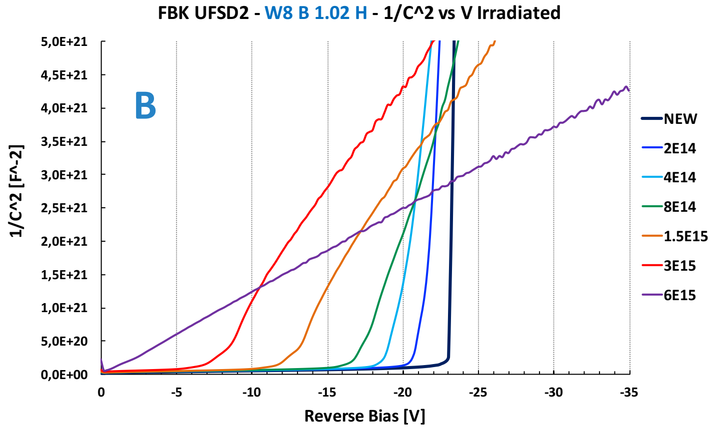
Boron
Radiation creates interstitial defects that inactivate the Boron

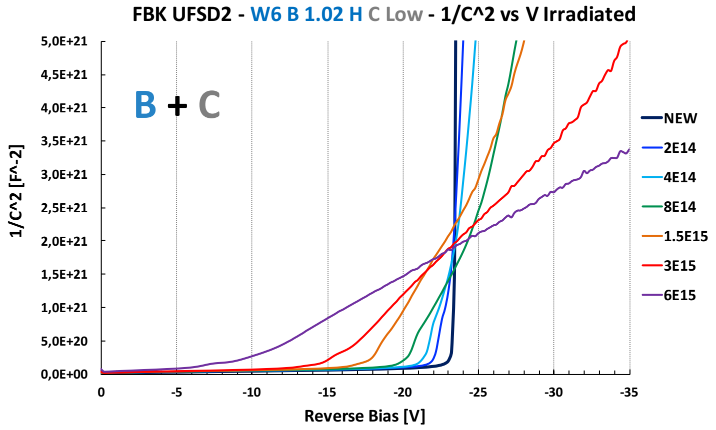


Carbon
Interstitial defects filled with Carbon instead of with Boron and Gallium

➢ SIMS measurements confirm this model: pre- and post-radiation sensors have exactly the same Boron density in the gain layer region, however after irradiation, the Boron is not active any longer
→ **Controlled annealing to re-activate the gain layer under study**

$1/C^2$ vs V_{bias} give information on the doping density inside the silicon volume

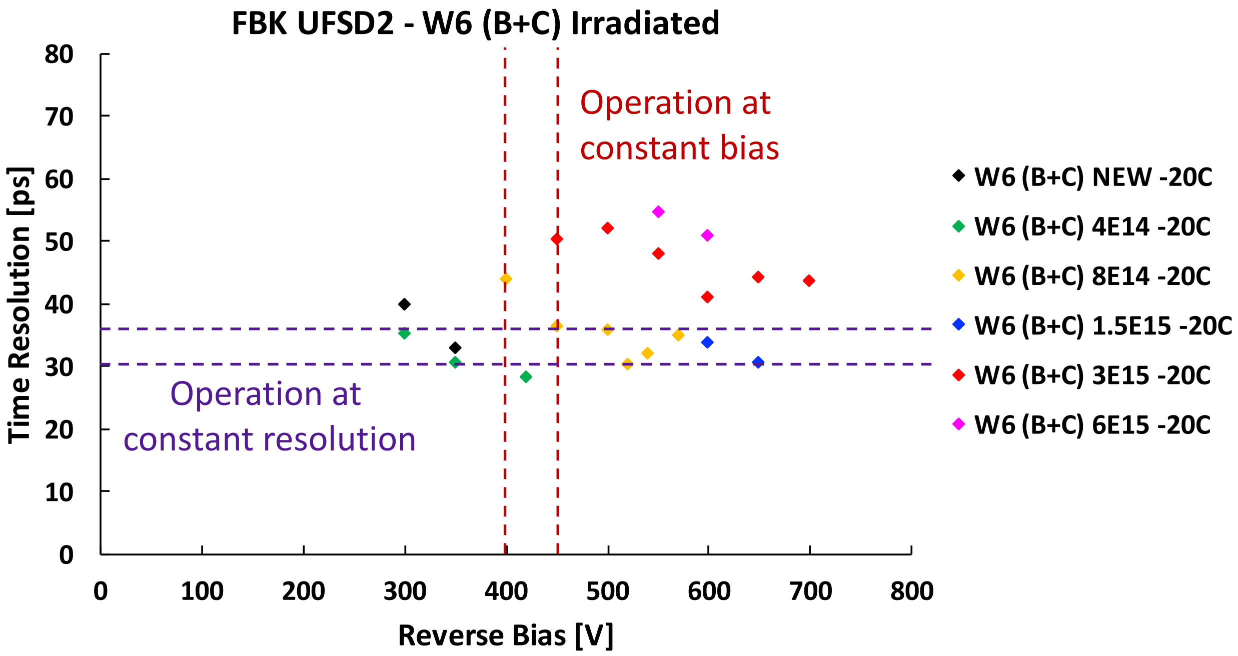




TIME RESOLUTION WITH CARBON

FBK UFSD2 B+C:

- ➢ Constant time resolution up to 1.5E15 n_{eq}/cm^2 increasing V_{bias} to 650
- ➢ Constant V_{bias} up to 1.5E15 n_{eq}/cm^2 with 30% degradation in time resolution

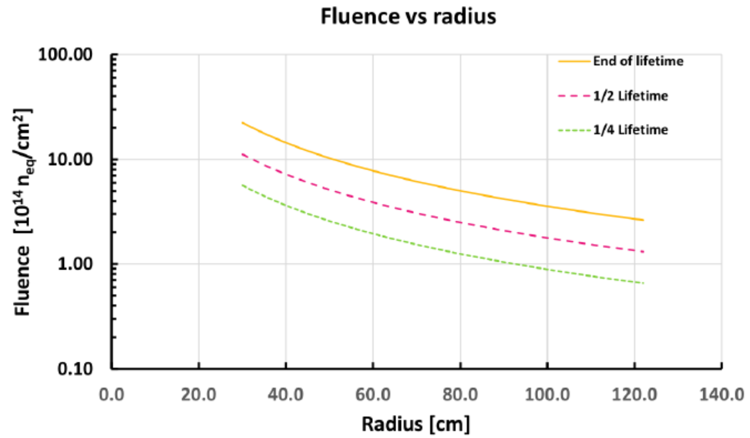


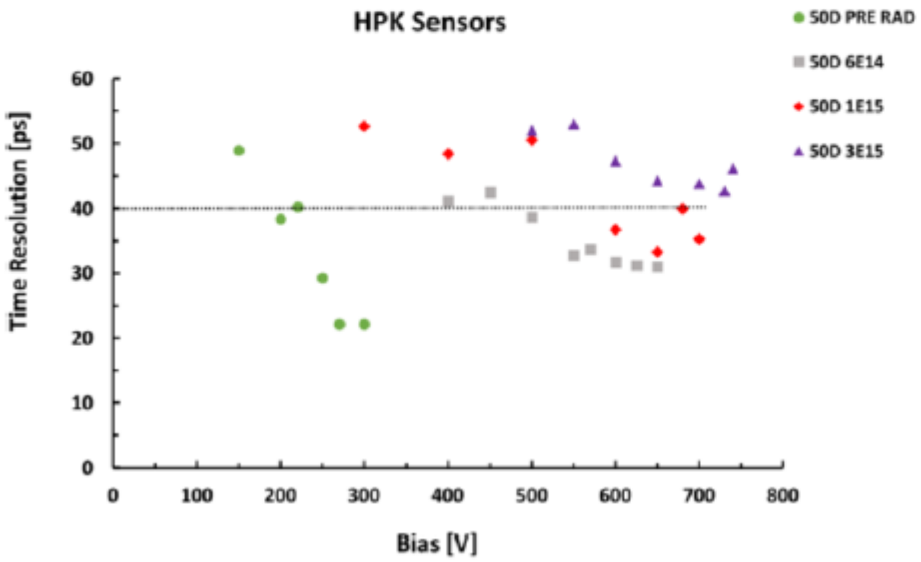
1.5E15 n_{eq}/cm^2 at HL-LHC correspond to 4000 fb^{-1} at $|\eta| = 3$

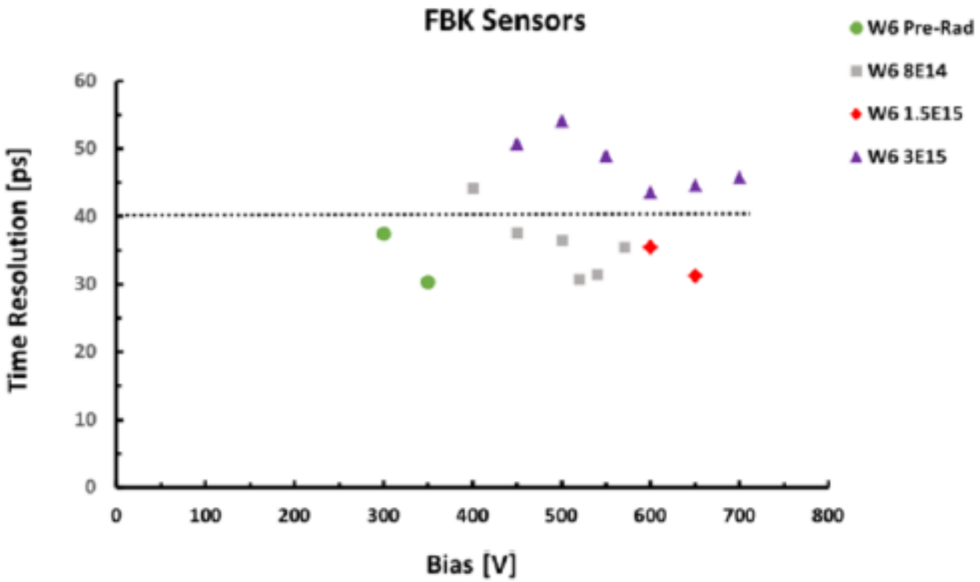
→ Current R&D focuses on reducing the need to increase the bias voltage

ETL RADIATION TOLERANCE

- Time resolution < 40 ps achieved with up to 1.5×10^{15} n_{eq}/cm^2
- Increasing bias voltage to compensate for loss of gain from radiation damage
- Leakage current mitigated by cooling to -30°C



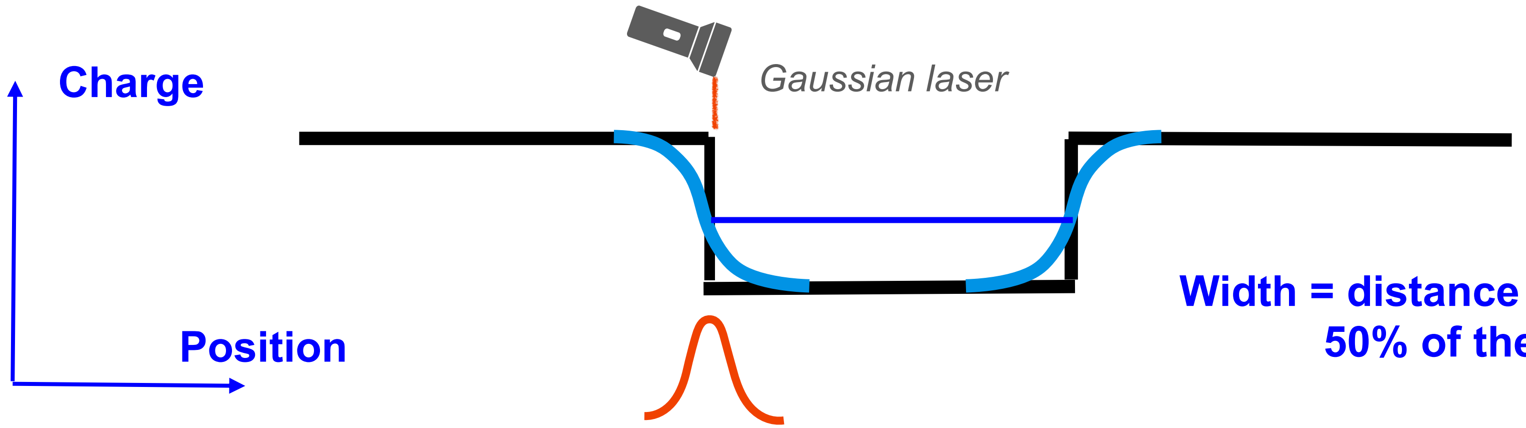


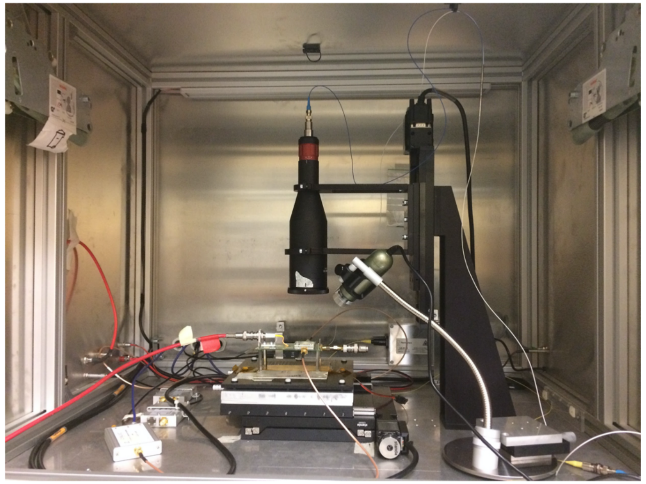


Measurement of the inter-pad width

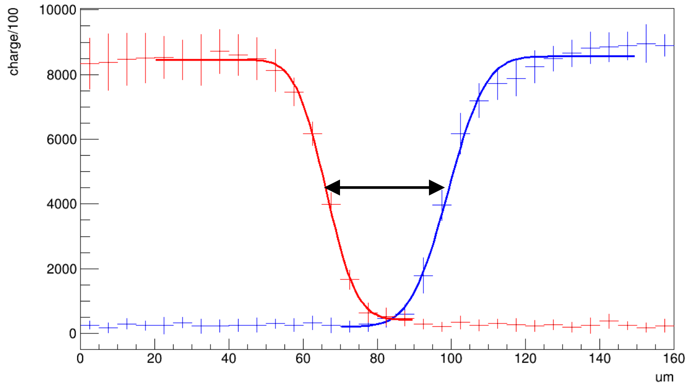
No-gain area width measured with a TCT setup (Particulars)

Get the width by scanning two nearby pads → **charge vs position**





Width = distance between 50% of the s-curves



Results with a point like spot → our spot is 10-15 μm with a Gaussian shape

The real profile is a convolution with a step function with a Gaussian = s-curve

FBK UFSD3.2 – Inter-pad Width

FBK UFSD3.2 – Type 4, 8, and 10
CMS Phase-2 *Preliminary*

Wafer	Type (IP)	Bias [V]	Measured [μm]
W4	T4	230	35.0
	T8	230	40.5
	T10	200	68.0
W10	T4	320	39.0
	T10	320	65.0
W14	T4	280	42.0
	T8	240	44.0
	T10	280	71.0
W7	T4	260	34.0
	T8	250	38.0

Inter-pad FBK UFSD3.2
CMS Phase-2 *Preliminary*

Type (IP)	Measured [μm]
4	35-40 μm
8	40-45 μm
10	65-70 μm

Inter-pad width measured using Transient Current Technique (TCT)

TCT laser parameters:
- f = 1 kHz
- Charge ~ 6 MIP
- Laser spot = 10 μm

Measurements performed at room temperature
Systematic uncertainty = 5 μm

HPK2 – Inter-pad Width Measurement

Inter-pad HPK2

CMS Phase-2 *Preliminary*

	IP	Bias [V]	Gain	Measured [µm]
Split 4	IP3	220	30	64.2
	IP4	220	30	91.1
	IP5	220	30	101.8
	IP7	220	30	120.4

Inter-pad width measured using Transient Current Technique (TCT)

TCT laser parameters:

- f = 1 kHz
- Charge ~ 6 MIP
- Laser spot = 10 µm

Measurements performed at room temperature

Systematic uncertainty = 5 µm

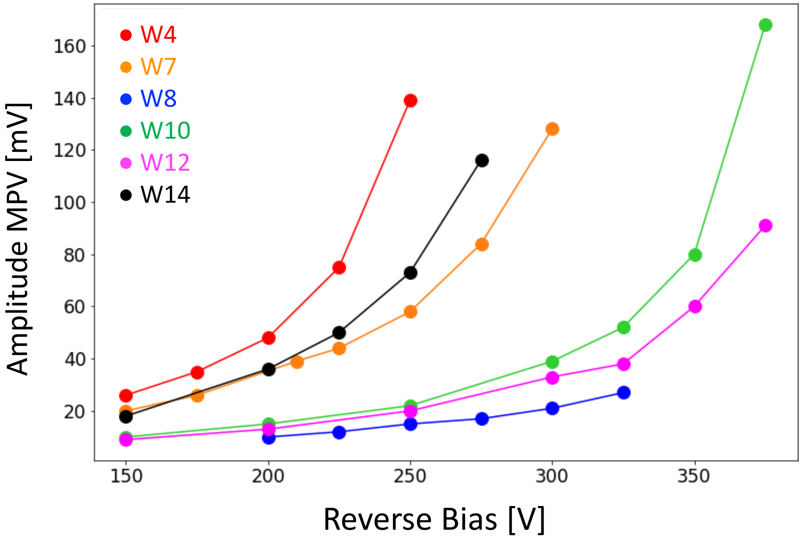
FBK UFSD3.2 – Amplitude & Charge

Wafer #	Thickness	Depth	Dose Pgain	Carbon	Diffusion
4	45	Shallow	L	0.4A	CHBL
7	55	Shallow	L	A	CHBL
8	45	Deep	L'	A	CBL
10	45	Deep	L'	0.6A	CBL
12	45	Deep	M'	A	CBL
14	45	Deep	M'	A	CBH

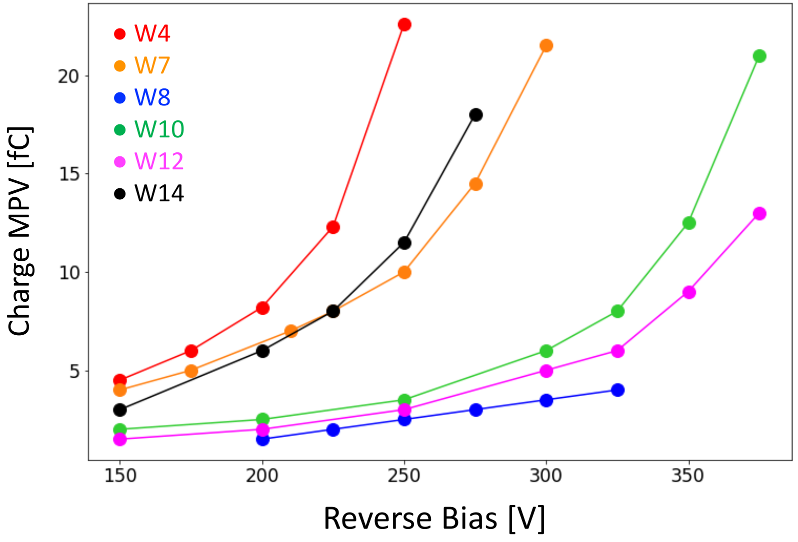
Measurements taken with beta source
Pre-amplification stage with UCSC board
Room temperature

charge [fC] = area [pWb] / 4700 Ω
4700 Ω is the UCSC board trans-impedance

FBK UFSD3.2 – Signal Amplitude – Beta Setup
CMS Phase-2 *Preliminary*



FBK UFSD3.2 – Collected Charge – Beta Setup
CMS Phase-2 *Preliminary*

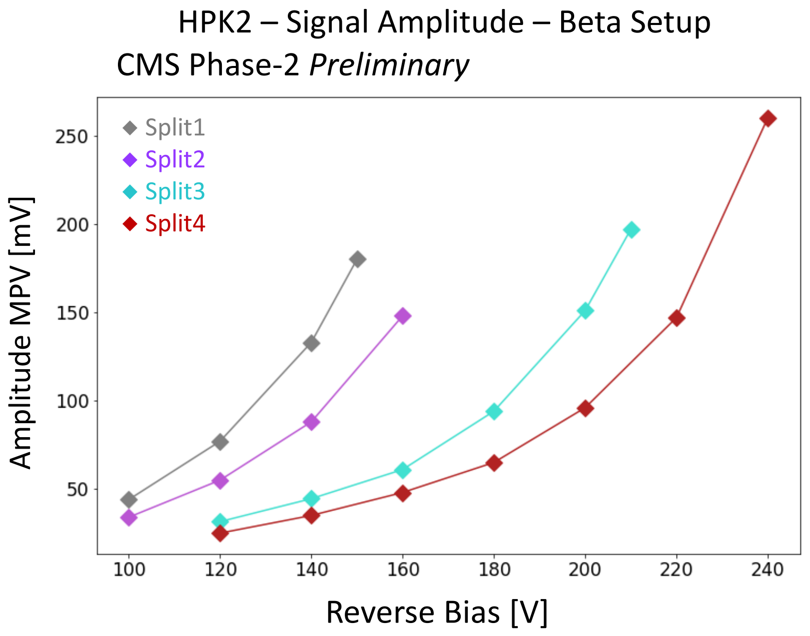


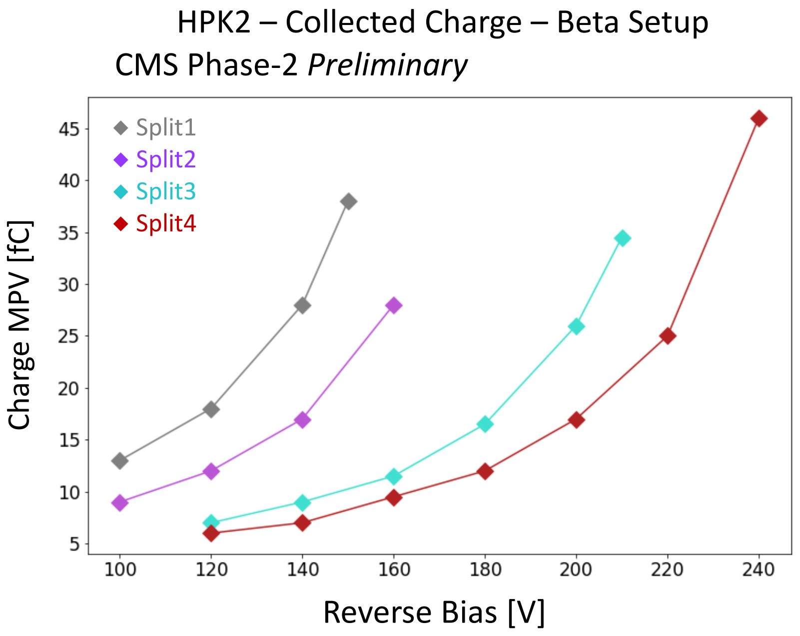
HPK2 – Amplitude & Charge

Gain split	BD voltage	Target
1	160V	ATLAS HG-TD
2	180V	
3	220V	CMS ETL
4	240V	

Measurements taken with beta source
Pre-amplification stage with UCSC board
Room temperature

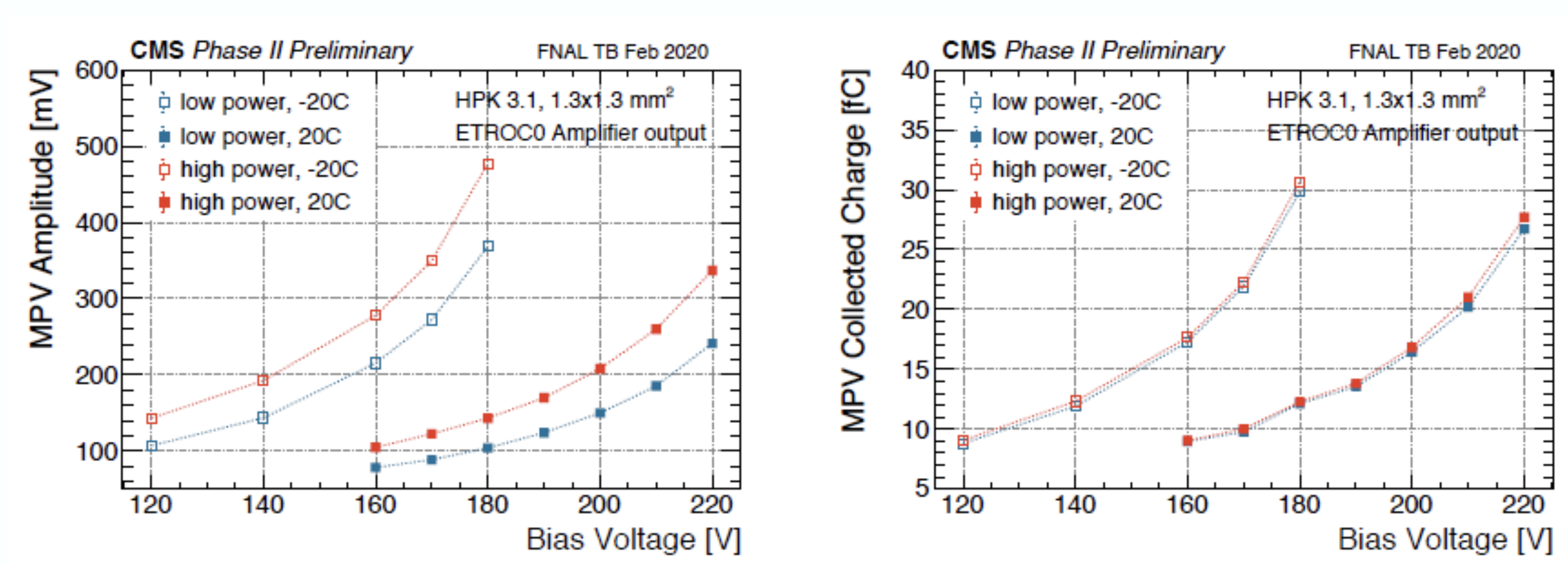
charge [fC] = area [pWb] / 4700 Ω
4700 Ω is the UCSC board trans-impedance





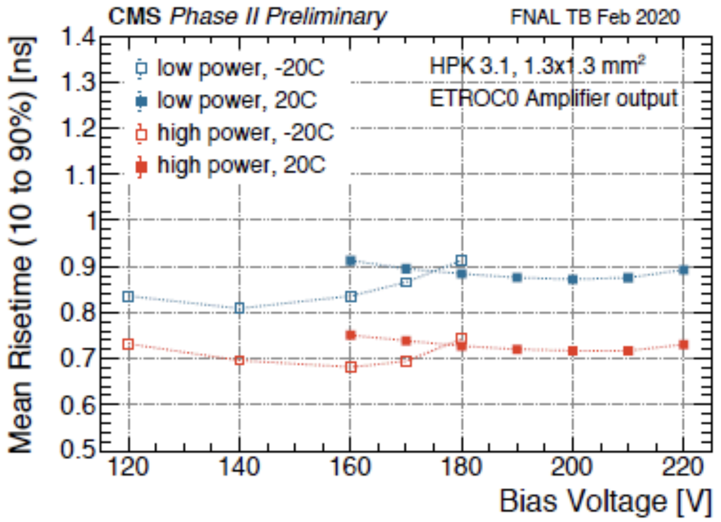
ETROC0 – Amplifier Performance

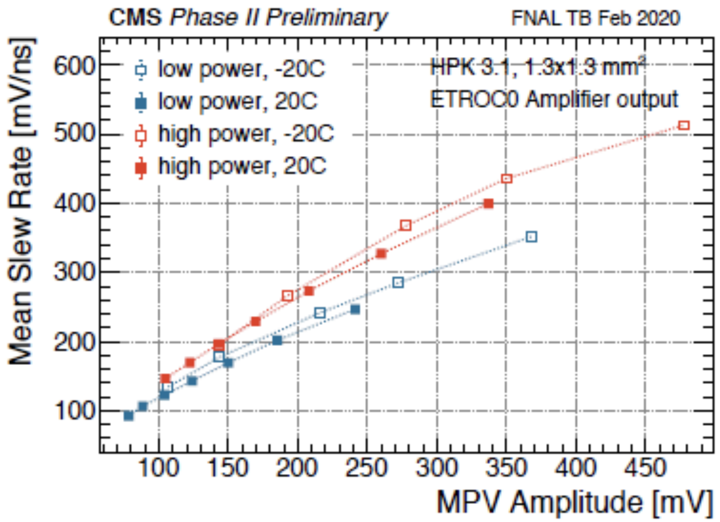
Most probable amplitude and charge as a function of reverse bias

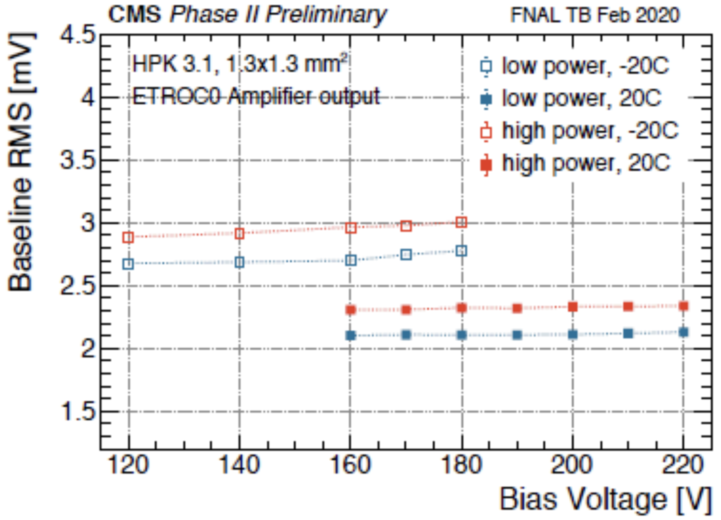


ETROC0 – Amplifier Performance

Key ingredients for understanding jitter and time resolution

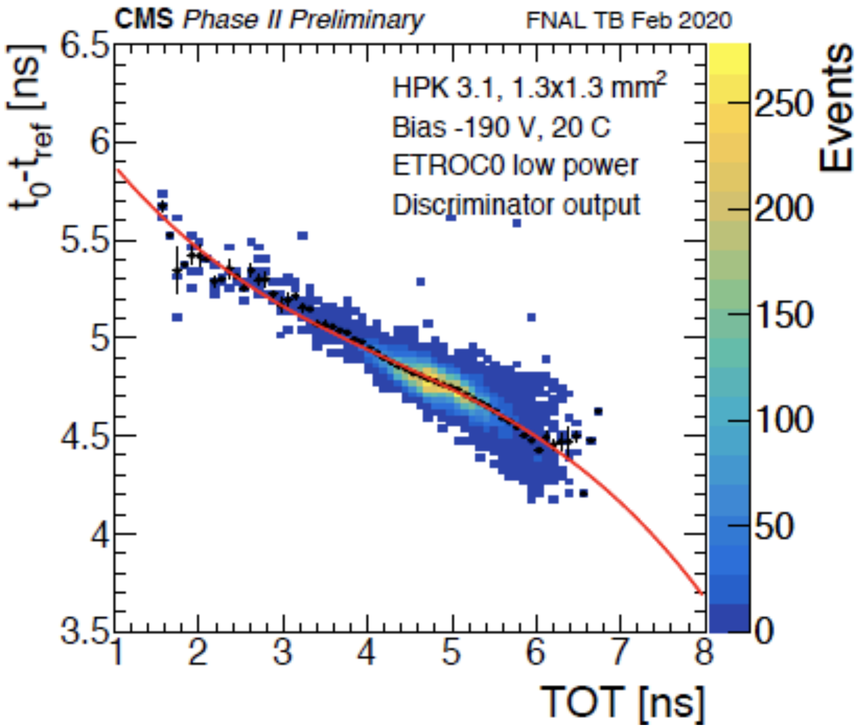






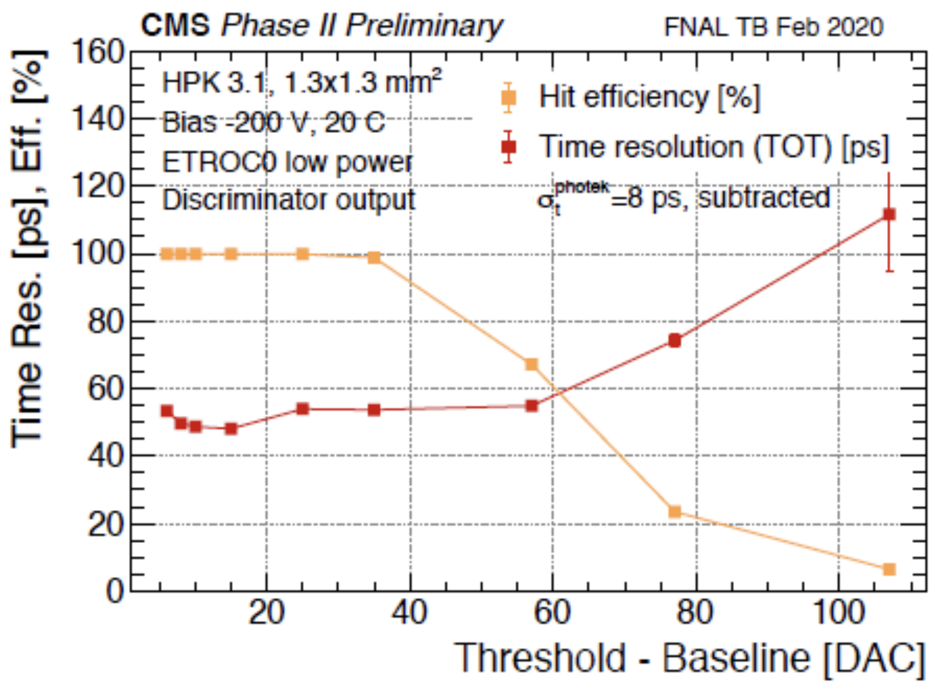
ETROC0 – Discriminator Procedure

An example of
time-walk correction



Charge MPV = 14 fC ⟶ TOT = 4.5 ns
The bulk is between 10-25 fC ⟶ TOT = 4-5.5 ns

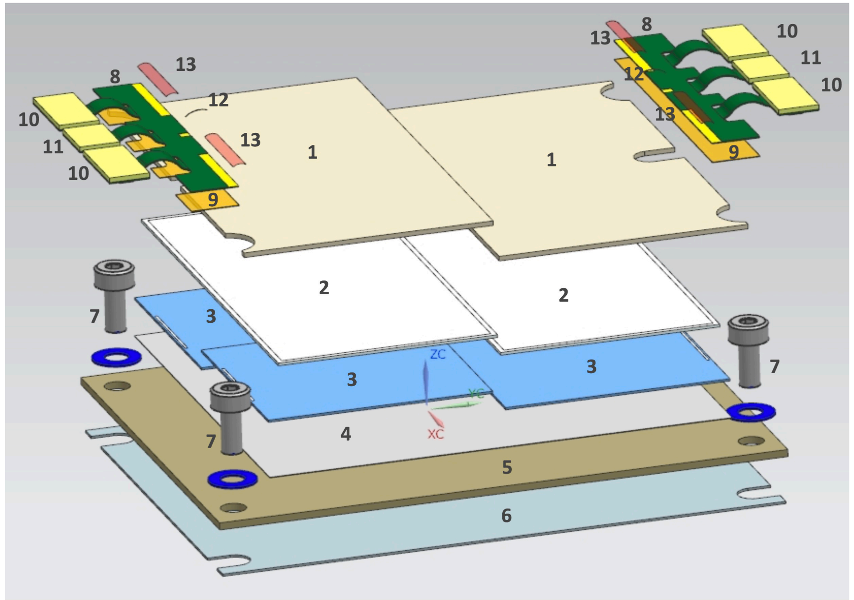
An example of threshold scan
to optimize efficiency & time resolution



Nominal operation at 15 DAC above the baseline

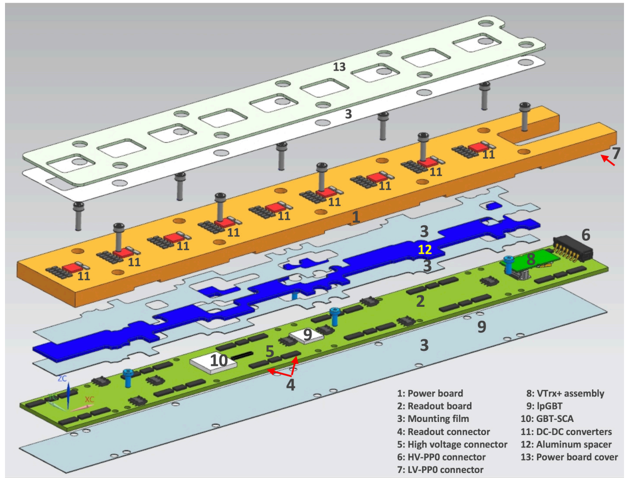
ETL Modules & Service Hybrids

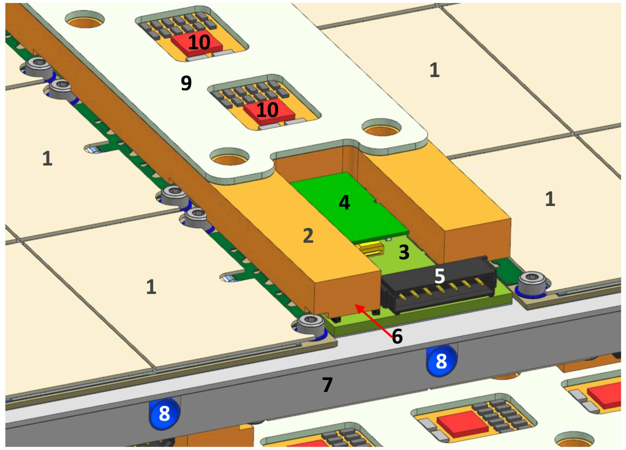
Module Design



1: AlN module cover
2: LGAD sensor
3: ETL ASIC
4: Mounting film
5: AlN carrier
6: Mounting film
7: Mounting screw
8: Front-end hybrid
9: Adhesive film
10: Readout connector
11: High voltage connector
12: LGAD bias voltage wirebond
13: ETROC wirebonds

Service Hybrid





1: AlN module cover
2: Power board
3: Readout board
4: VTRx+
5: HV-PP0 connector
6: LV-PP0 connector
7: Support disk
8: CO_2 cooling tube
9: Power board cover
10: DC-DC converters