Nikhef

Vertex Detector for LHCb upgrade II

- Introduction to LHCb upgrade-II
- Scaling from upgrade-I
- Key performance parameters and trade-offs
- Technological challenges

LHCb

VERTEX LOCATOR

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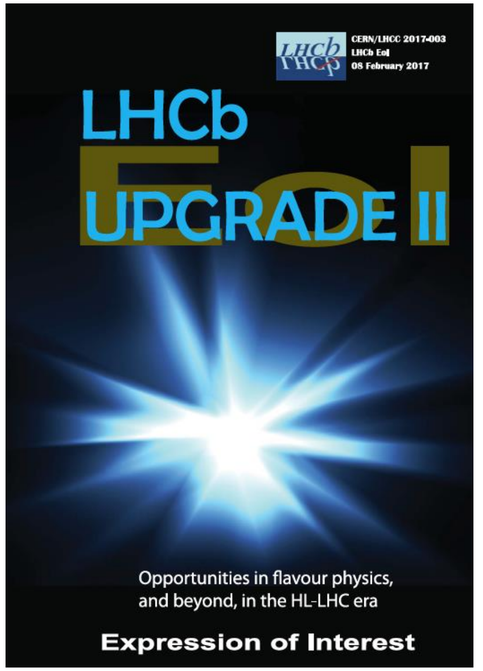
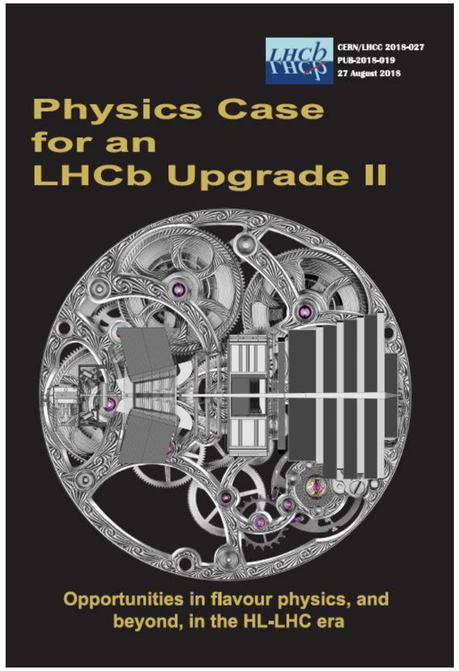
on behalf of the LHCb VELO group
October 8th 2020

LHCb upgrade II

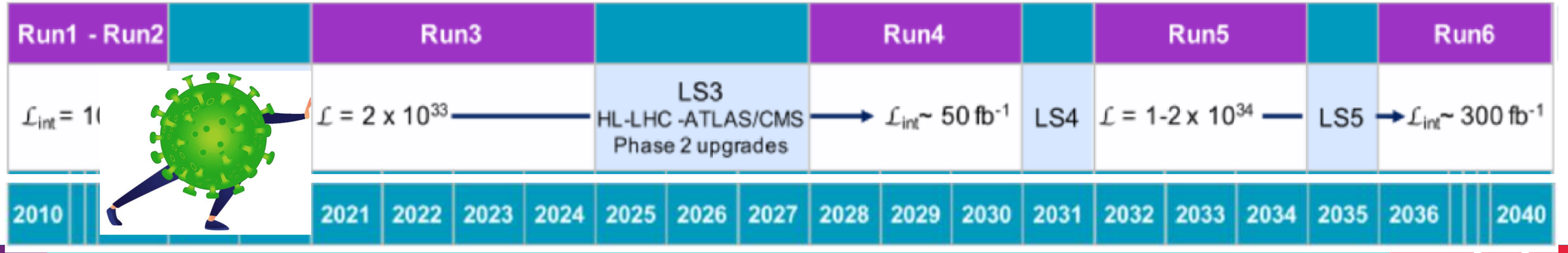
- LHCb: dedicated heavy flavour experiment at LHC
- Why upgrade:
  - Hints of New Physics in LHC Runs1&2
  - Need much more data to further test theoretical predictions
  - Run at higher luminosity
  - Hence need for new / improved detector
- Upgrade-I currently being built/installed
  - (see Manuel's talk)
- Ramping up developments for Upgrade-II
  - To be installed in LS4 (~2031)



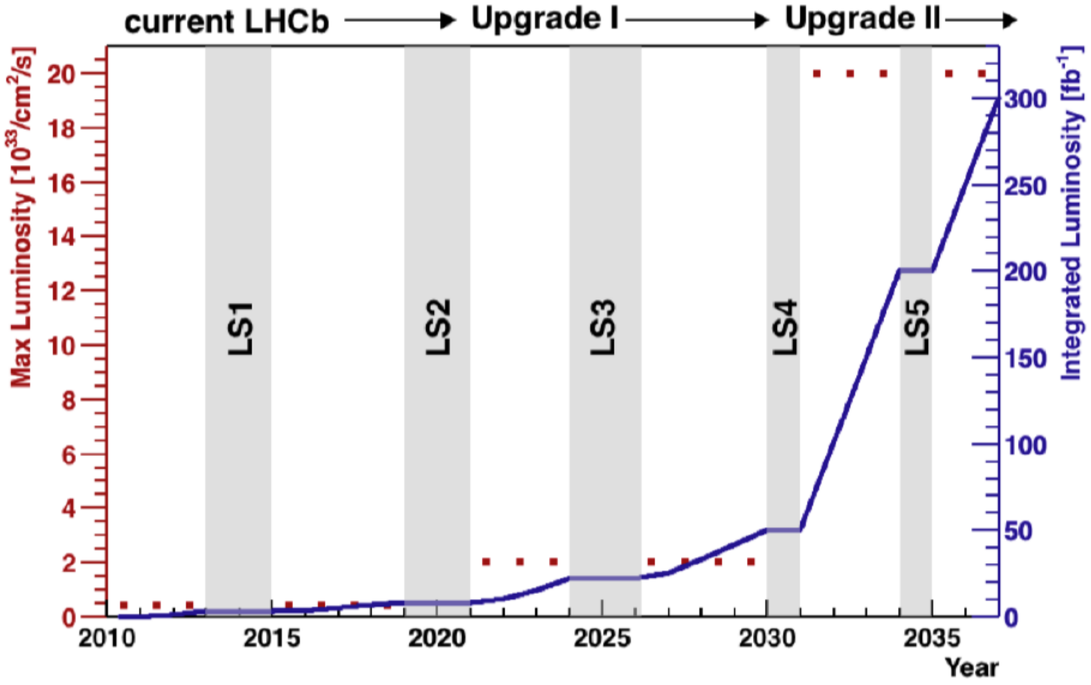
[LHCC-2017-003]



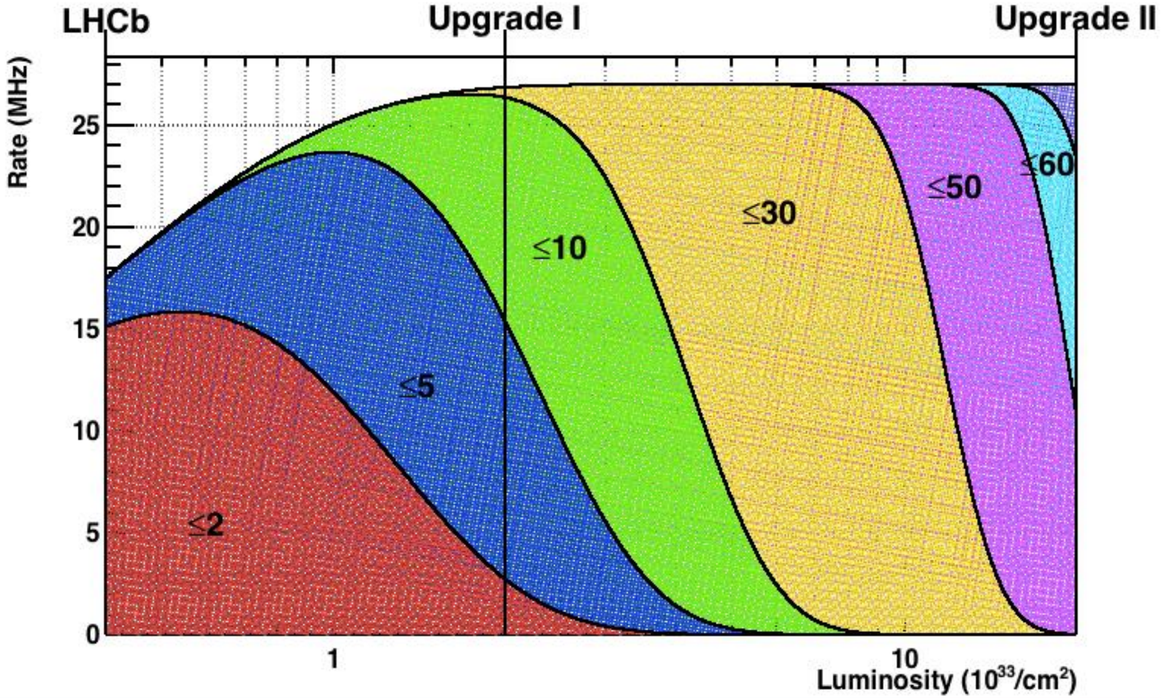
[LHCC-2018-027]



Upgrade II operating conditions

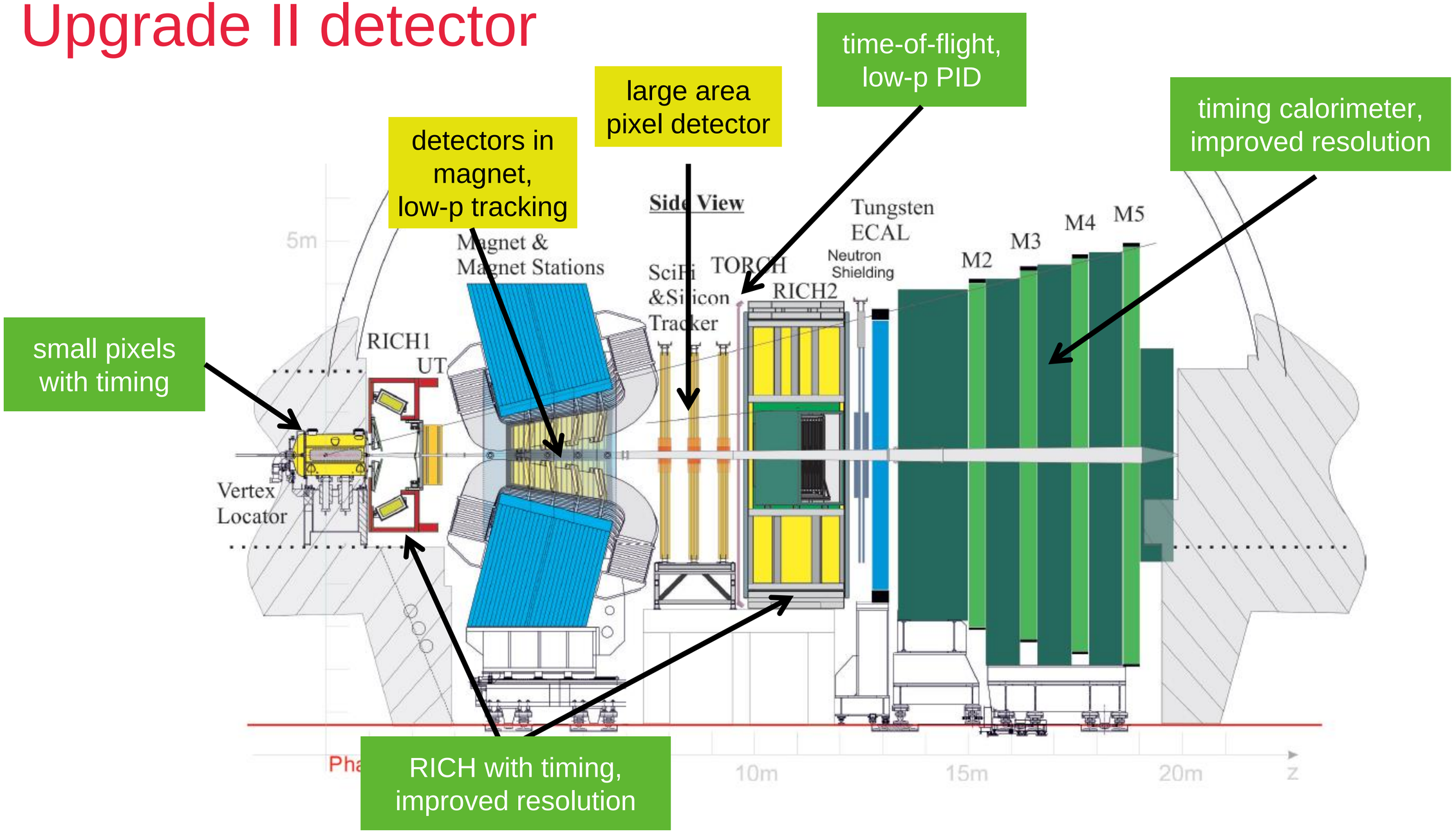


- HL-LHC will give LHCb a luminosity of 1.5×10^{34} cm^{-2}s^{-1}
- = 7.5x luminosity of Upgrade I
- but also 7.5x particle/track/hit rate
- and 7.5x radiation damage / unit of time



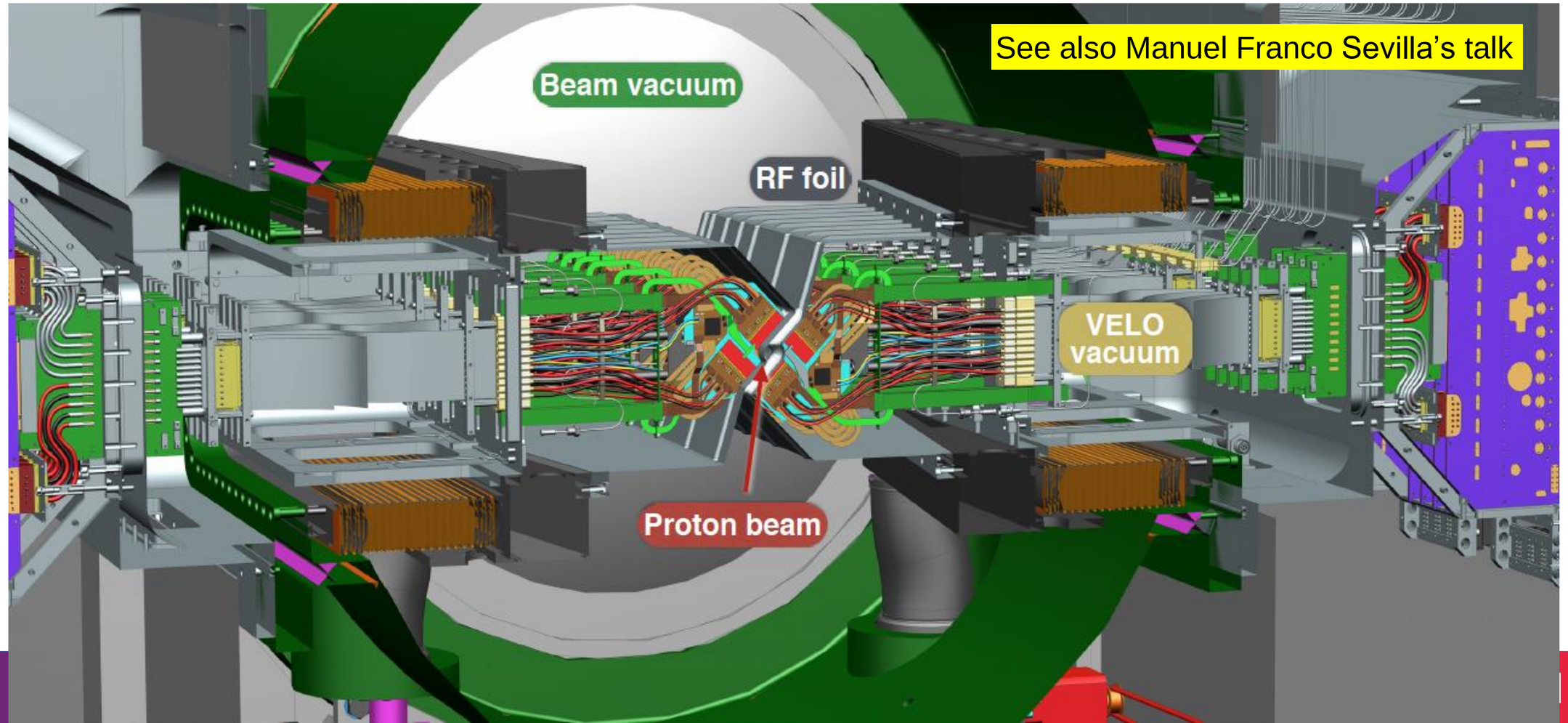
- pile-up of ~50
- σ_z ~ 45 mm
- σ_t ~ 185 ps

Upgrade II detector



Upgrade-I as starting point for Upgrade-II

- Upgrade-II is in very early stage of R&D phase
- -> Showing Upgrade-I design in absence of a detailed/optimised design for Upgrade-II
- Moveable detector, to allow proton beam injection/ramping
- In vacuum to minimise material (‘beam pipe’) between vertices and first sensor



Scaling up from Upgrade-I

Baseline: Upgrade-II should have at least the same performance as Upgrade-I

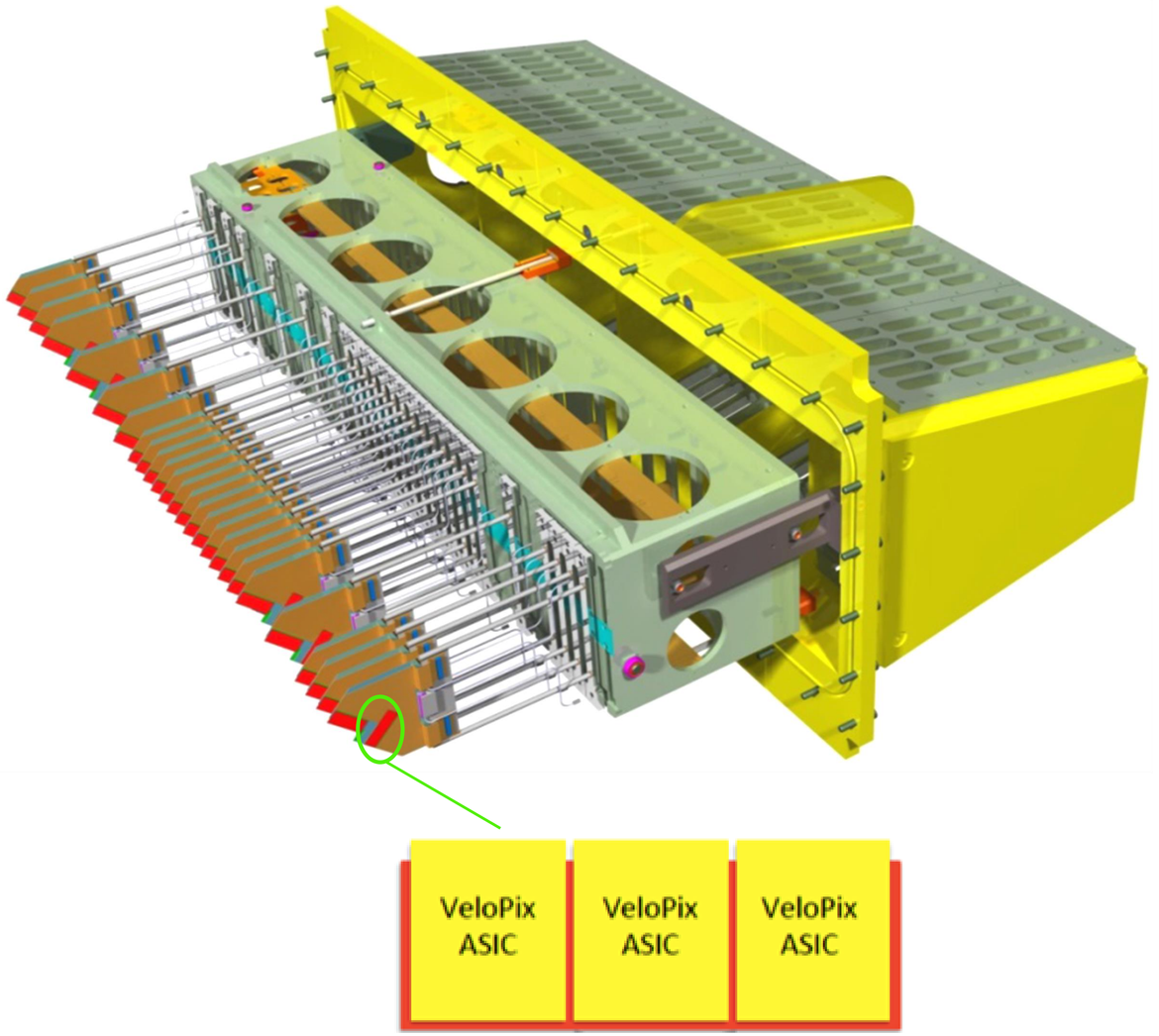
Hit/track rate, radiation etc. are scaled up from Upgrade-I

Key numbers Upgrade-I vertex detector:

- 26 stations
- Silicon planar pixels (200 μm n-on-p)
- 55 μm pitch
- binary readout (VeloPix ASIC)
- 5.1 mm from beam
- fluence at tip of sensor: 8×10^{15} 1 MeV n_{eq}/cm^2
- hottest ASIC (2 cm^2) produces ~ 20 Gbit/s

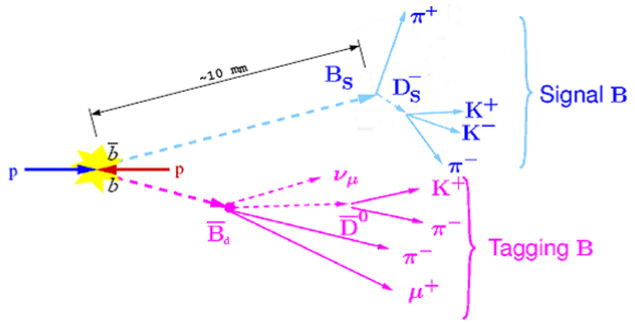
Upgrade-II

- integrated luminosity 300 fb^{-1} (6x)
- instantaneous luminosity 1.5×10^{34} $cm^{-2}s^{-1}$ (7.5x)

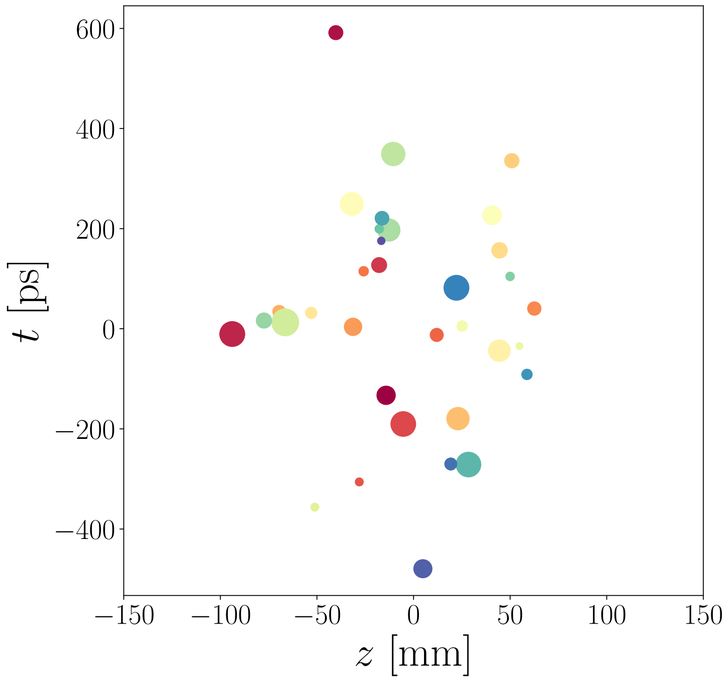


Why timing for high luminosity

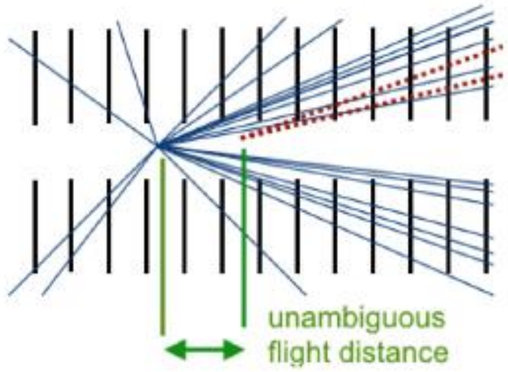
- Disentangle multiple primary vertices
- Assign secondary vertices to correct primary vertices
- Physics background reduction



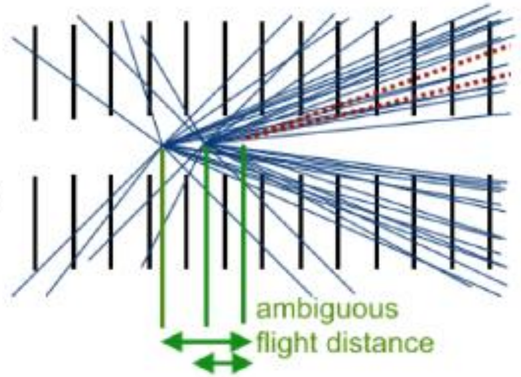
typical single bunch crossing



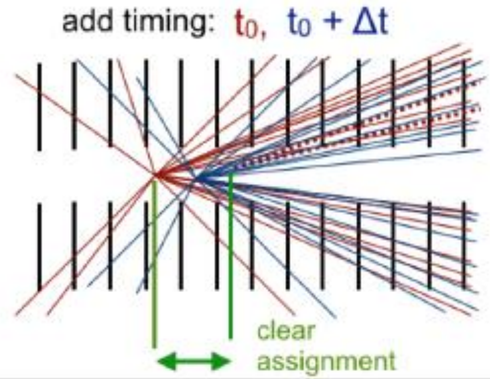
single primary vertex:



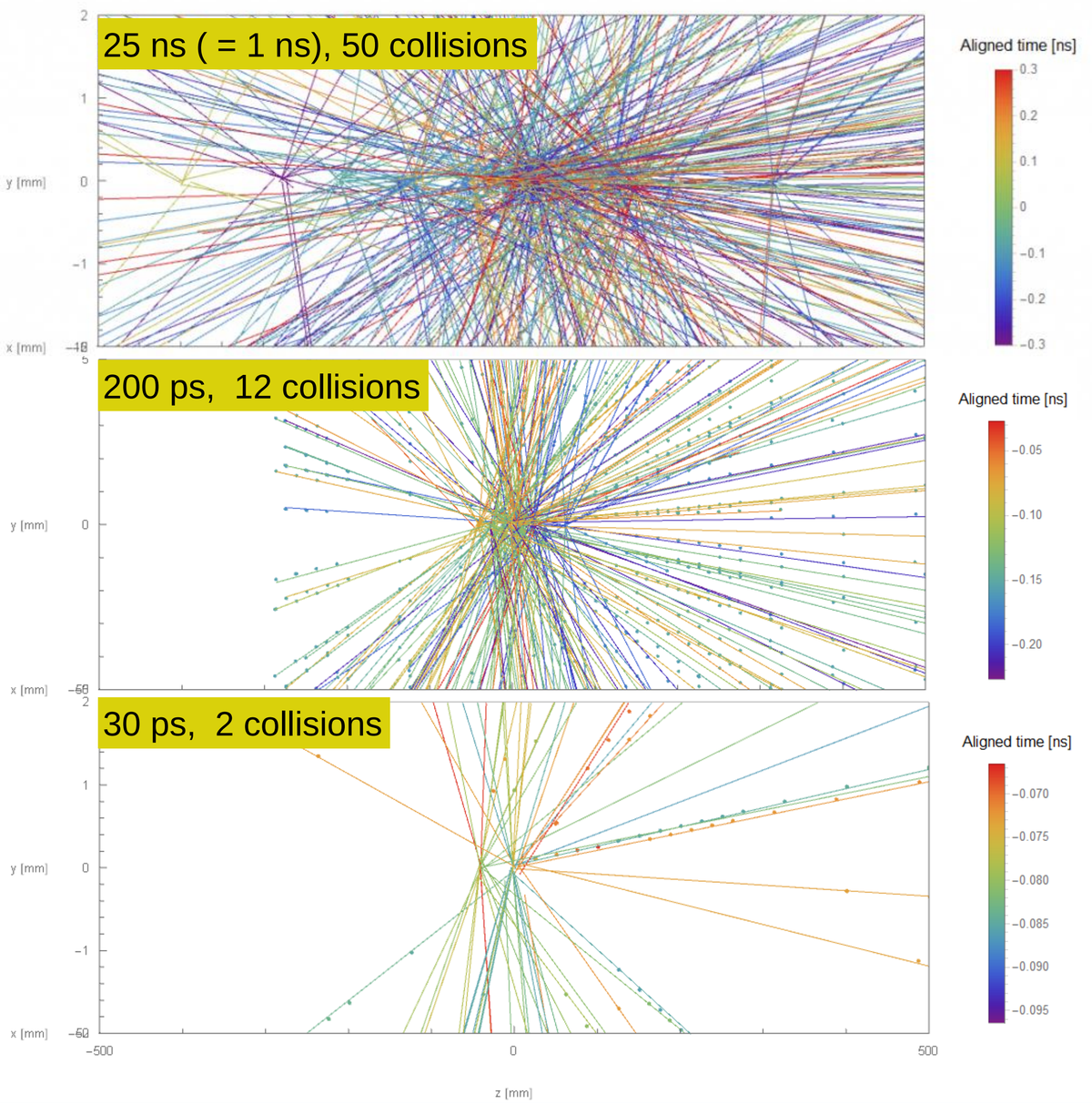
two primary vertices:



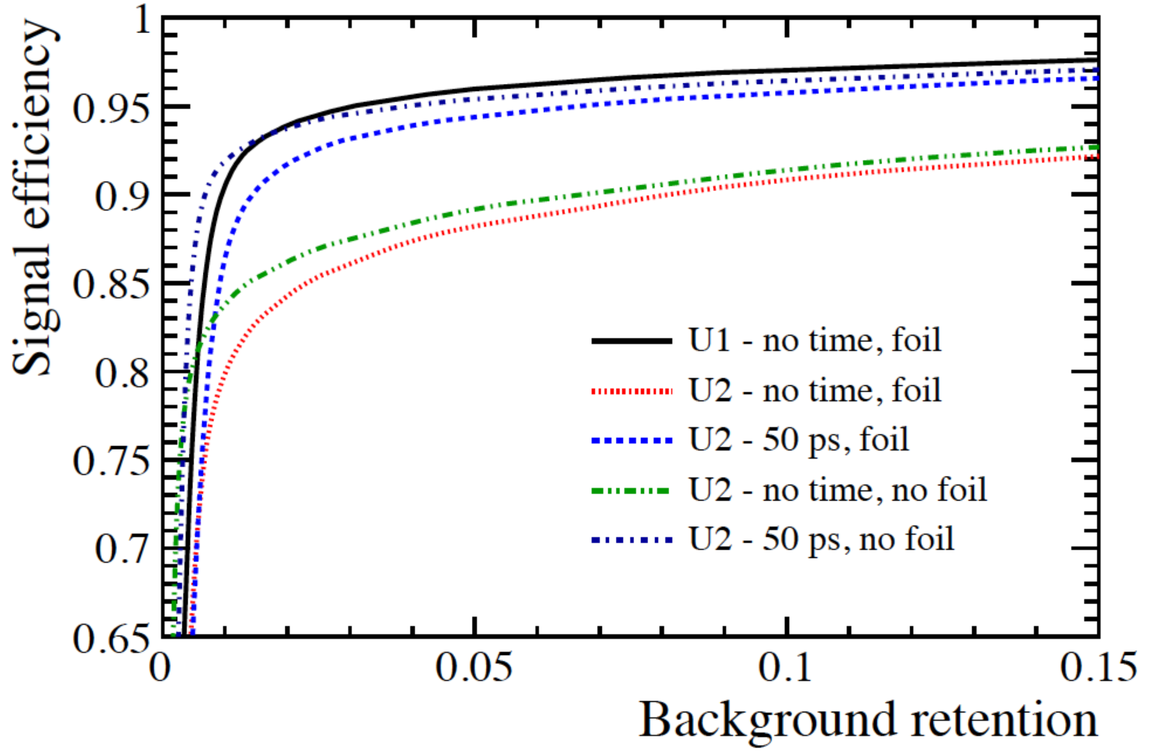
two primary vertices + time decoding $t_0, t_0 + \Delta t$



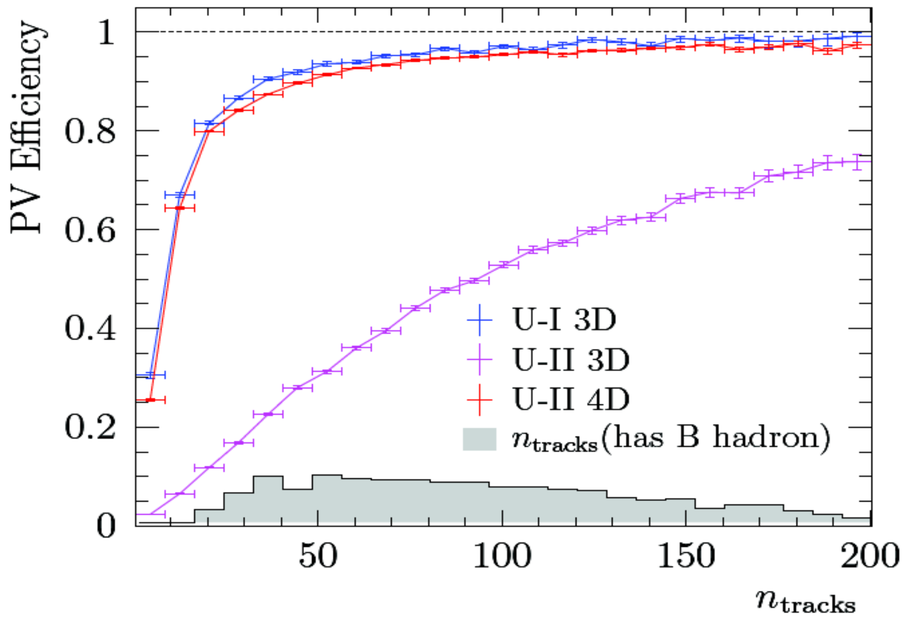
Time slices

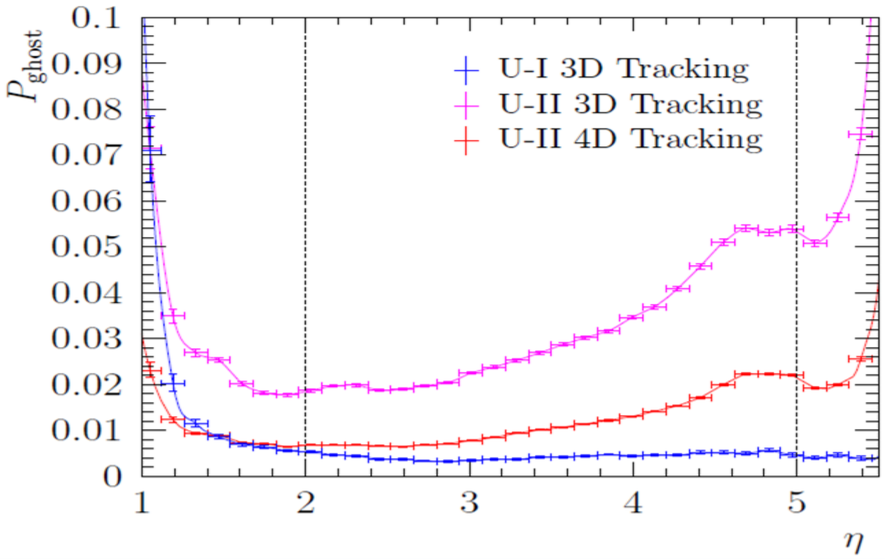


- Required temporal resolution < 50 ps / hit, < 20 ps / track
- TOF complicates matters



Timing layer or 4D tracking





- Timing is key for primary vertex efficiency
- Either with timing planes or 4D tracking

4D tracking benefits:

- Pattern recognition efficiency
- Reduction of ghost track rate, saves CPU power

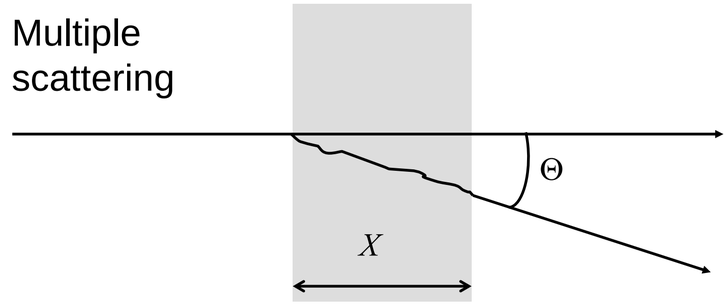
- Studies ongoing of 4D tracking on CPU, GPU and FPGAs

- Timing layer(s) not ruled out, but
  - Tighter timing requirements (track time)
  - Development of two technologies
  - Less redundancy, poorer efficiency due to smaller geometric coverage

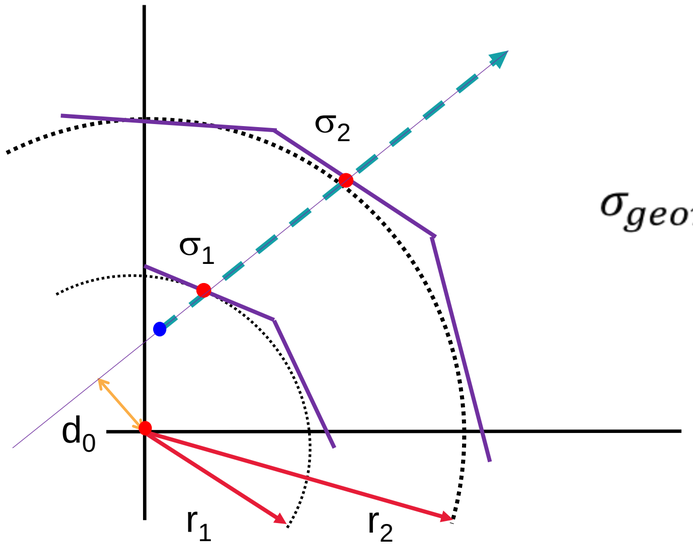
Core business: how to get a good IP resolution (simplified)

3 main ingredients:

- intrinsic hit resolution σ_1, σ_2
- Distance to 1st measured point and lever arm
- Multiple scattering in detector material and RF-foil
  - worse at low P_T



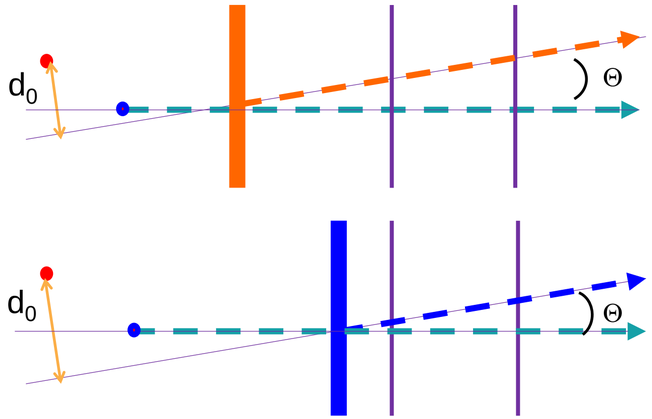
$$\sigma_{MS} = \frac{r}{p} 13.6\ MeV \sqrt{\frac{x}{X_0}} \left[1 + 0.038 \log\left(\frac{x}{X_0}\right)\right]$$



$$\sigma_{geom} = \sqrt{\frac{r_2^2\sigma_1^2 + r_1^2\sigma_2^2}{(r_2 - r_1)^2}}$$

$$s_{d_0}^2 \approx s_{geom}^2 + \left[\frac{r}{p_T} f\left(\frac{x}{X_0}\right)\right]^2$$

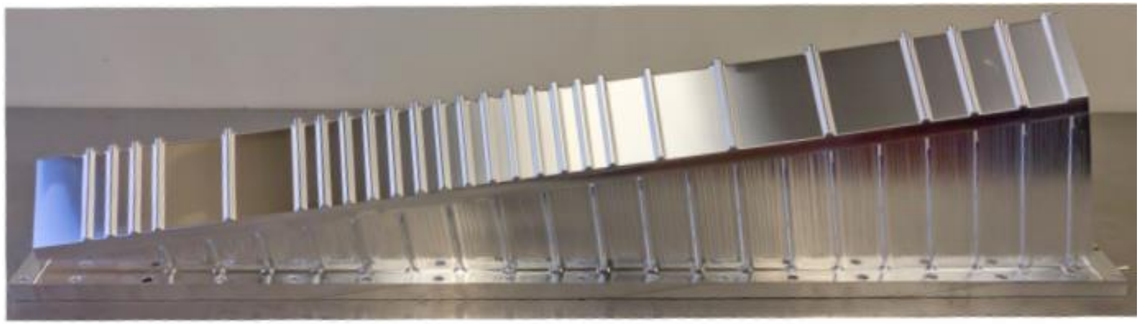
location of material is important

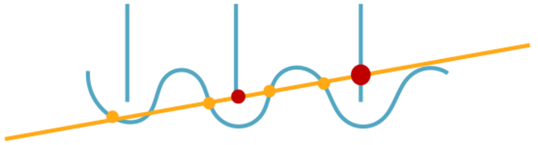


Material budget: RF foil

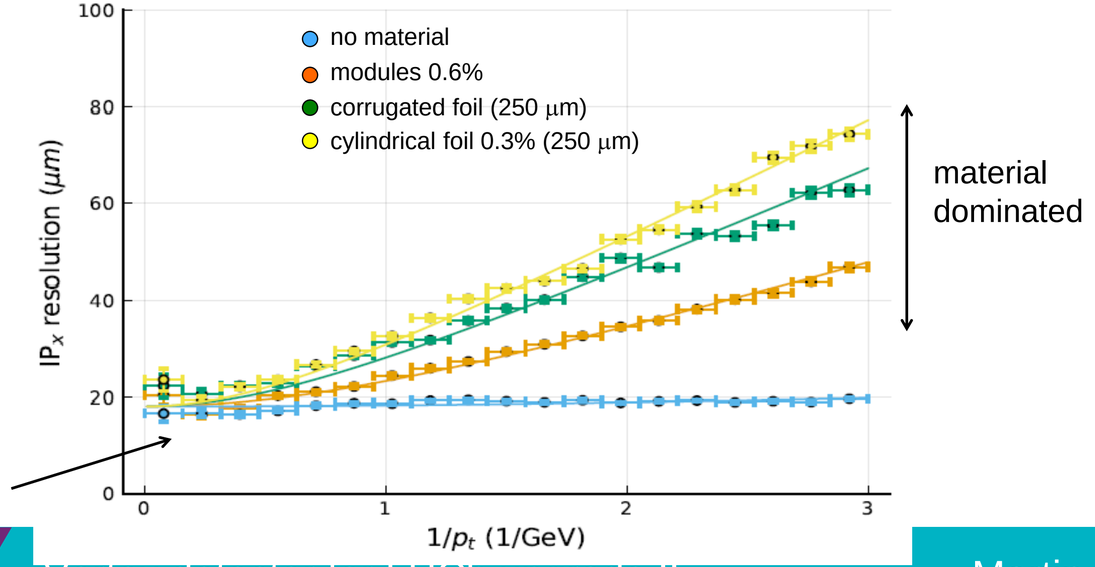
VELO is in a secondary vacuum enclosure:

- Guides beam mirror currents, avoid wakefields
- Minimises RF pickup by the sensor modules
- Lowers the constraints on material outgassing
  - which pollutes beam pipe surfaces
- Corrugated foil shape reduces amount of material before first measured point, which is a significant factor for IP resolution
- Thickness set by need to tolerate 10 mbar pressure difference between primary and secondary vacuum



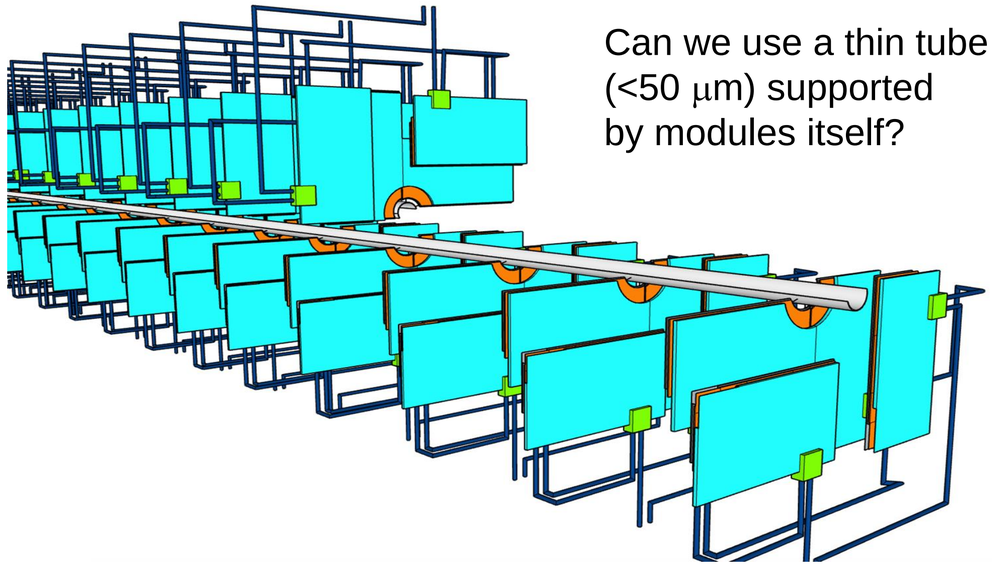


Corrugations needed to minimize material.



material dominated

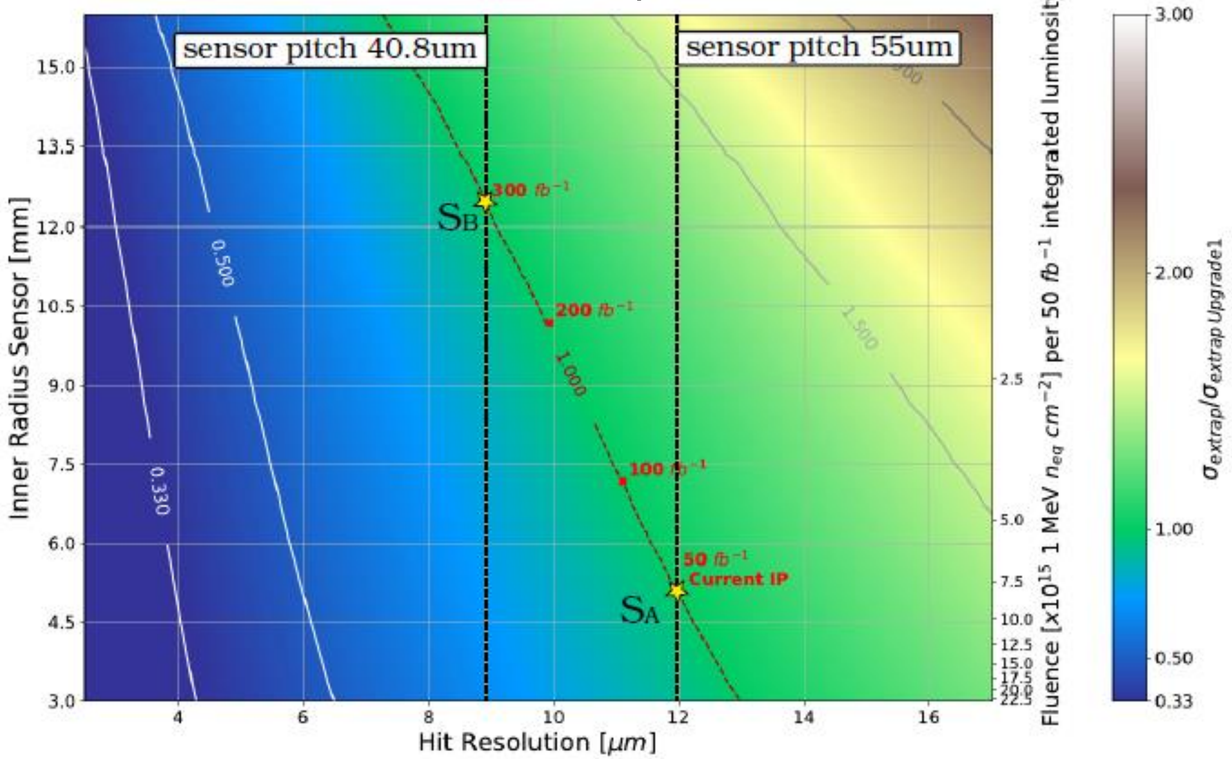
geometry dominated



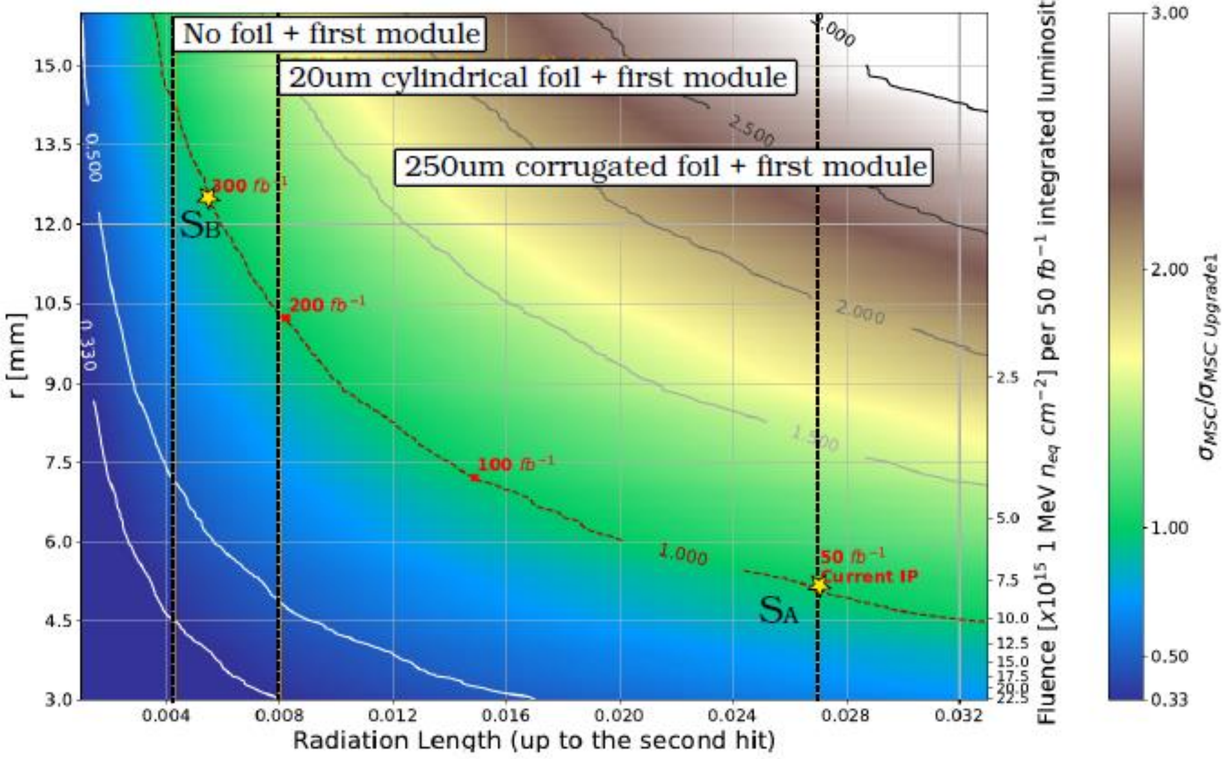
Can we use a thin tube (<50 μm) supported by modules itself?

Optimise distance vs. pitch vs. material vs. …

Geometrical dependence



MSC dependence



- Upgrade-I sensors are at 5.1 mm from beam
- Same performance for Upgrade-II can be achieved at 12.5 mm from beam (8x less radiation) if:
  - Pixel pitch is reduced from 55 to 41 μm (-> 55% of area for the pixel electronics)
  - Material in RF foil and first detection layer is drastically reduced

Find a compromise

Physicists

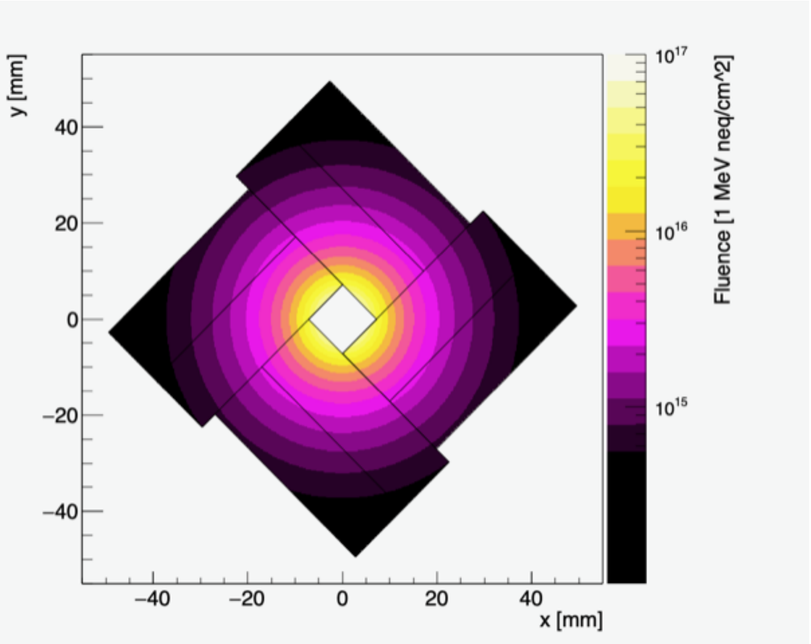
(ASIC) engineers

- smaller pixels
- faster timing
- thinner sensors (less signal)
- less material
- lower temperature / power

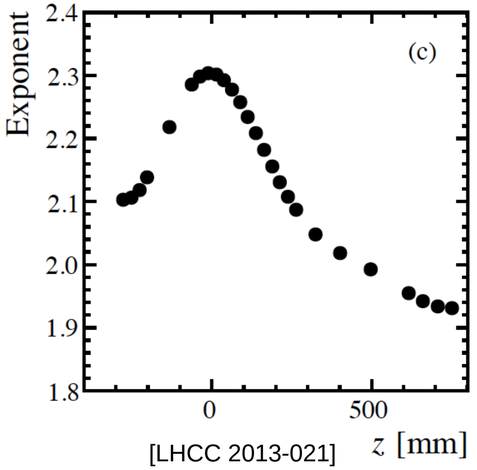
- not too small pixels
- more signal
- low pixel capacitance
- generous power budget

Radiation levels

- High in an absolute sense: ~5x10^{16} 1 MeV n_{eq} / cm^2 @ 5.1mm
- Highly non-uniform
  - Factor 40-100 difference in fluence within in a single sensor
  - Is a challenge for sensors, especially those with gain
  - Is challenge for the ASIC: it is all about locally high rates
- To date no single sensor technology has been shown to survive the required life time fluence
- (bi-)annual replacement could be an option

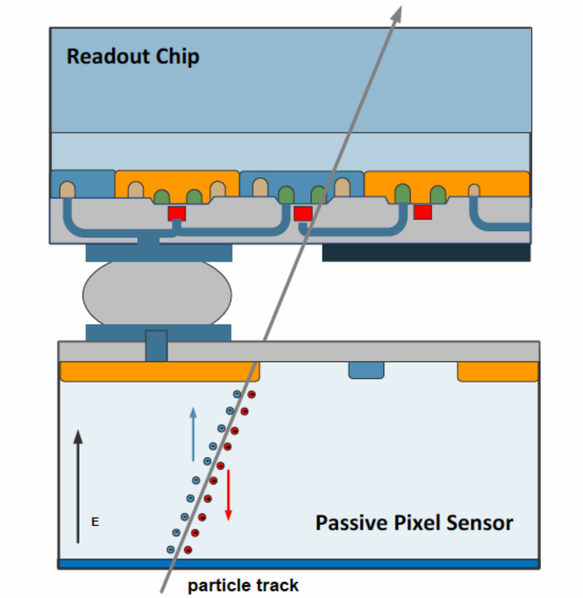


- fluence in radial direction drops as AR^{-k}
- somewhat smaller k for downstream stations



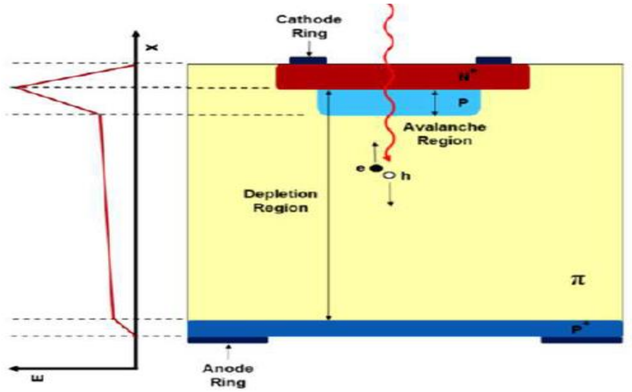
[LHCC 2013-021]

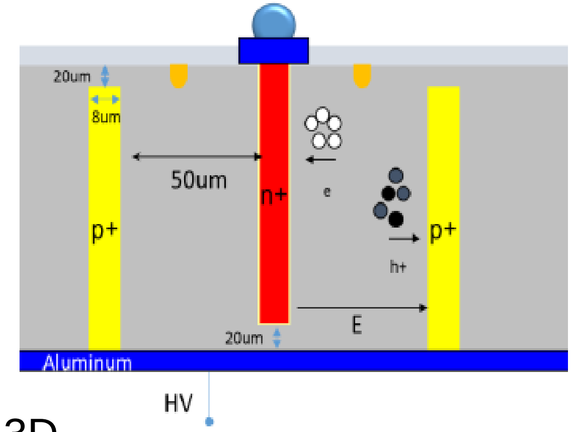
one slide on sensor technology



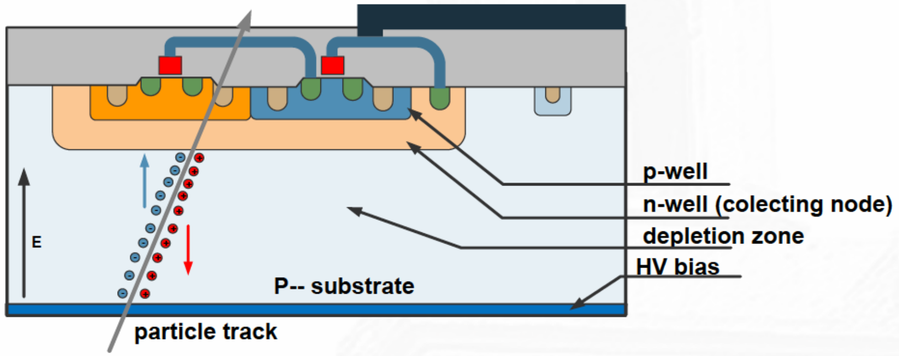
hybrid planar
- signal proportional to thickness
- charge collection time depends on thickness
- faster -> thinner -> less signal -> FE challenge

(hybrid) Low Gain Avalanche Detector (LGAD)
- gain provides sufficient charge at small thickness
- gain drop as function of fluence
- non-uniform irradiation (next slide)





(hybrid) 3D
- signal proportional to thickness
- small column to column distance -> fast
- higher pixel capacitance
- impact of dead regions requires study

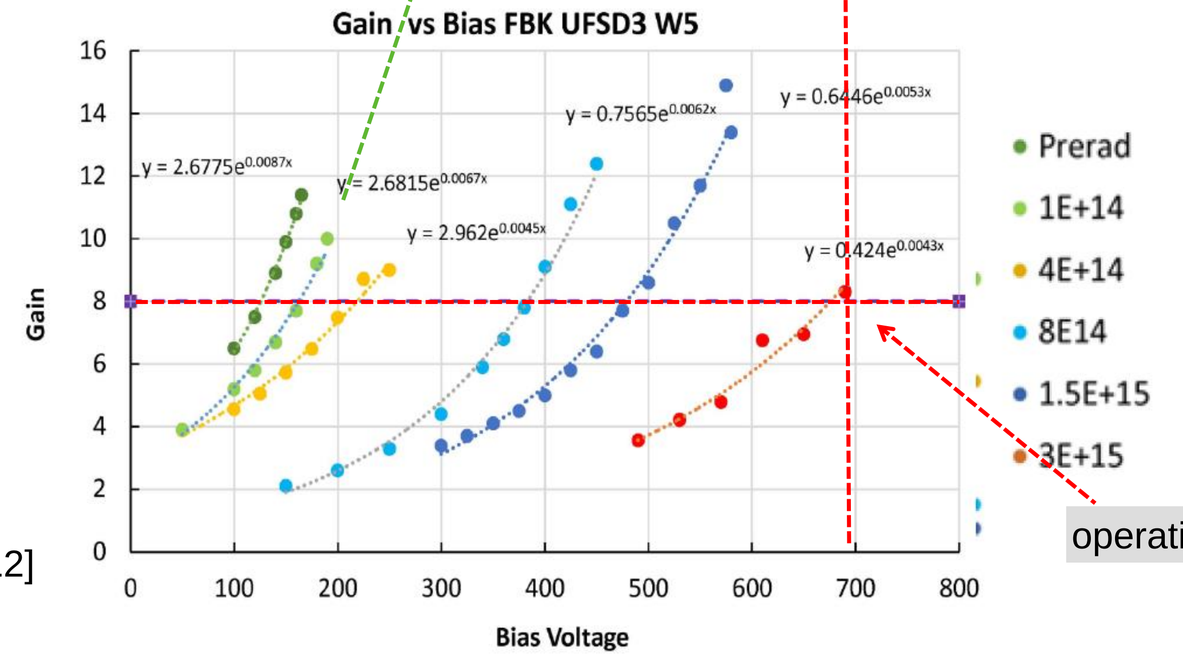


(depleted) monolithic
- thin layer, hence small signal
- but also low capacitance
- Alice upgrade for LS4 considers < 50 ps/hit timing
- readout in same technology as sensor, relatively large feature size
- moderately radiation tolerant

Where VELO is different, LGAD and non-uniform irradiation

other corner of sensor is almost not irradiated,
follows this green gain curve

where does the green curve meet the red bias line?



operating point for tip of sensor

[H. Sadrozinski, HSTD12]

- Initial acceptor removal reduces gain
- Gain can be recovered by applying more bias voltage
- VELO fluence is very non-uniform
  - can we run with one bias voltage per sensor, how to get rid of the huge signals?
  - is it possible to define multiple bias regions in one LGAD sensor?

A few words on the ASIC

Front-end: minimise jitter by maximising slope at amplifier output (ideal sensor, dirac delta signal)

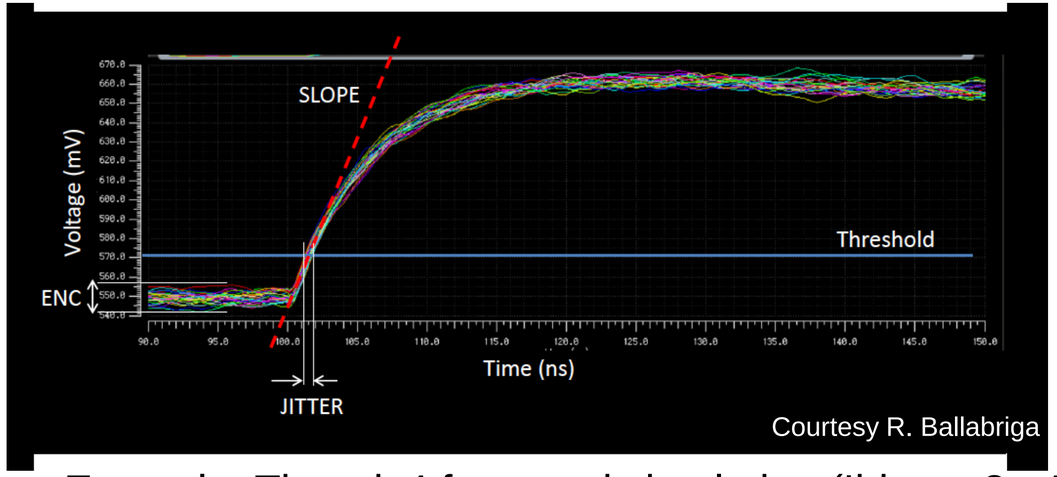
$$\frac{dv_{out}(0)}{dt} \sim \frac{Q_0\, g_m}{C_I(C_L + C_M)}$$

Optimal for:

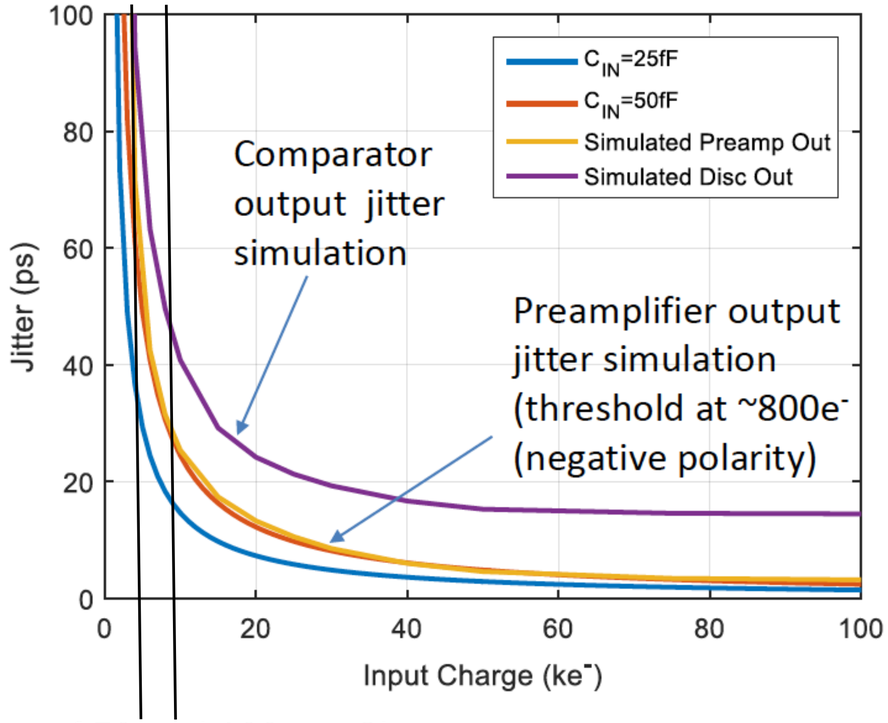
- Large input signal (Q_0)
- Large gain (g_m), g_m increases with ampl. bias current
  - at the cost of more power
  - how much power can we afford?
- Low capacitance (both input and internal)

Other key ASIC figures (size 2 cm^2)

	@5.1 mm	@12.5 mm
TID	24 MGy	3 MGy
pitch	55 μm	41 μm
Bandwidth	~ 250 Gbit/s	~94 Gbit/s
hottest pixel	350 kHz	40 kHz



Example: Timepix4 front-end simulation (Ibias = 3 uA)

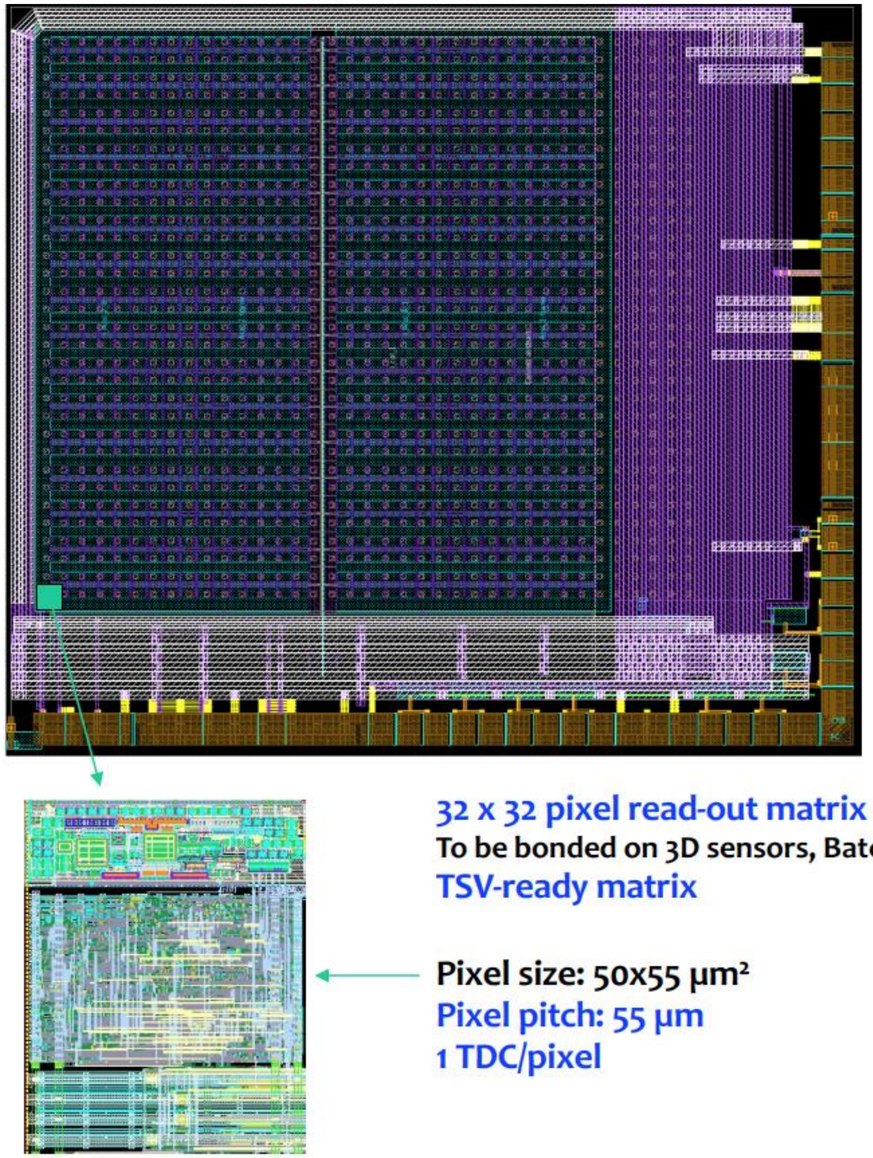


charge of 50 and 100 μm Si

Fine pitch fast timing ASICs : TimeSPOT

TIME and SPace real-time Operating Tracker

See previous talk by Adriano Lai



32 x 32 pixel read-out matrix
To be bonded on 3D sensors, Batch #2
TSV-ready matrix

Pixel size: 50x55 µm²
Pixel pitch: 55 µm
1 TDC/pixel

- Addressing the VELO upgrade-II challenge
- 28 nm technology
- Optimised for 3D-trench sensors
- 55 µm pitch
- 25% of area for Analog front-end
- TDC per cell
- Submitted last week

simulated performance:

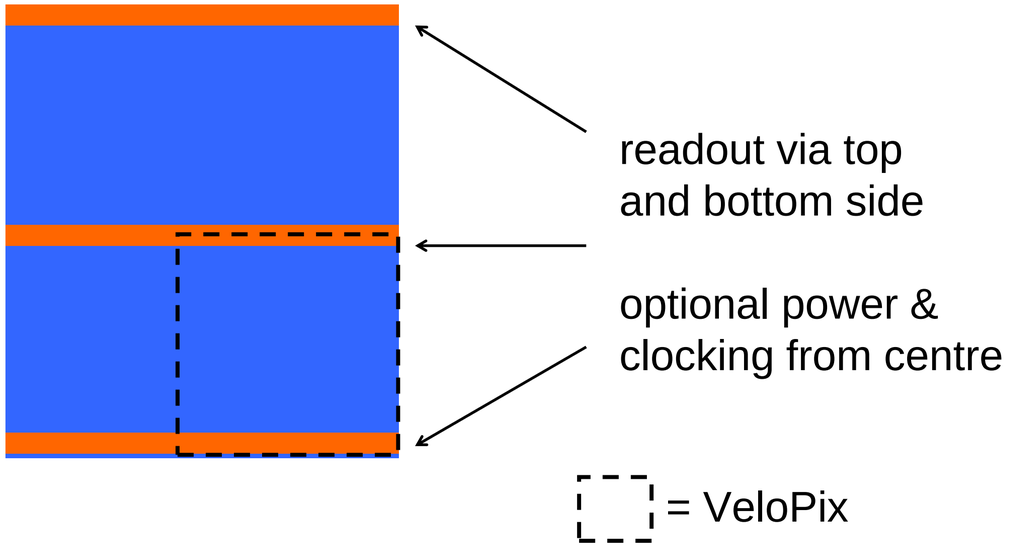
HP stands for High (or maximum) Power, i.e. ≈ 23 µW / cell

	Schematic		Layout	
Power	Nominal	HP	Nominal	HP
Slew-Rate [mV/ns]	380	540	250	360
RMS noise [mV]	5.0	4.9	3.9	3.8
Jitter [ps]	13.2	9.1	15.6	10.5
Power per channel [µW]	18.2	31.5	18.6	32.9

Full scale ASIC with fast timing capabilities

Timepix4 (Medipix4 collaboration, 2019)

- General purpose ASIC
- 65 nm CMOS
- 512x448 pixels, 55 μm pitch
- Per pixel TDC, shared oscillator (8 pixels)
- TDC resolution 200 ps / 60 ps (bin / rms)
- 160 Gbit/s output bandwidth (16x10)
- 24.7 mm x 28.2 mm



- Timepix4 exists!
- Similarly to Timepix3, it will be our ‘tool’ for sensor characterisation at the system level
- Complementary to the smaller scale prototypes (e.g. 3x3, 5x5, NxN pixels)

But, not every pixel is the same …

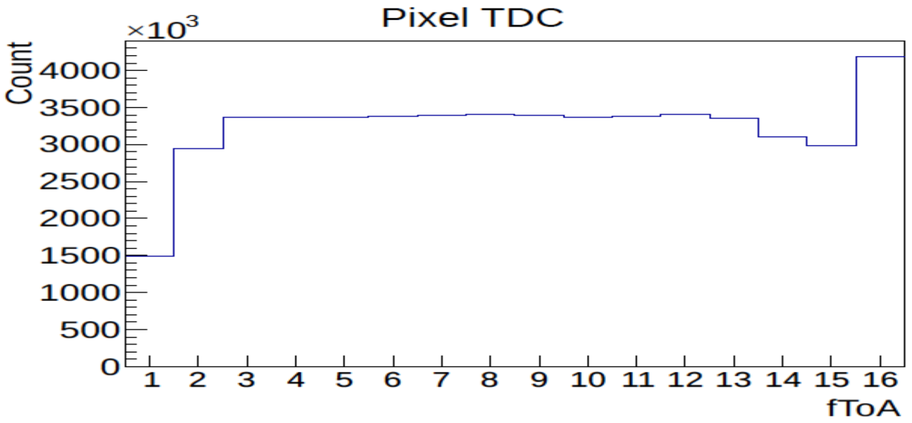
- If you “zoom in” everything will look grainy

- Example from Timepix3 telescope
- Time bin of 1.56 ns -> binary resolution 450 ps
- TDC bin-to-bin variations
- Pixel-to-pixel time offsets much larger than resolution

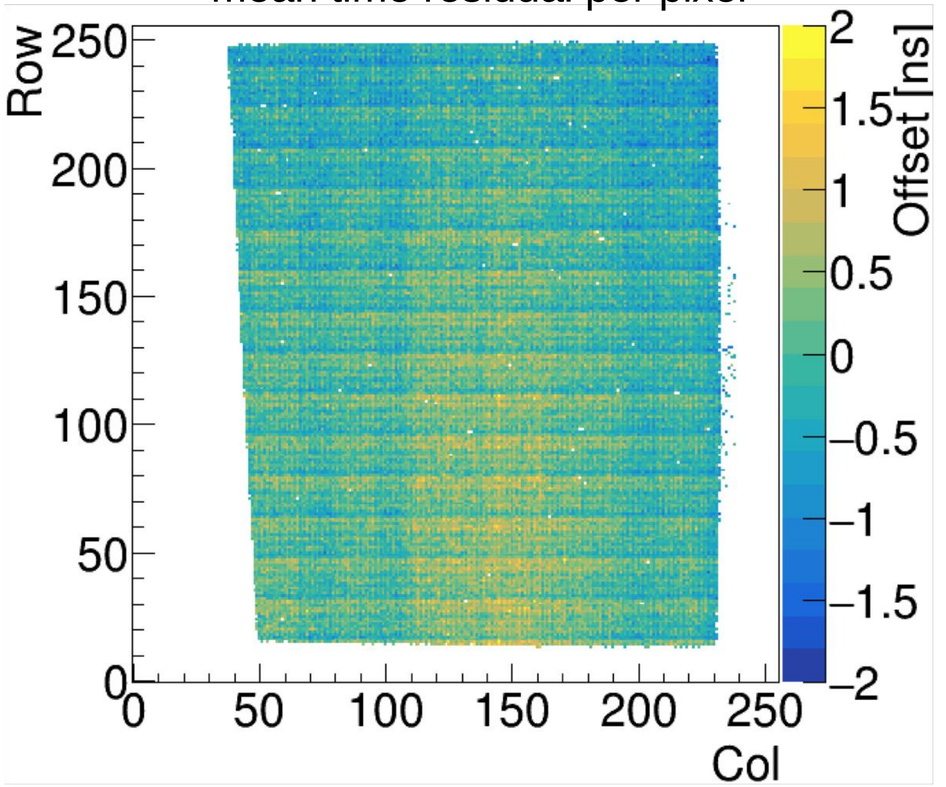
- Static offsets and timewalk can be corrected for
- Ultimately we only care about stability

But:

- Extra info requires on-chip logic and/or bandwidth
- How to determine tuning parameters?
- Is on-chip correction possible?



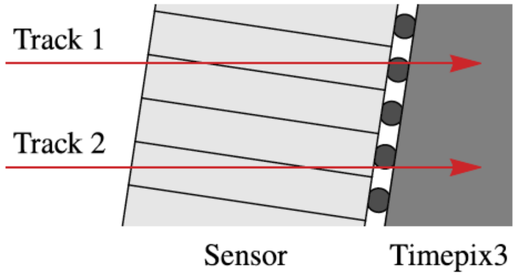
mean time residual per pixel

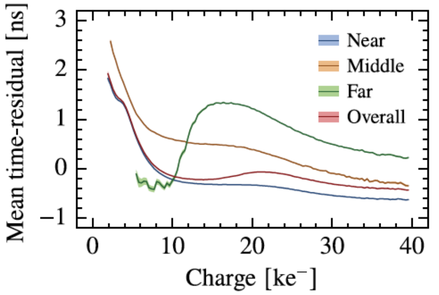


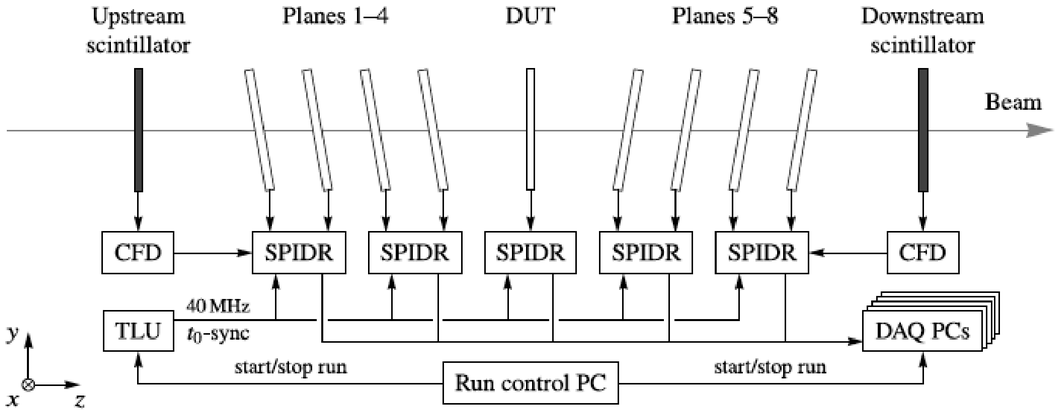
[K. Heijhoff: 2020 JINST 15 P09035]

System level timing

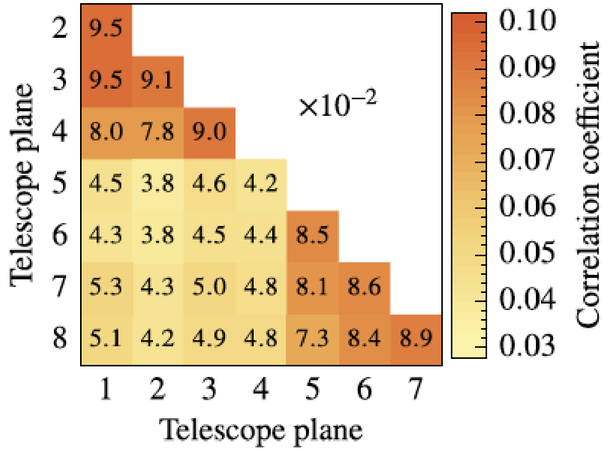
- We often assume that things simply scale by sqrt(N), e.g. hit to track time, track to vertex
- Correlation of time measurements can easily affect the scaling
  - e.g. due to clocking effects, both on-chip and across detector
- As example, a timing study of our Timepix3 telescope
- Note that the telescope is not really optimised for timing
  - order 1 ns RMS per plane before any corrections
- But correlations due to poor clocking already appeared



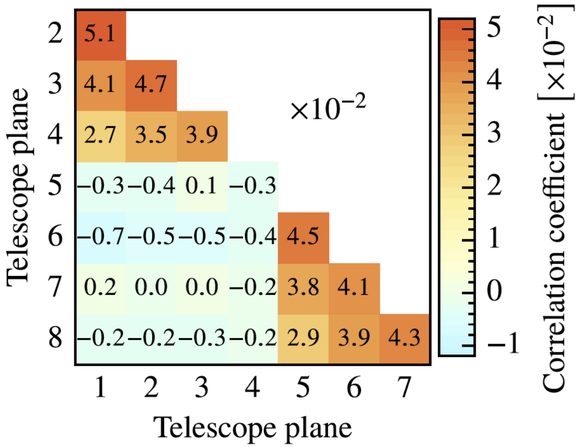




plane to plane correlations
after intercept corrections

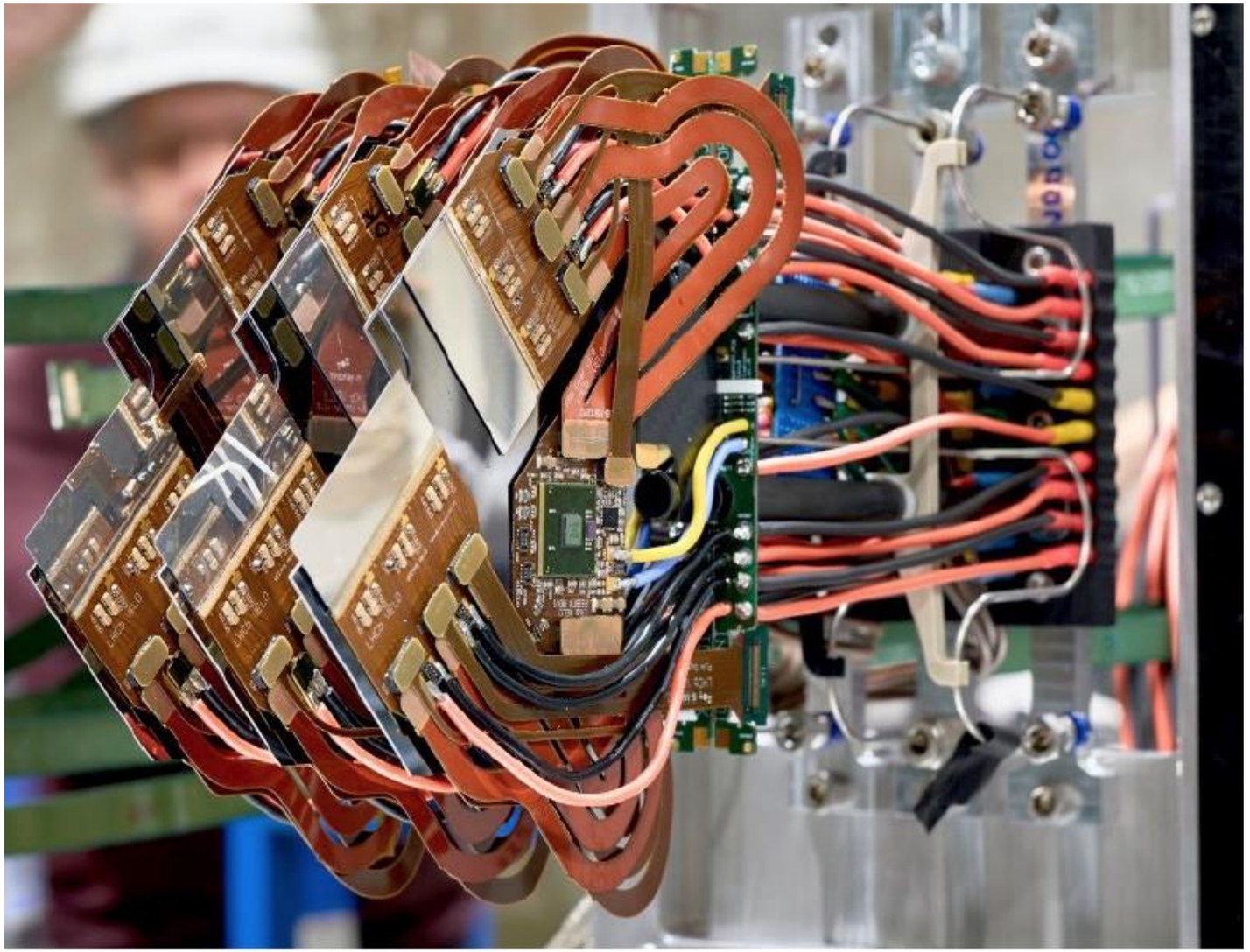


plane to plane correlations
after offline clock corrections



[K. Heijhoff: 2020 JINST 15 P09035]

The challenge doesn’t stop after the sensor and ASIC

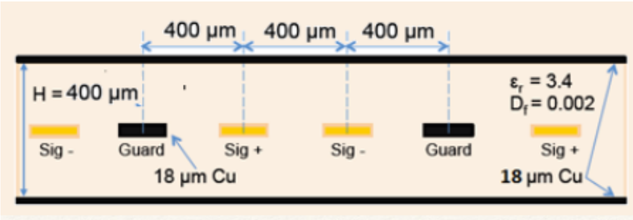


- Data rates
- Powering (in vacuum)
- Cooling
- Mechanics

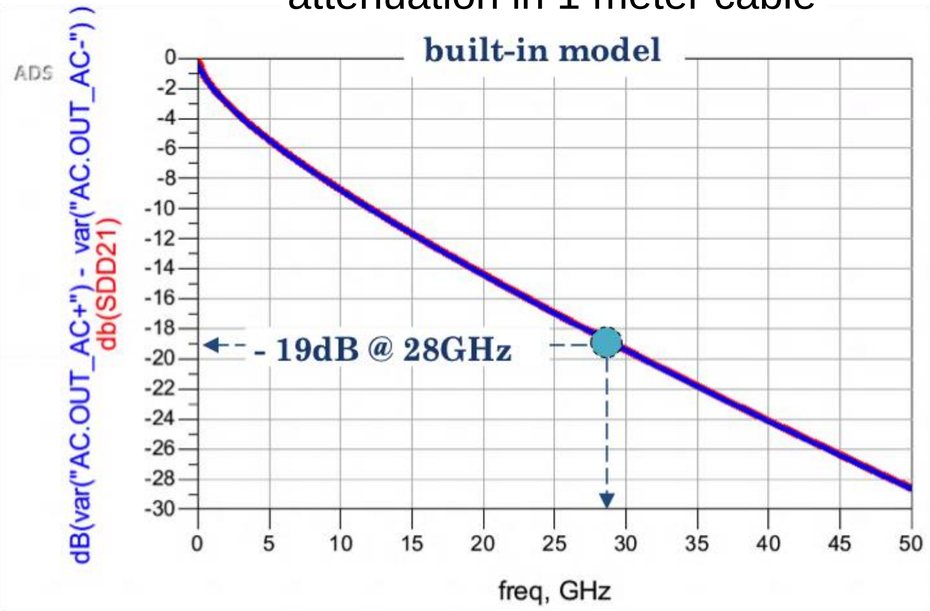
Data transmission challenge

- Smaller ASIC technologies are very performing
- Low power 28+ Gbits/s serialisers seem feasible in 28 nm
- But ‘our’ cable technology does not scale in the same way
  - has to be radiation hard, vacuum compatible
- -> bridging the first 0.5 – 1 meter in vacuum is a challenge
- Large losses in the dielectric

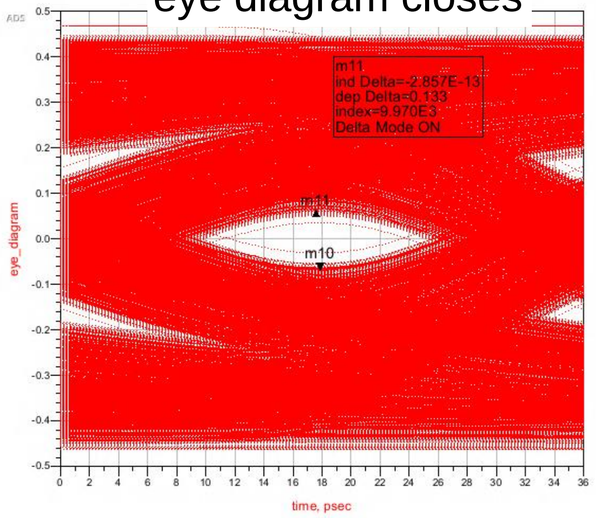
stripline cross section



attenuation in 1 meter cable

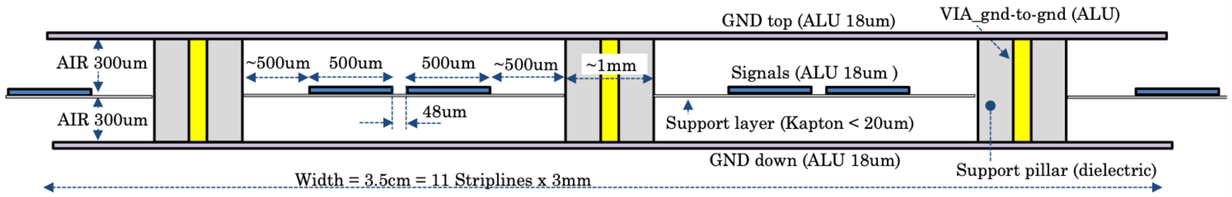


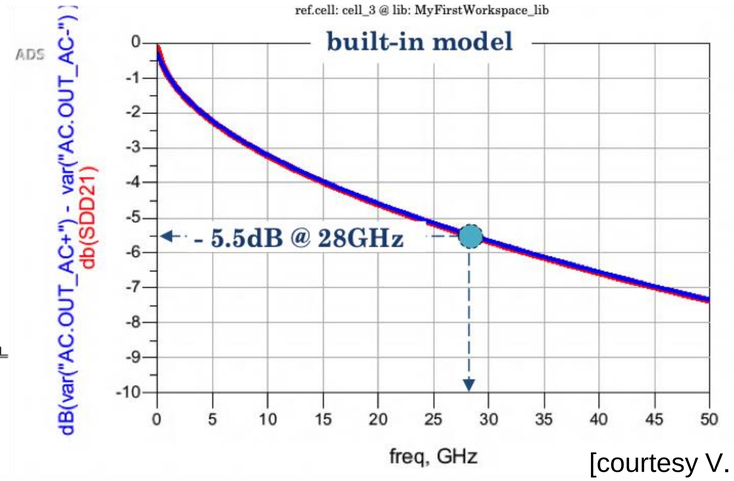
eye diagram closes

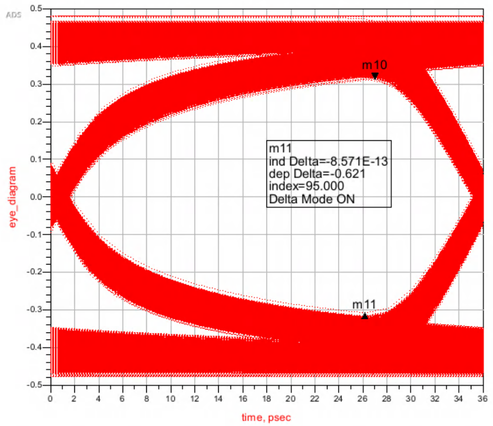


What can we do about it?

- Get rid of most of the dielectric?
- Air-filled / suspended striplines
- Technically possible, but very expensive

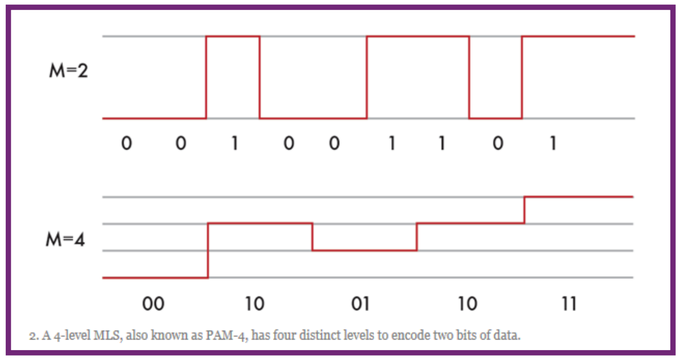


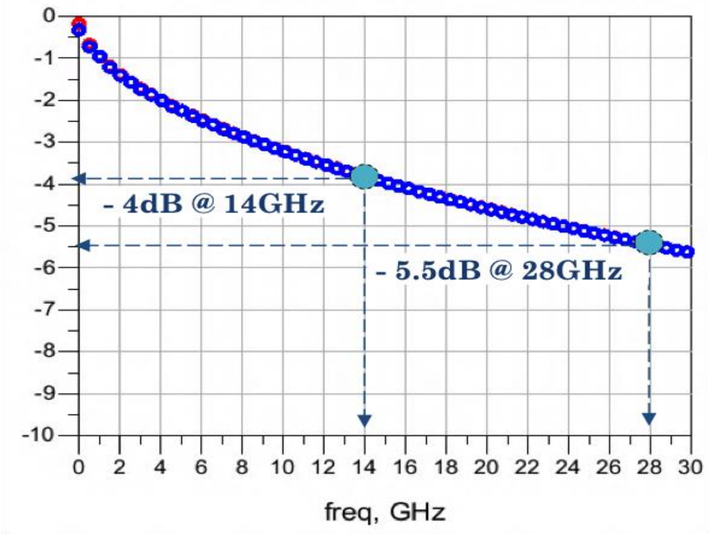




[courtesy V. Gromov]

- Multi-level signalling at lower speed?
- e.g. PAM4, probable little/no benefit for us





3 levels -> 33% signal = -9dB

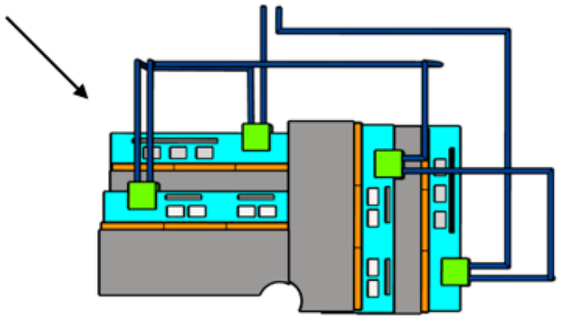
PAM4: -4 dB – 9 dB = -13 dB

compared to -5.5 dB

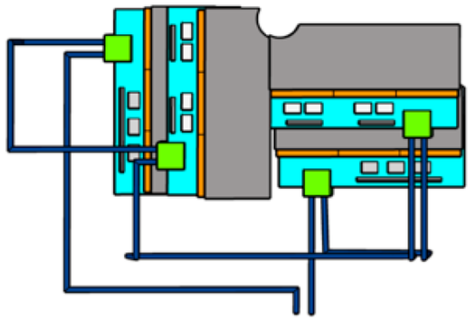
- Or can/dare we go ‘optical’ near the ASIC?
- Versatile link (VCSEL) reaches 1 MGy / 10^{15} n_{eq}, or Mach Zehnder Modulators

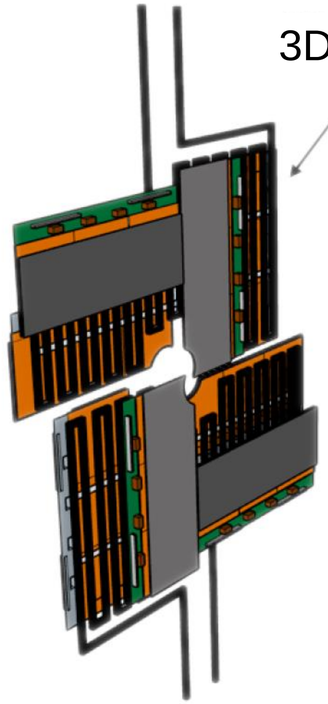
Cooling for Upgrade-II

- VELO (prime) introduced bi-phase CO_2 cooling in HEP
- VELO Upgrade-I: CO_2 cooling via Silicon micro-channel plates
  - Elegant solution, but large micro-channel plates are expensive
- Upgrade-II modules will dissipate more power
  - CO_2 cooling might not run cold enough
  - Bi-phase Krypton could be a possibility

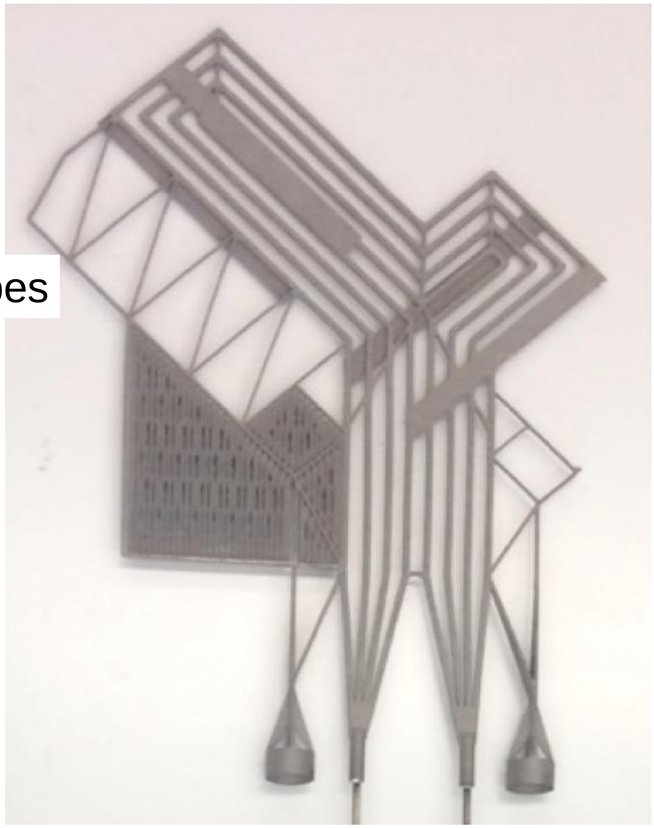


smaller micro-channel plates
to reduce cost



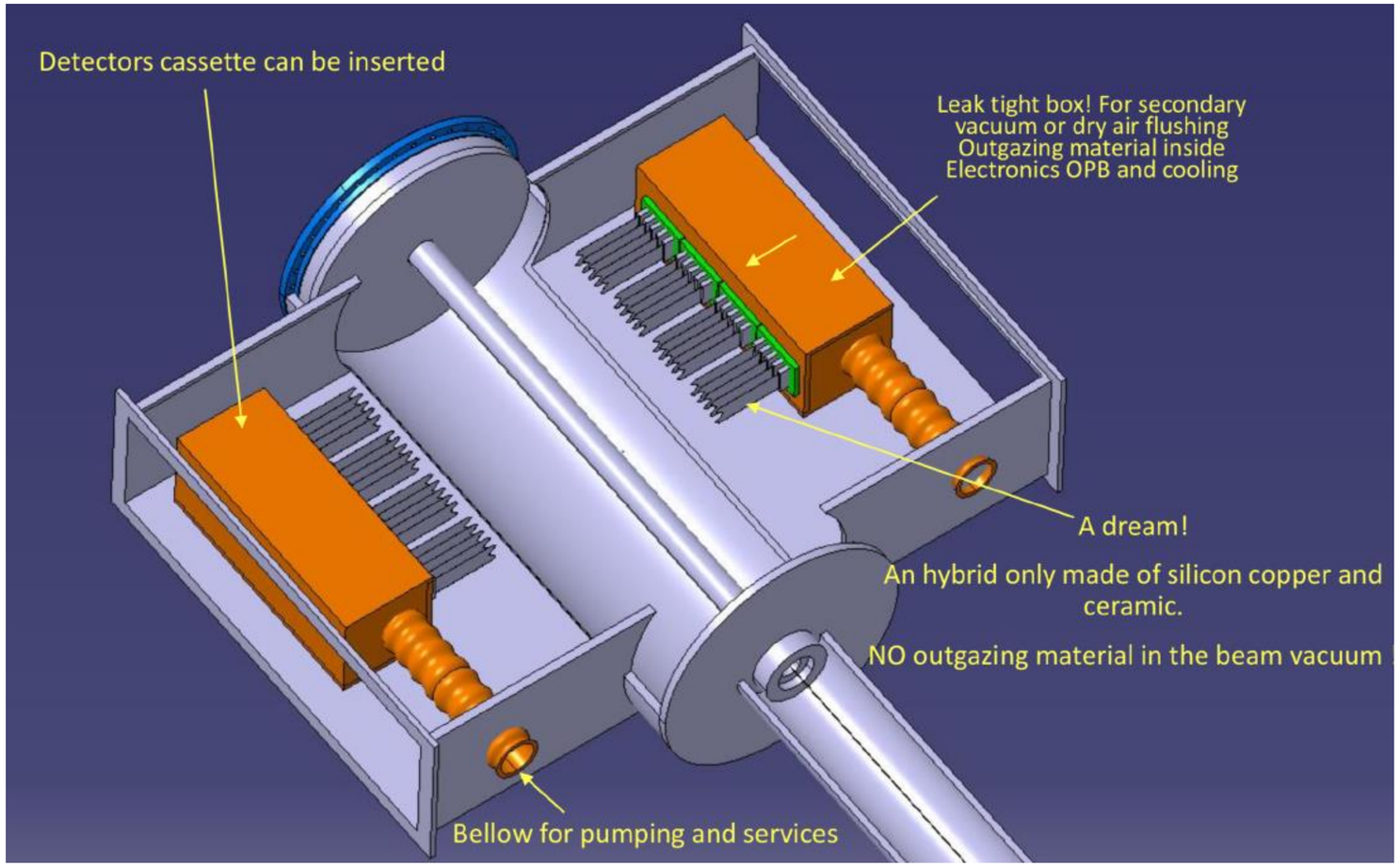


3D printed titanium pipes



3D titanium printed pipes already prototyped for Upgrade-I

Mechanics



- What if in a few years from now (end of R&D phase) there is no sensor that provides sufficient signal after $6x10^{16}$ n_{eq}?
- Considering (bi-)annual replacement of detector
- Major impact for mechanical design
- Detector modules that can swapped during technical stops

Summary

- LHCb is planning another luminosity upgrade (II), to be installed in 2031
- Timing at high lumi is essential to keep the same performance as Upgrade-I
- 4D tracking vs. timing layer is subject to further studies
- Challenges are the (non-uniform) radiation, spatial and temporal resolution, data rate, cooling, online reconstruction, …

- R&D ramping is up
- Currently in exploratory phase where non of the technologies can be excluded