


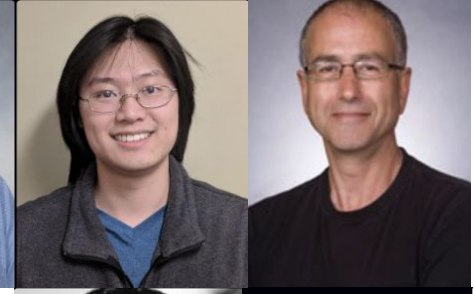



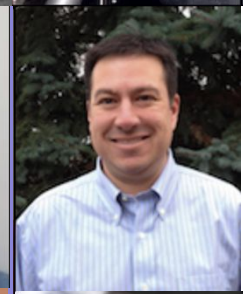

Innovative Algorithms (IA)

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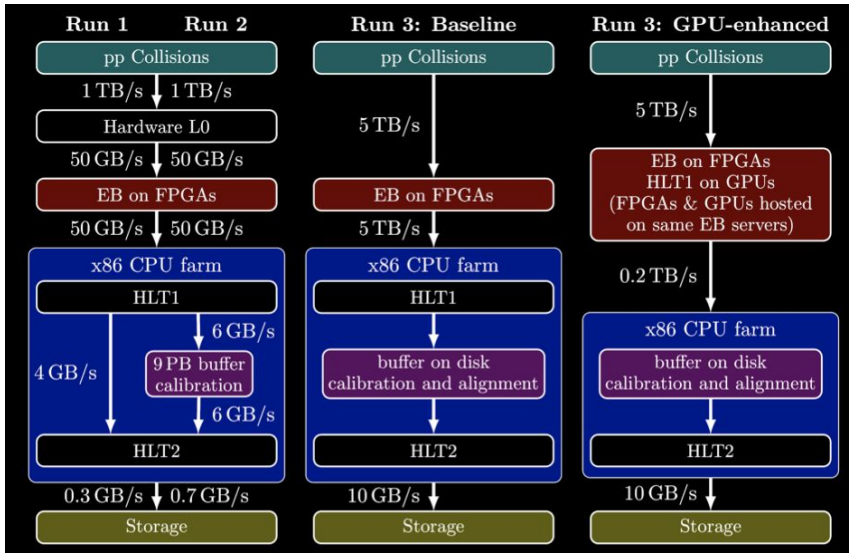
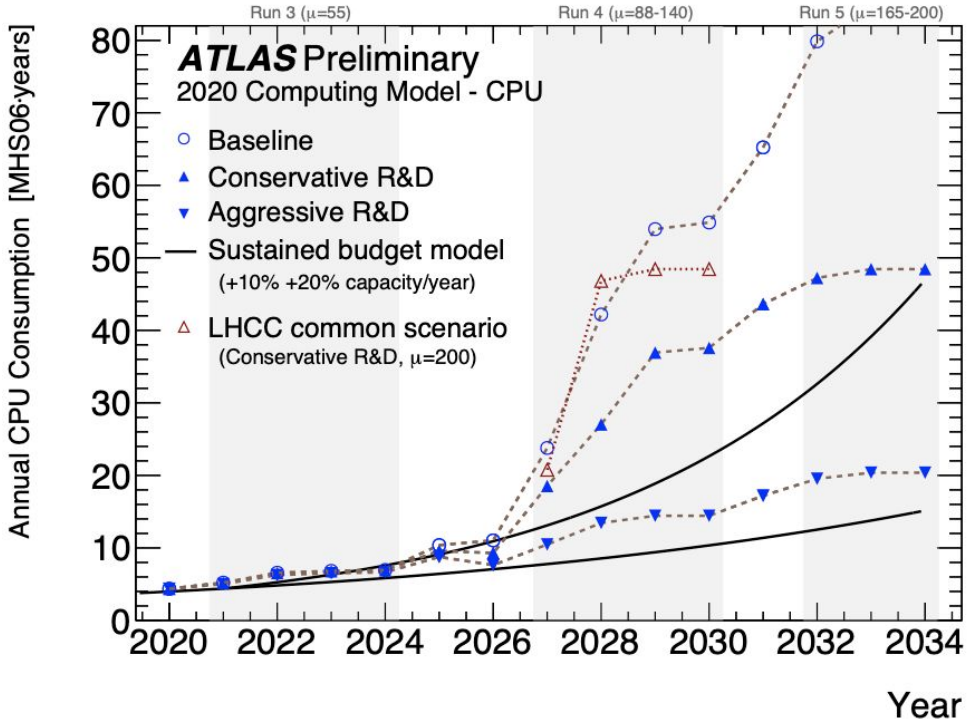
Co-Leads


Computational challenge at the LHC

Evolution of LHCb HLT1 for Run 3





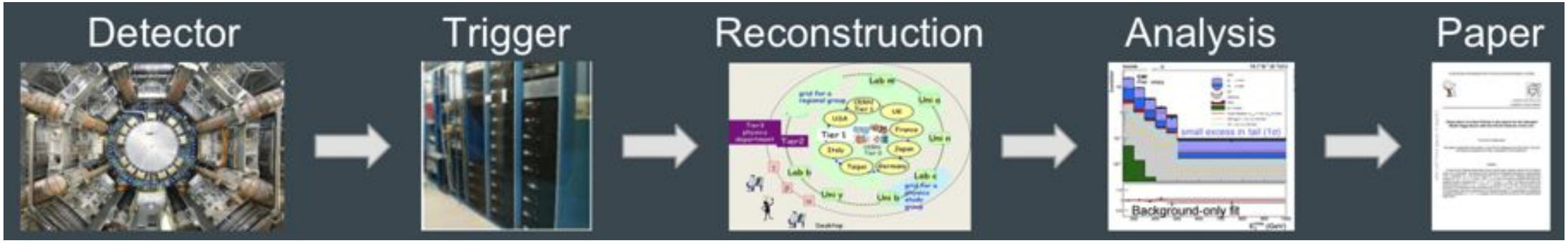
The **real-time processing** in the trigger and **reconstruction** of raw detector data (real and simulated) represent major components of today's computing requirements in HEP.

Focus Area: Innovative Algorithms

Developing and reengineering algorithms for critical HEP applications.

- **Software trigger**: Quasi-real-time processing of detector data to select most "interesting" events (reduce rate by 100x).
  - *Input rate is 1-30 MHz, required latencies are O(seconds).*
- **Offline reconstruction:** Processing raw data for analysts O(100) billion events per year processed by a globally distributed computing facility

The distinction between these areas is blurring given the evolution in software and hardware. It is natural to focus on both



IA goals towards HL-LHC

Achieving the physics and computational performance needed for HL-LHC will require significant algorithmic innovation and software engineering research to take advantage of **vector processors**, **hardware accelerators** and other **emerging technologies**.

Research in Innovative Algorithms aims to

- Achieve **technical improvements** in trigger or reconstruction algorithms to meet HL-LHC requirements without **cost** increases or ceding **physics** performance
- Focus efforts to establish **best practices software** and for the effective use of **evolving computing hardware**
- Enable **new algorithmic approaches** to provide substantial gains in physics and computational performance.

As a group Innovative Algorithms aims to play a **leading role** in solving the “HL-LHC computing problem” and hence in the development of the computing models

Major Activities and Goals

Developing tracking algorithms for HL-LHC

Determining charged-particle trajectories ("tracking") requires most CPU in reconstruction

- Develop more efficient algorithms
- Develop more performant algorithms

Re-engineering algorithms for hardware accelerators

Hardware accelerators are the way forward to speed up and reduce infrastructure cost

- Use of hardware accelerators for tracking
- ML on accelerators in realistic HEP apps

Exploiting major advances in machine learning (ML)

Capitalize on industry and data science techniques and tools

- Investigate new HEP applications of ML
- Apply new ML techniques to HEP

IA projects are all part of broader efforts

- Critical algorithms for software trigger and event reconstruction applications are rarely the work of one individual or one group.
- Collaborations allow the Institute to enable a **broader set** of topics important for HL-LHC. Our researchers are working
  1) As well-integrated parts of international experimental collaboration (e.g. CMS, ATLAS, LHCb) and multi-experimental teams (e.g. FASTML, ACTS)
  2) With researchers funded by the US operations programs, DOE (ExaTrkX), as well as other NSF projects (eg, CSSI, HDR)
- These collaborations let the Institute **lead the community** towards Institute goals critical for the success of HL-LHC, and help ensure that successful projects will be **sustained** by a broad community.
- IA has defined with the individual PIs clear IRIS-HEP contributions and deliverables within these broad collaborations

IA projects in a slide..

1. PVFinder : ML approach to finding primary vertices (UC, MIT): Working to establish to what extent a better PV performance (physics, technical) can be achieved via an ML approach?
2. Allen framework: Configuration and monitoring of GPU framework (MIT). Due to the Allen project results, LHCb recently adopted a GPU-based first-level trigger (HLT1) for Run 3.
3. mkFit: Efficient track finding on modern architectures (UCSD, Princeton, Cornell). Has achieved large speed ups in track building. Focused on deployment into CMS HLT for Run 3.
4. FPGAs and ML for calorimetric reconstruction (MIT). Identified use case algorithms and prototypes for ML algorithms using FPGAs “as a service”
5. ACTS tracking (UC-Berkeley, Stanford). CPU/GPU implementations of Kalman filter, seed finding, ambiguity resolution in ACTS framework.
6. GNNs for tracking (UIUC, Princeton): Recently started R&D on applying graph neural networks to (pixel) tracking. Moving towards an increased collaboration with ExaTrkX.
7. ML for Jet algoirhtms (NYU): Hosted ML4Jets; Developing common benchmarks

Ideas for new initiatives? Bring a slide on Thursday

IA related events

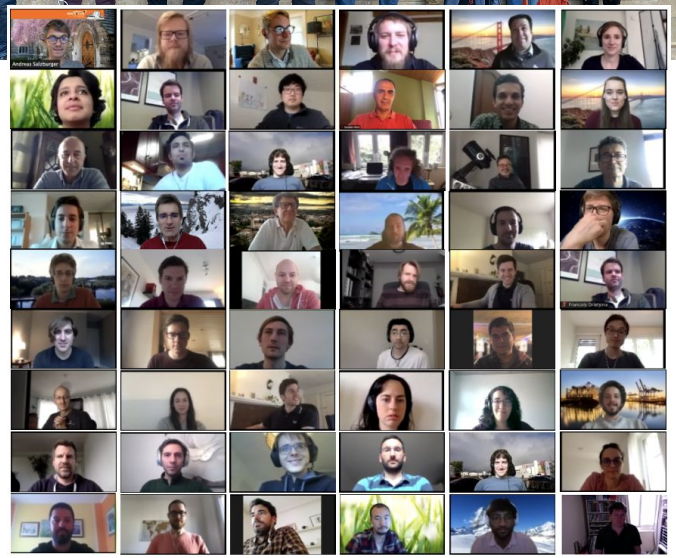
Events like ML4Jets and CTD2020 essential for building collaborations towards HL-LHC. Lets think ahead about continued community engagement.

- CTD/WIT2021 is planned to be at Princeton… (COVID allowing..)

We've used topical meetings to stay informed on the typically dispersed projects

- We've generally had limited attendance from team members. Different approaches that would be more attractive to you?

ML4Jets @NYU



CTD2020@~~Princeton~~ (ZOOM)

Towards milestones / metrics

Aims for Y3-5:

- If not already, demonstrate that your R&D is solving an important problem
  - *Articulate what is the potential impact.*
  - *Show that your approach is of interest to >=1 LHC experiment (and fits into its potential future computing model planning)*
  - *Show how your approach has more general applicability beyond your experiment*
- If not already, demonstrate that your R&D has promise to solve Run 3 (LHCb) or HL-LHC (Atlas/CMS) physics or technical performance gaps:
  - *Focus on being able to compare to 'state-of-the-art" approaches*
  - *Describe how the performance of your approach will be measured*
  - *Articulate your alternative approaches being taken in your experiment or elsewhere*
- Set quantitative goals
  - *We are asked 'when", 'by how much" especially in the context of performance demonstrations and experimental integrations. We understand its R&D, but we need to continue establishing targets.*
- Explain the Y4 or Y5 "big picture" goals of your R&D

FPGAs for online/offline processing

IRIS-HEP (and in particular IA) has a number of projects that have as their primary or secondary goal to enable the use of FPGAs.

> Being 2 years in, we propose to formulate an Institute view on the feasibility and roadmap for the use of FPGAs in lieu of CPUs or other hardware accelerator technologies
>
> Specifically, questions such as:
>
> 1. What sorts of algorithms most well suited for FPGA?
> 2. How easy is the programming model for “interesting” algorithms to HEP?
> 3. What are current estimates of throughput per unit cost relative to CPU and GPU. What is known about relative technology evolutions?
> 4. What is the architecture of a compute facility?

We would like to organize a first internal discussion this summer.. FPGA use of at scale with production algorithms driven by experimental frameworks could be a possible grand challenge opportunity if we identify them as critical for HL-LHC computing models (collaboratively with other projects in HEP)