Status of the CNM LGAD Runs

The 37th RD50 Workshop

18-20 November 2020 (Zagreb, online)

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R&D lines towards the final ETL sensor @ CNM

L1 - Substrate: 6-inch epitaxial wafers (6LG3)

Motivation: Overcome the limited SiSi or SOI wafer availability.

Action: Engineering run on 6-inch epitaxial wafers (just completed)

L2- In-wafer uniformity of the multiplication layer (AIDA2020v2)

Motivation: Improve the non-uniform activation of the multiplication layer

Action: replacement of the annealing furnaces for a more uniform dopant activation/diffusion (in progress, to be completed by March 2021)

L3 – Radiation Tolerance Optimization (6LG3, AIDA2020v2)

Motivation: Ensure the required charge range before and after irradiation

Action: Sensor's Optimization runs AIDA2020v2 and 6LG1 (radiation tolerance study in progress)

L4-Interpad optimization (AIDA2020v2)

Motivation: Minimize the non-gain interpad region

Action: Study different interpad geometries and its effects on breakdown voltages

L5 - Large sensor's Yield (6LG3-CMS)

Motivation: Realistic estimation of ETL sensor's yield , detailed specification of the pre-production detectors

Action: dedicated manufacturing run with final ETL design (in progress to be completed by April/May 2021)

I. Vila - ETL Sensor Meeting November 16th 2020

Current Status of the CNM LGAD Runs

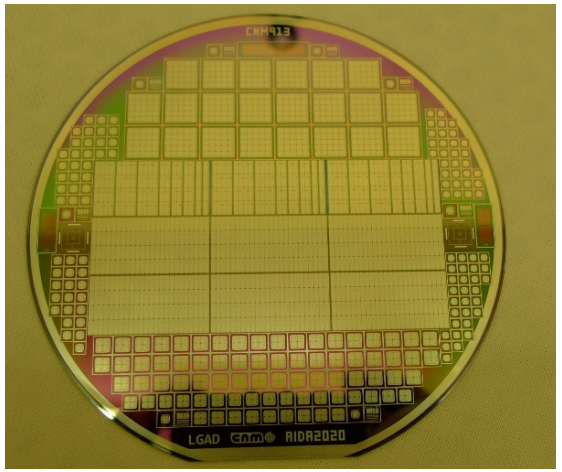
Run	Description	Clean Room Step
12916	4” AIDA 2020 LGAD	Completed Electrical Characterization in Progress
13002	6” Epi-Wafers LGAD (6LG3)	Completed Electrical Characterization in Progress
13840	6” ATLAS-CMS Common Run (6LG3)	Step 39/97 (JTE) Waiting for New Diffusion Furnace
13911	6” AC-LGAD (6ALG1)	Step 23/116 (P-Stop) Waiting for New Diffusion Furnace

Run 12916: LGAD AIDA 2020 v2 Specifications

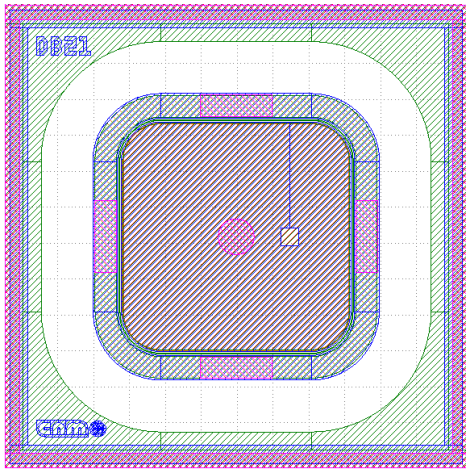
- **Four wafers** with the same dose/energy parameters.
- **4-inch** p-type high resistivity 50 μm **Si-Si wafers.**
- IV/CV Measurements on-wafer.

Wafer	Thickness (μm)	Dose (at/cm^2)	Energy (keV)
1-4	50	Medium	Low

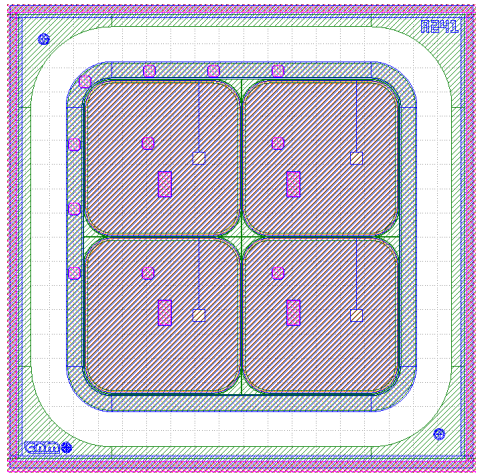
Wafer



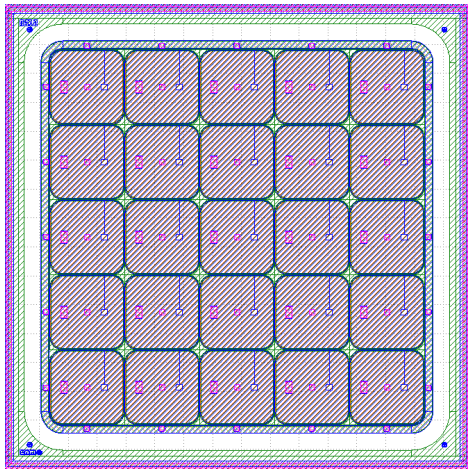
Pad diodes



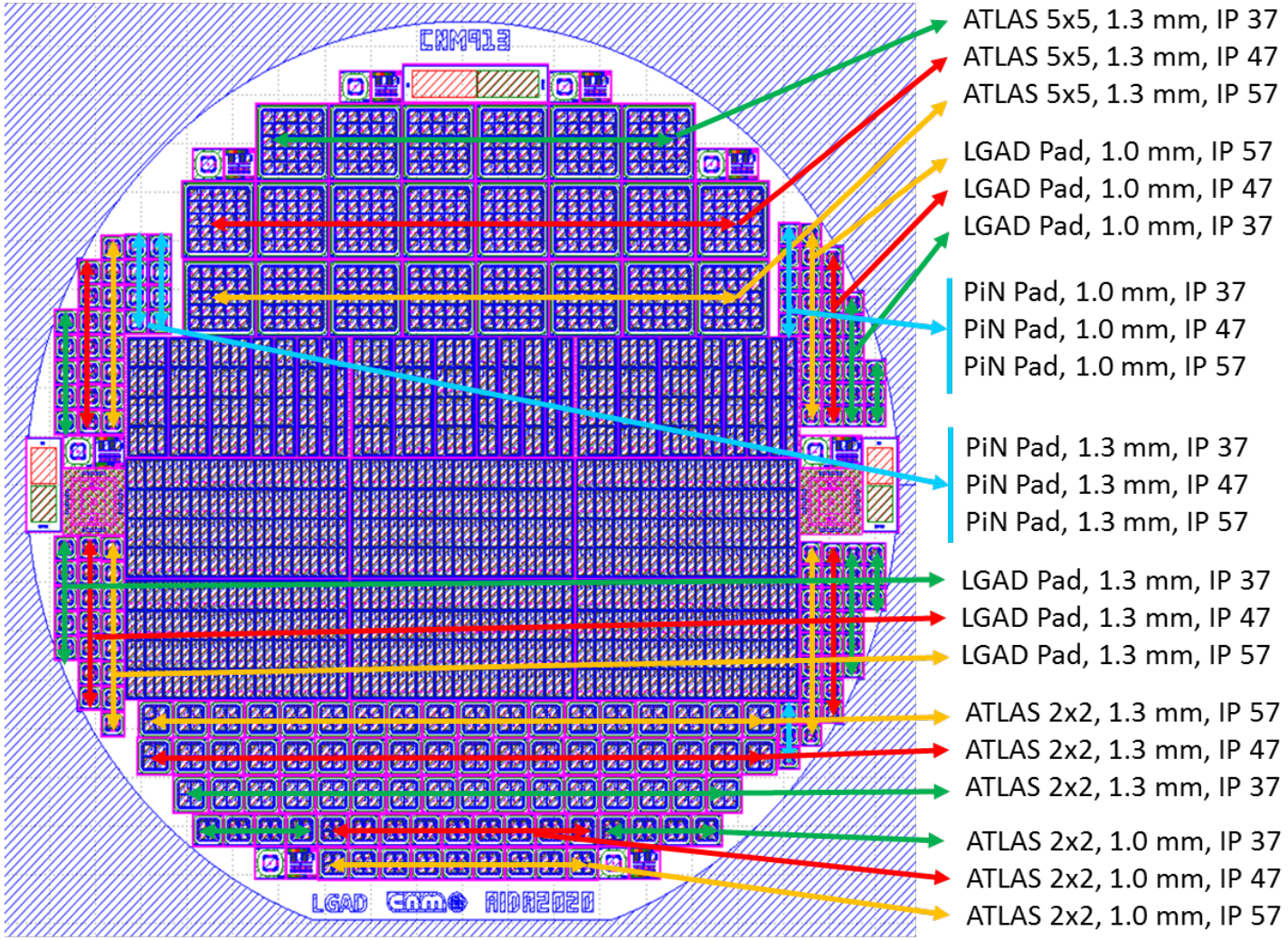
2x2 Array



5x5 Array



Run 12916: LGAD AIDA 2020 v2 Specifications



ATLAS 5x5, 1.3 mm, IP 37
ATLAS 5x5, 1.3 mm, IP 47
ATLAS 5x5, 1.3 mm, IP 57

LGAD Pad, 1.0 mm, IP 57
LGAD Pad, 1.0 mm, IP 47
LGAD Pad, 1.0 mm, IP 37

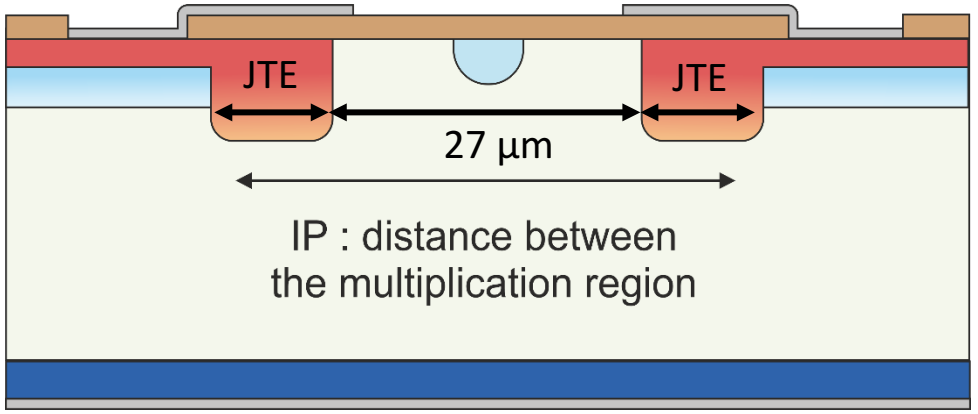
PiN Pad, 1.0 mm, IP 37
PiN Pad, 1.0 mm, IP 47
PiN Pad, 1.0 mm, IP 57

PiN Pad, 1.3 mm, IP 37
PiN Pad, 1.3 mm, IP 47
PiN Pad, 1.3 mm, IP 57

LGAD Pad, 1.3 mm, IP 37
LGAD Pad, 1.3 mm, IP 47
LGAD Pad, 1.3 mm, IP 57

ATLAS 2x2, 1.3 mm, IP 57
ATLAS 2x2, 1.3 mm, IP 47
ATLAS 2x2, 1.3 mm, IP 37

ATLAS 2x2, 1.0 mm, IP 37
ATLAS 2x2, 1.0 mm, IP 47
ATLAS 2x2, 1.0 mm, IP 57



The distance between the JTE remains the same, we are changing the JTE width.

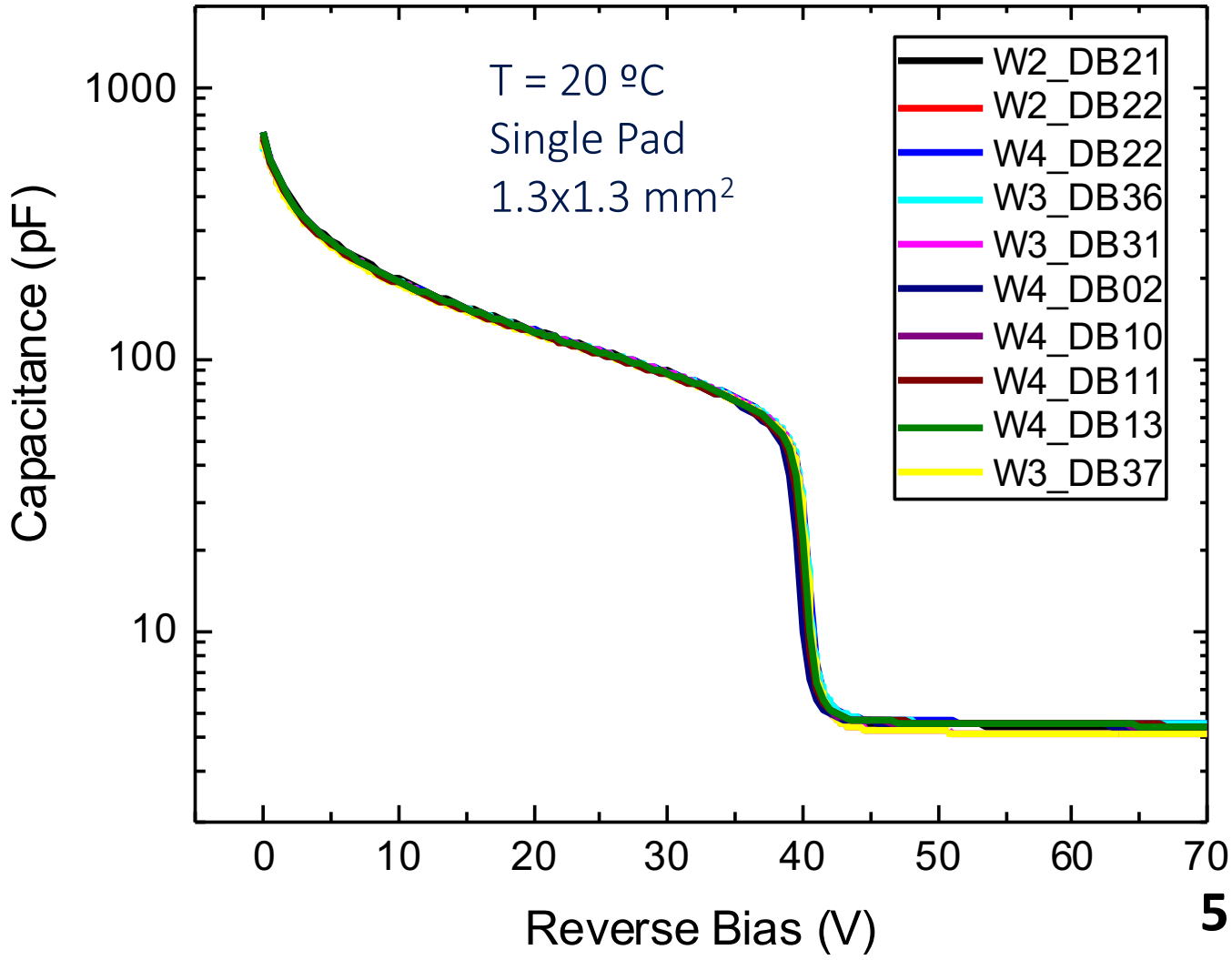
- IP 37 → JTE = 5 µm
- IP 47 → JTE = 10 µm
- IP 57 → JTE = 15 µm

Run 12916: LGAD AIDA 2020 v2 Capacitance Measurements

Wafers 2,3,4 Single Diode
1.3x1.3 mm² @ 20°C

High uniform depletion of the gain layer

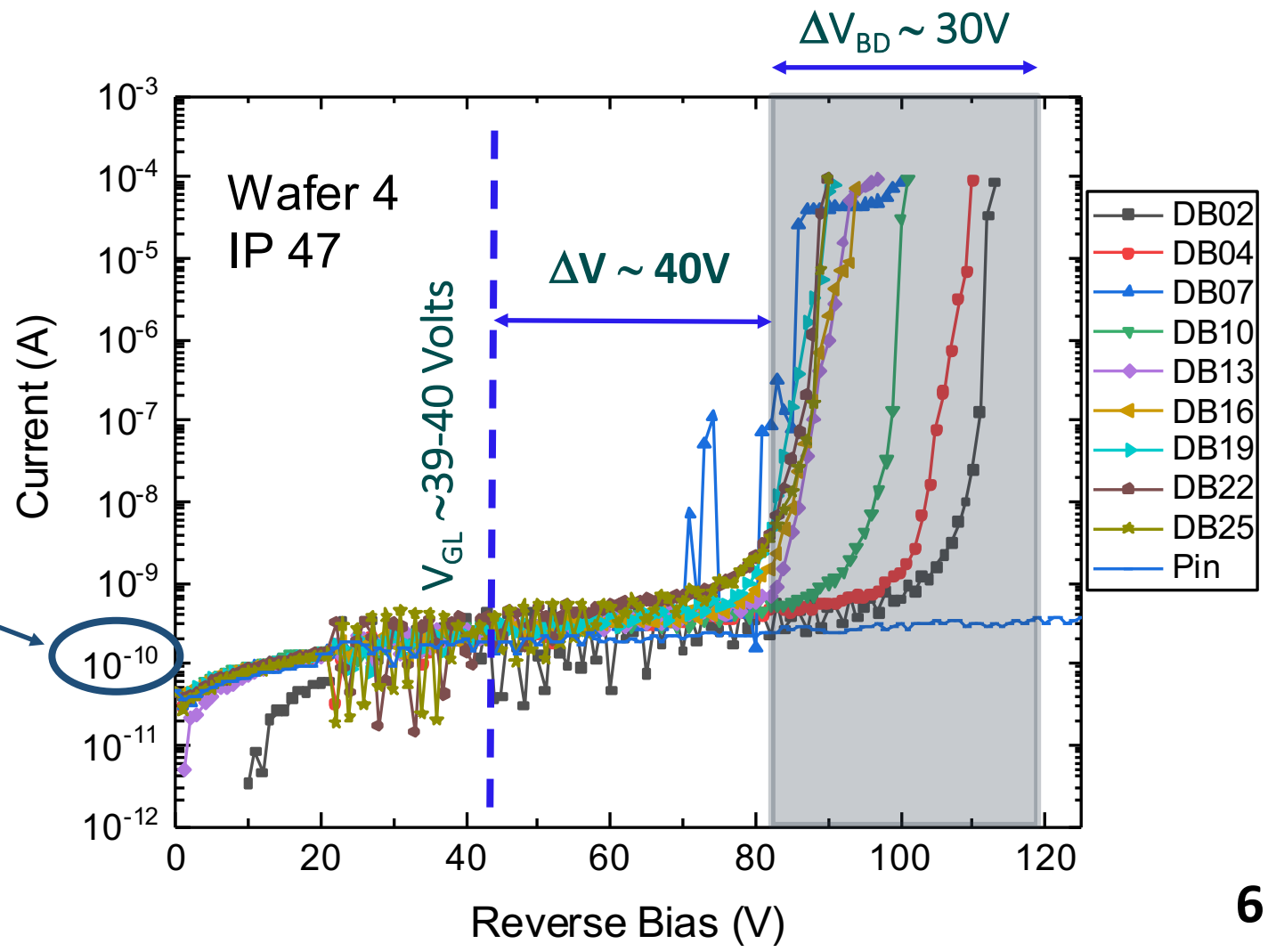
V_{GL} ~ 39-40 V



Run 12916: LGAD AIDA 2020 v2 Current-Voltage Measurements

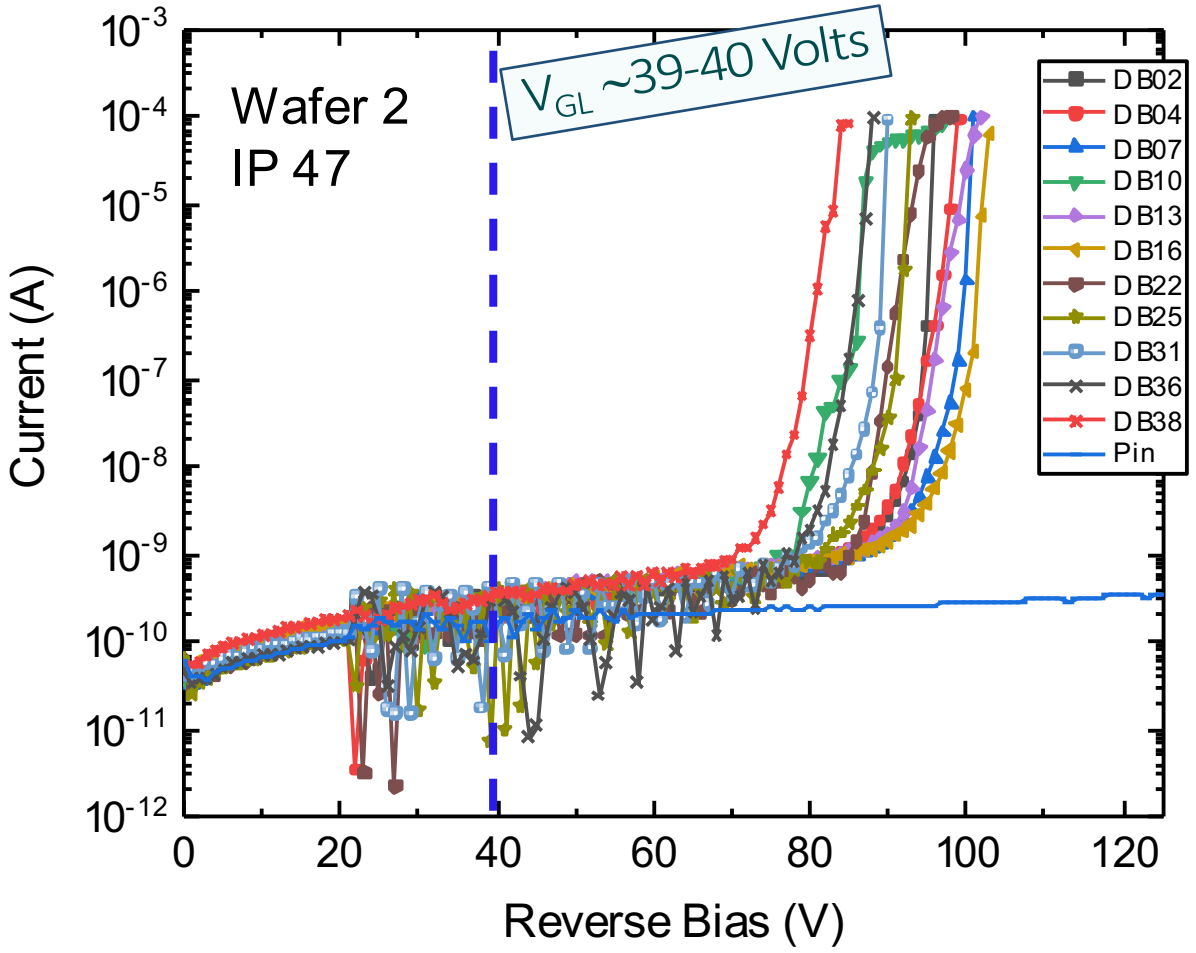
Wafer 4 Single Diode
1.3x1.3 mm² IP47 @ 20°C

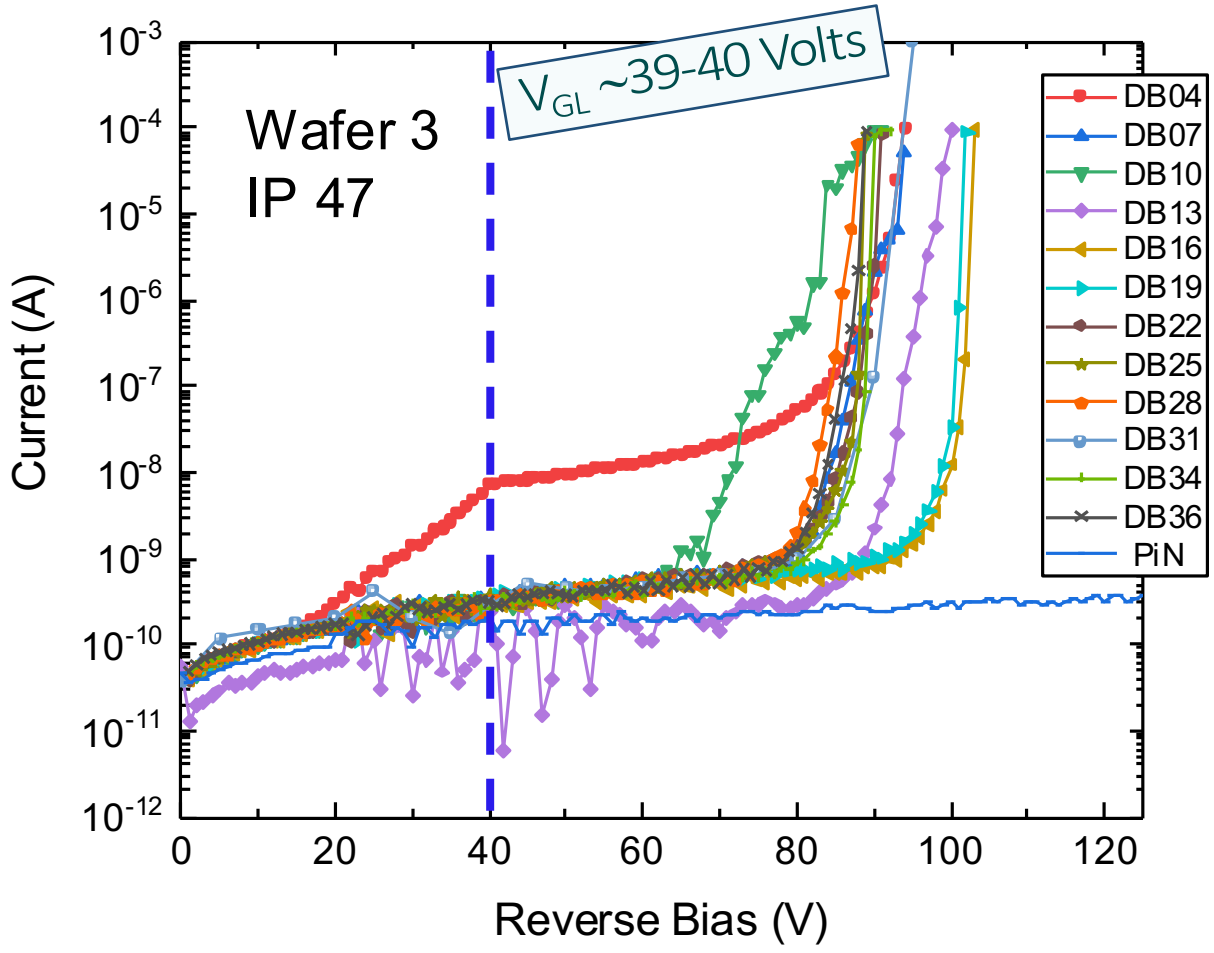
Reverse current around 100 pA
(consistent with PIN diode)



Run 12916: LGAD AIDA 2020 v2 Current-Voltage Measurements

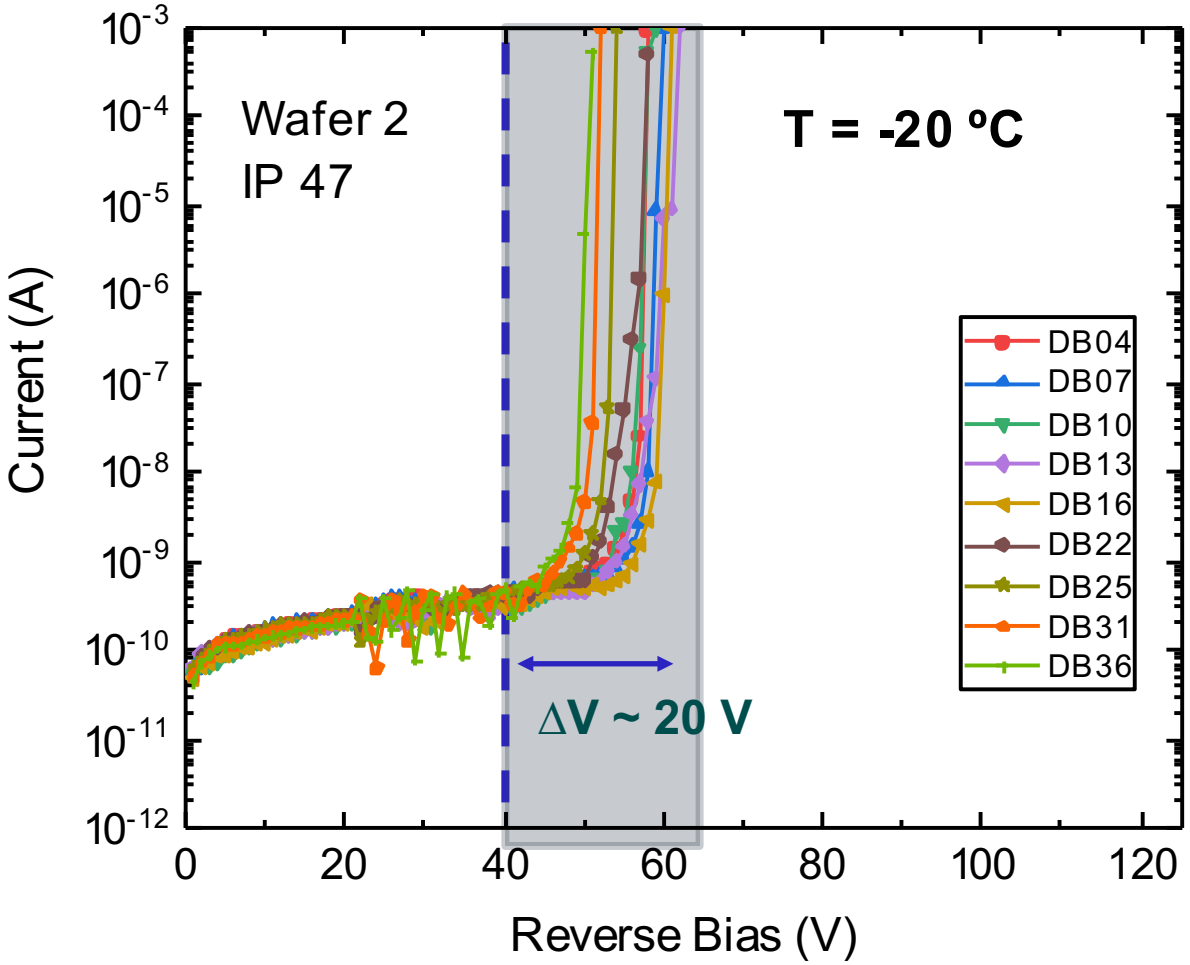
Wafer 4 Single Diode 1.3x1.3 mm² IP47 @ 20°C

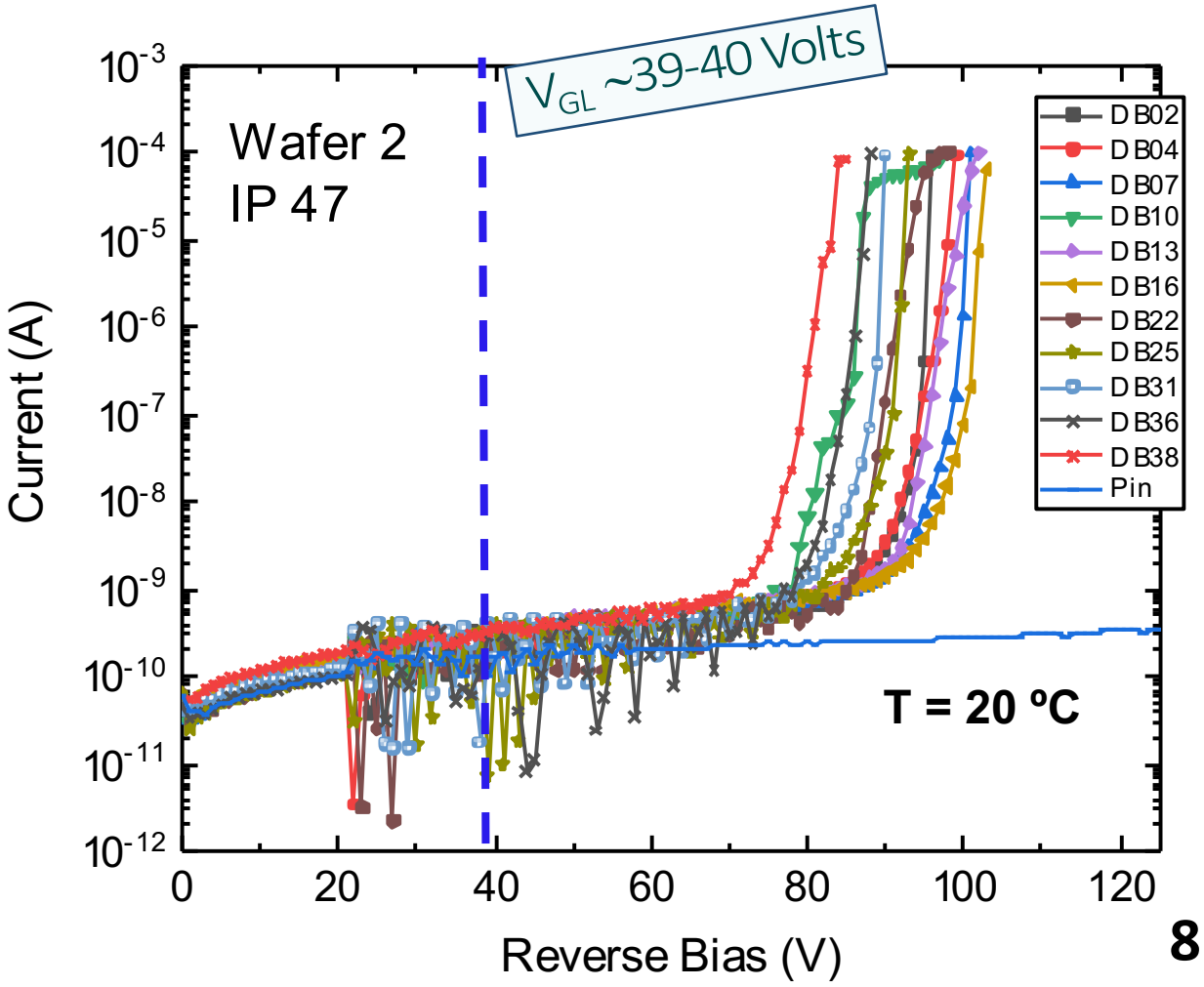




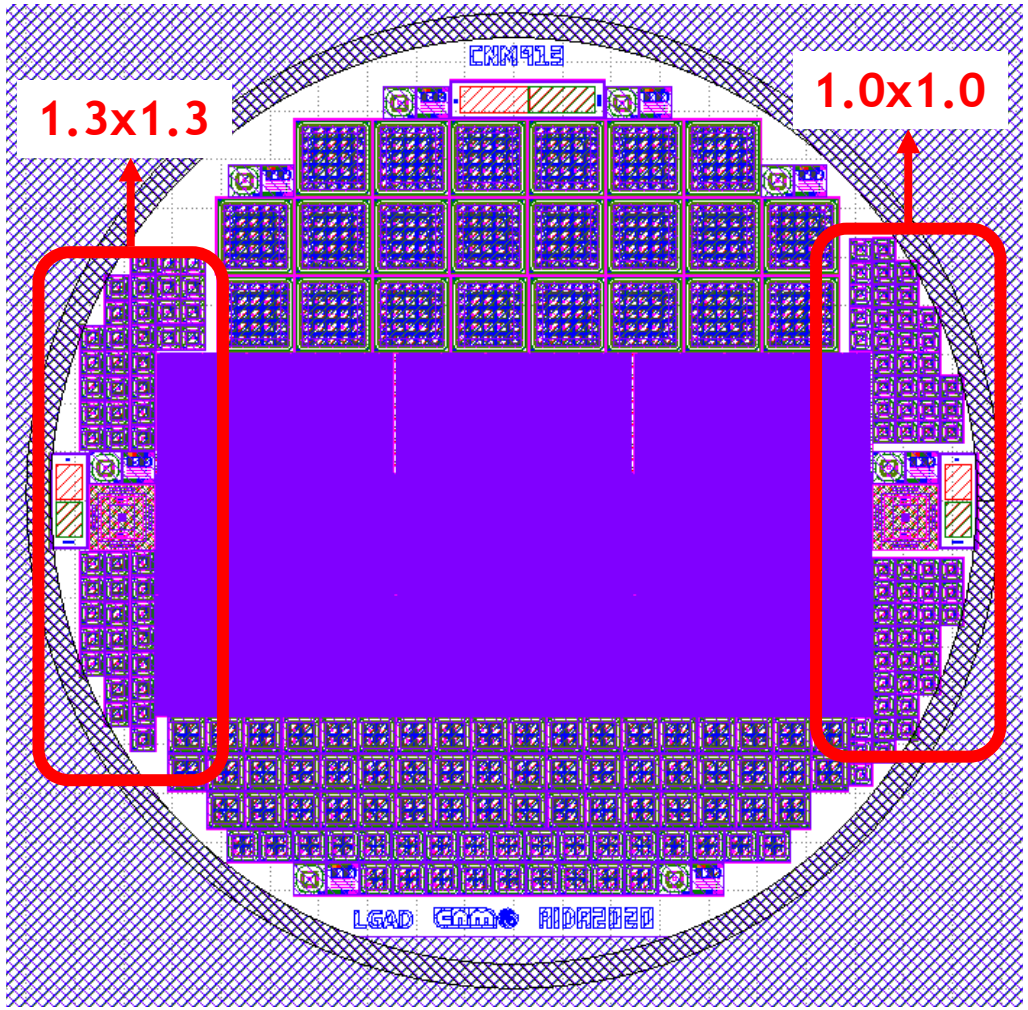
Run 12916: LGAD AIDA 2020 v2 Current-Voltage Measurements

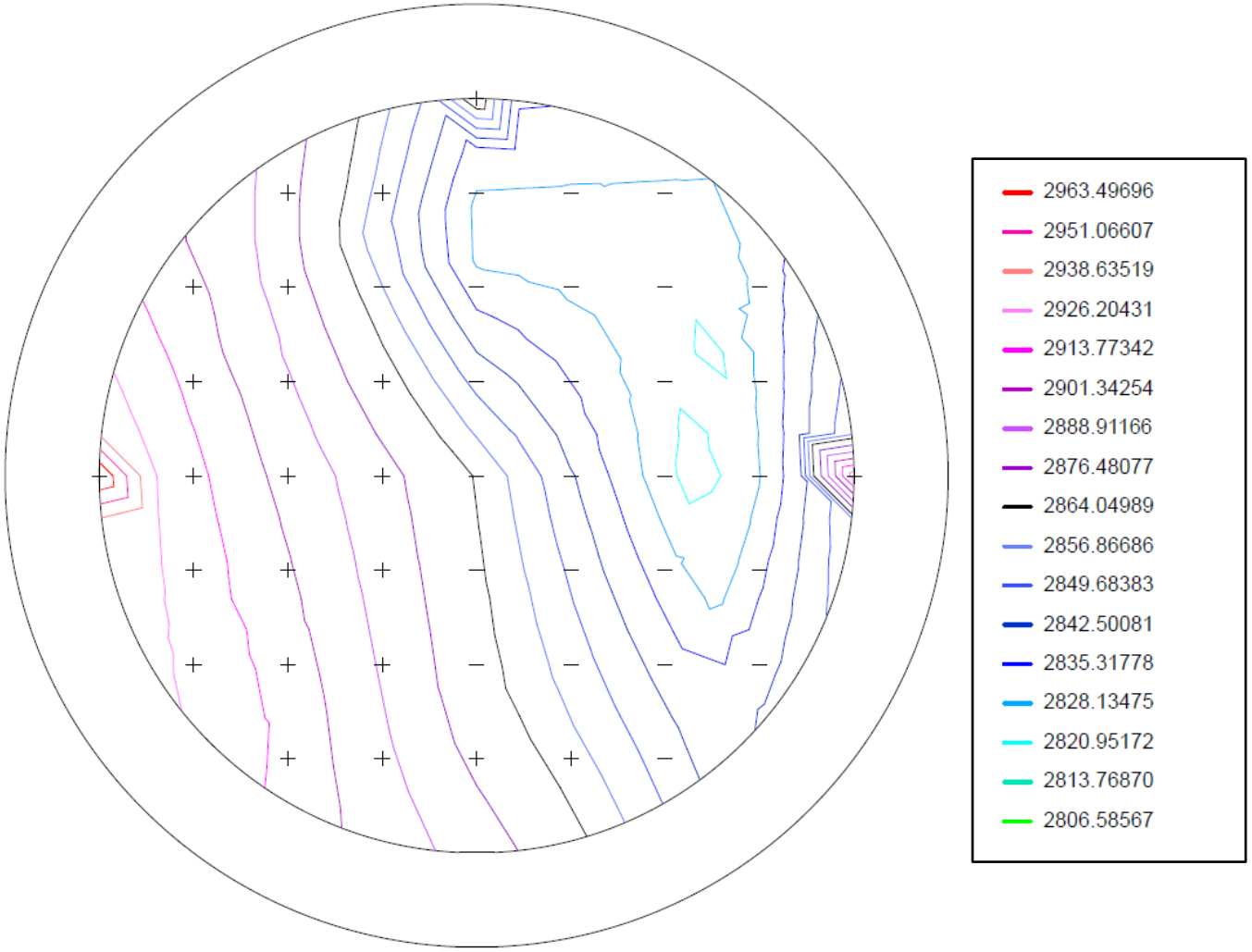
Wafer 2 Single Diode 1.3x1.3 mm² IP47





Run 12916: LGAD AIDA 2020 v2 Sheet Resistance Measurement





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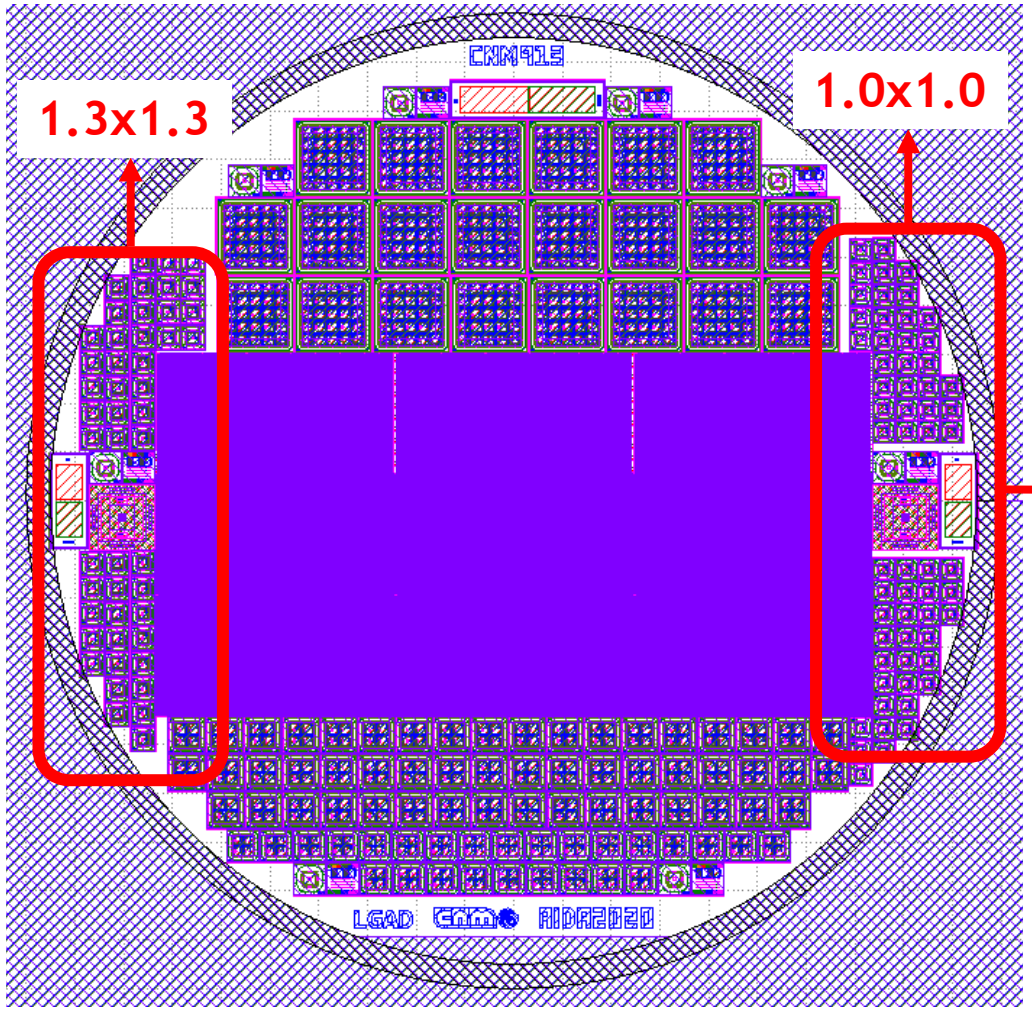
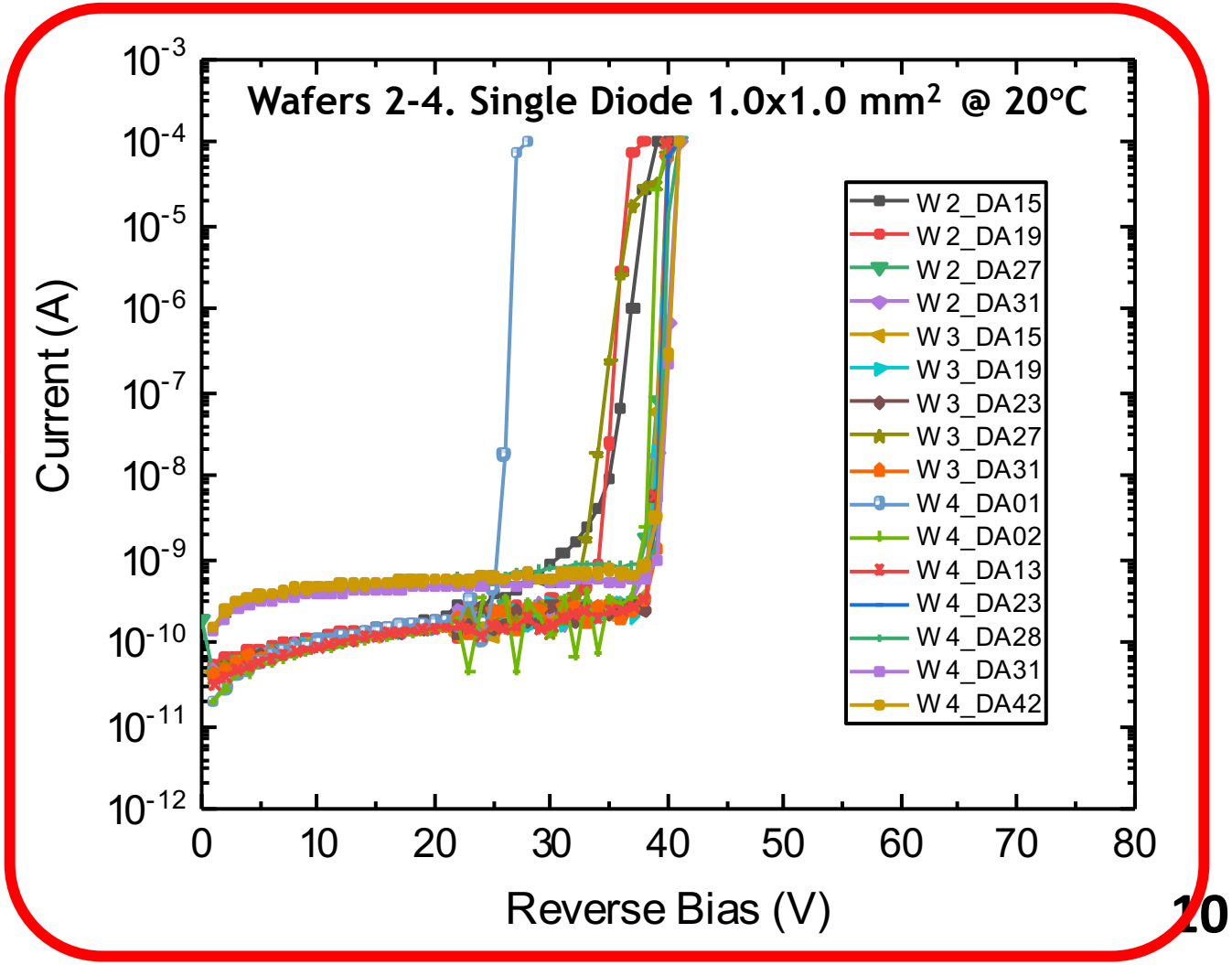


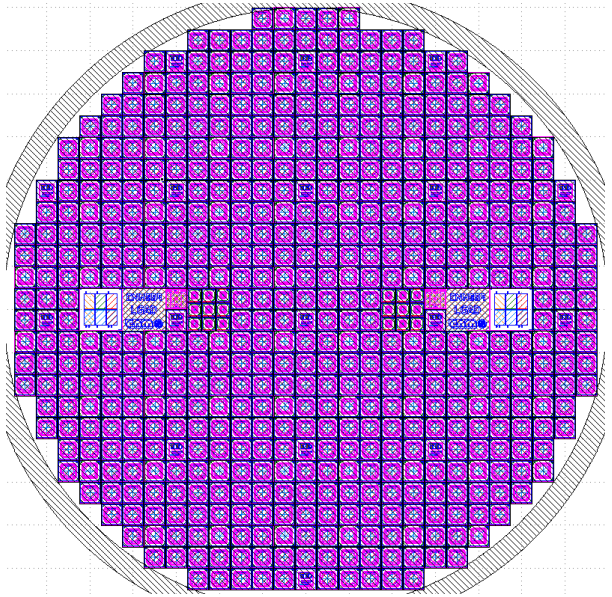


Run 12916: LGAD AIDA 2020 v2 Conclusions and Future Work

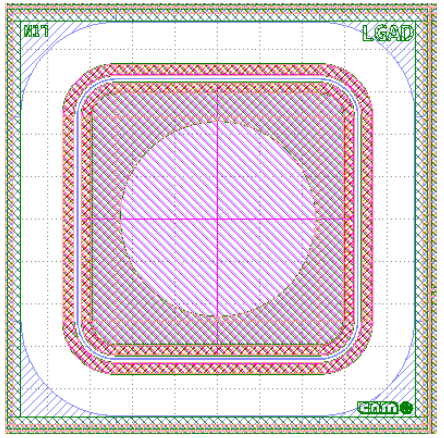
- LGAD AIDA2020v2 electrically characterized on wafer.
- IVs show low leakage current and low breakdown voltage at -20 ºC.
- High uniformity on the gain layer in all the wafers.
- Dicing process completed for 1.3x1.3 mm^2 structures:
  - CMS-like single pads (1.3x1.3 mm^2) available with three Inter-path geometries.
  - To be distributed for irradiation tolerance assessment campaign.
  - Old-design Large sensors and multi-pad 2x2 and 5x5 geometries are also available.

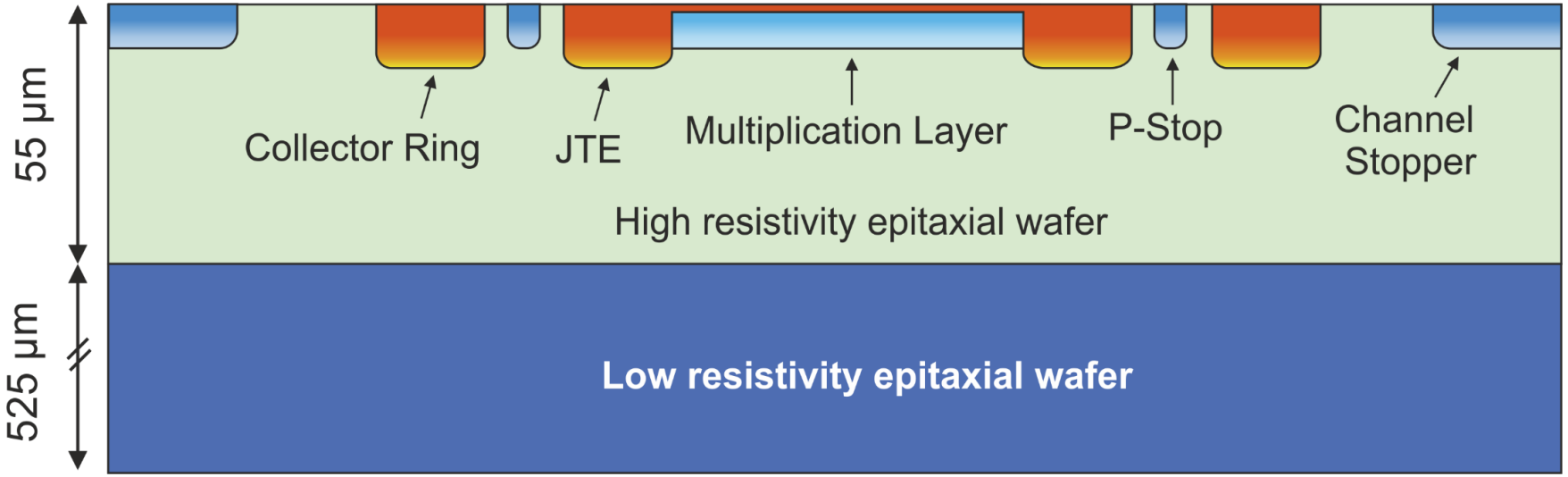
Run 13002 (6LG3): 6-inch LGAD in Epitaxial Wafers

- **4 wafers (3 LGAD + 1 PiN).**
- 6-inch 55/525 µm **epitaxial** wafers.
  - Handle wafer resistivity = 0.001-1 Ohm-cm
  - Substrate resistivity > 200 Ohm-cm
- Same mask as Run 11486. 6LG1 (50 µm, SOI wafers)



Pad diodes





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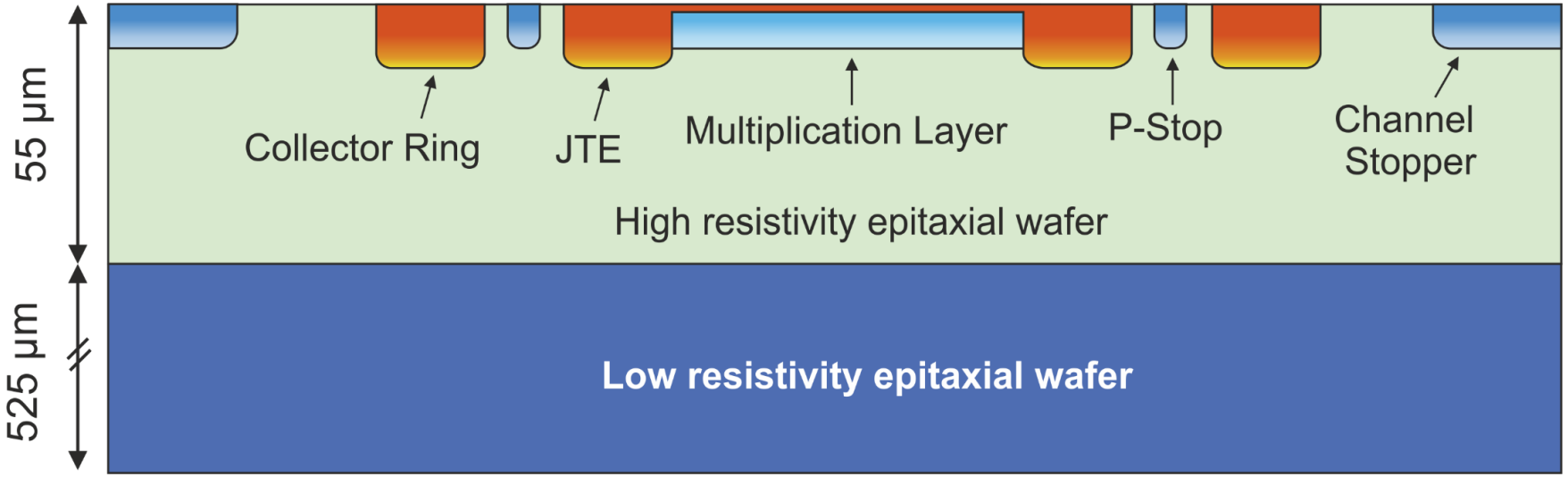
Wafer	Dose (at/cm^2)	Energy (keV)
1	-	-
2	Medium	Medium
3	Med-High	Medium
4	High	Medium



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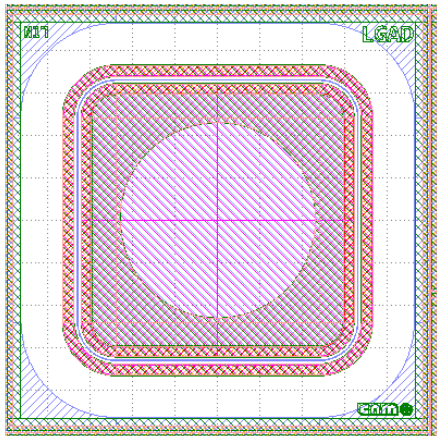
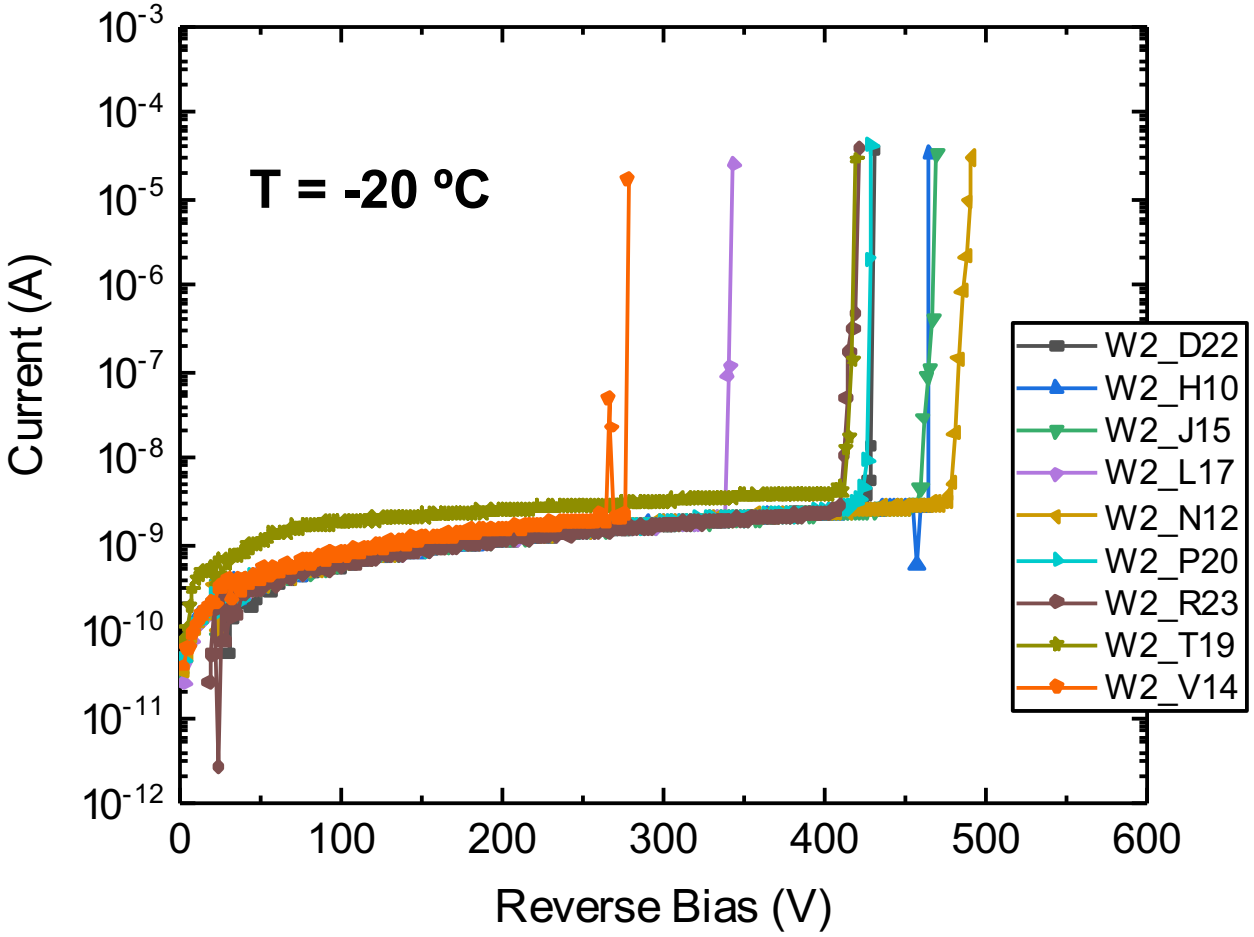
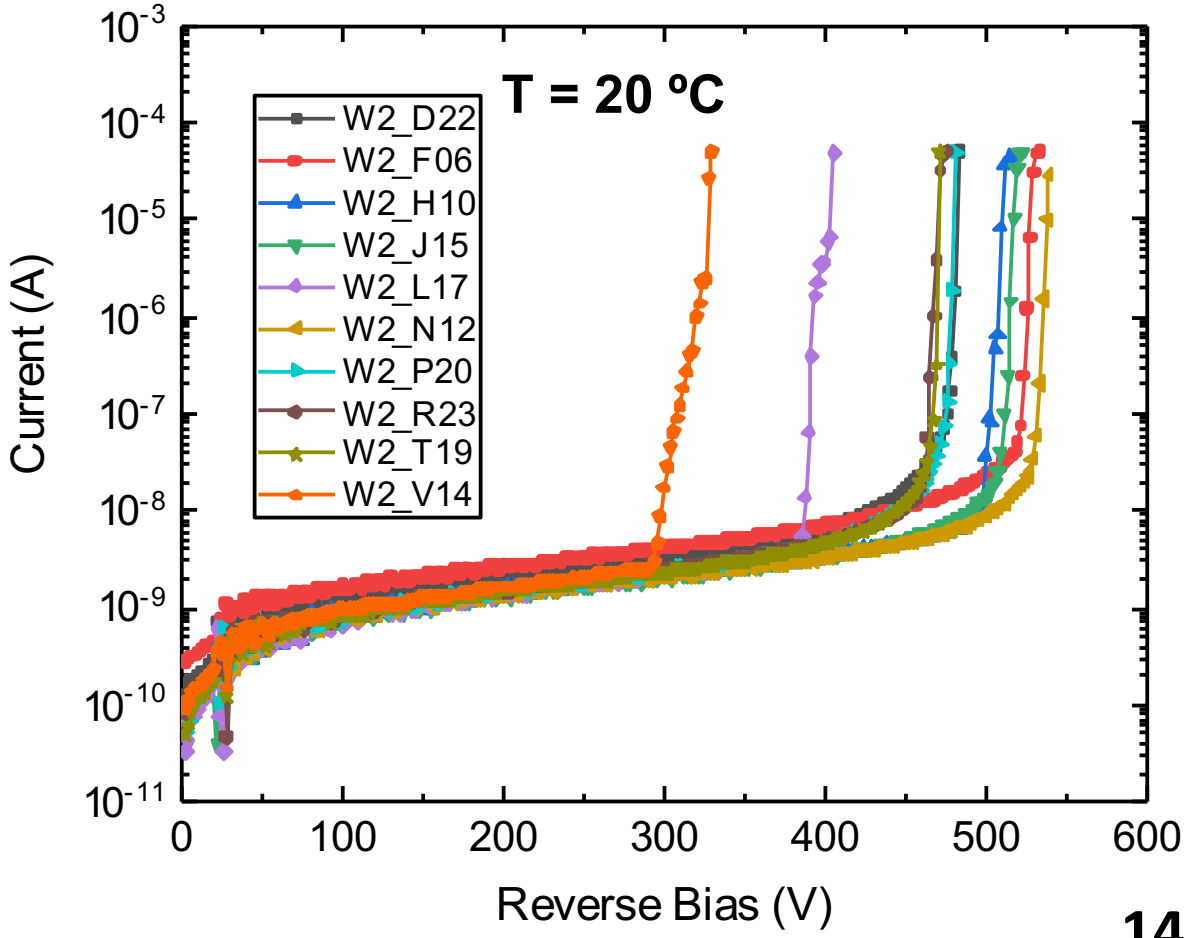


Run 13002 (6LG3): I-V Measurements on Wafer

Wafer 2 Single Diode 3.3x3.3 mm²





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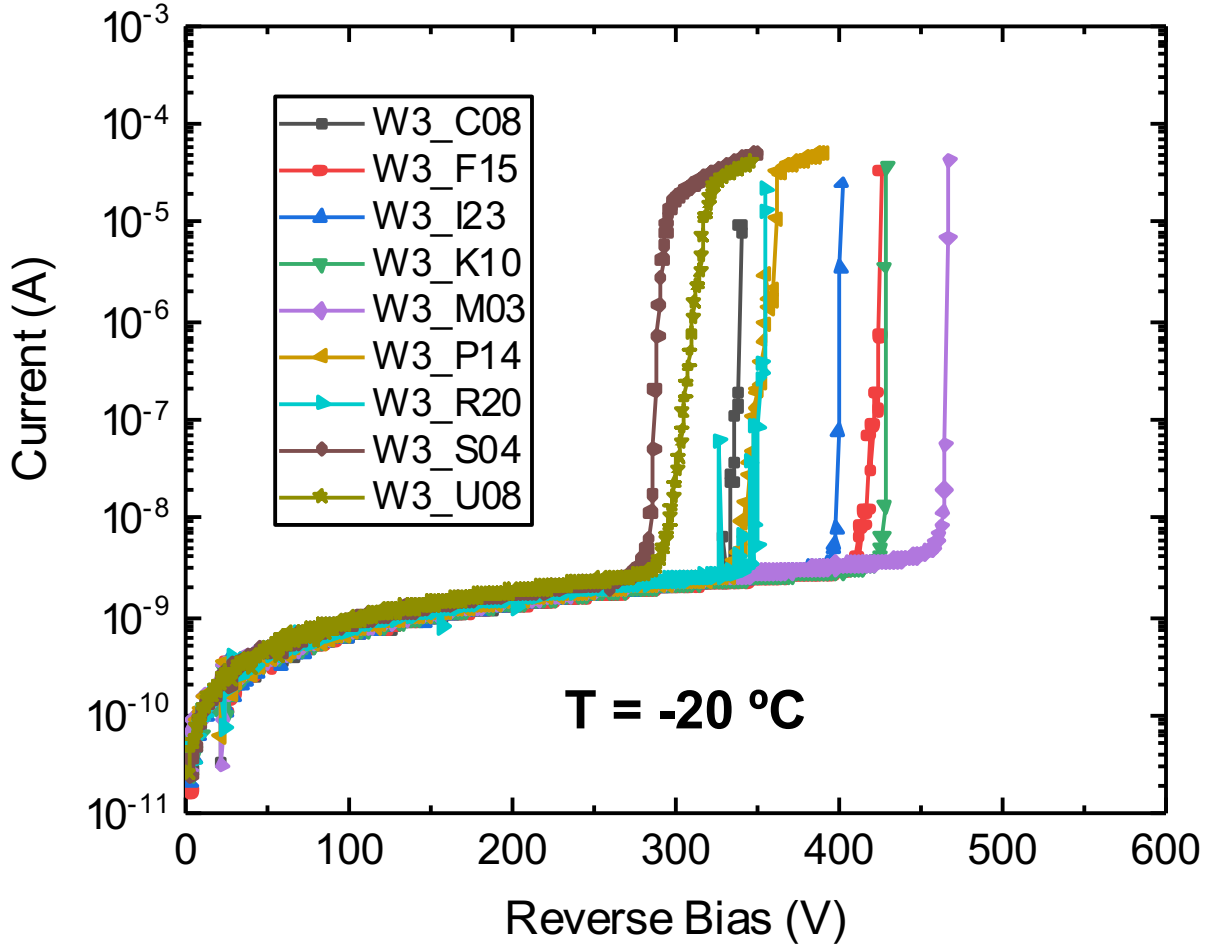

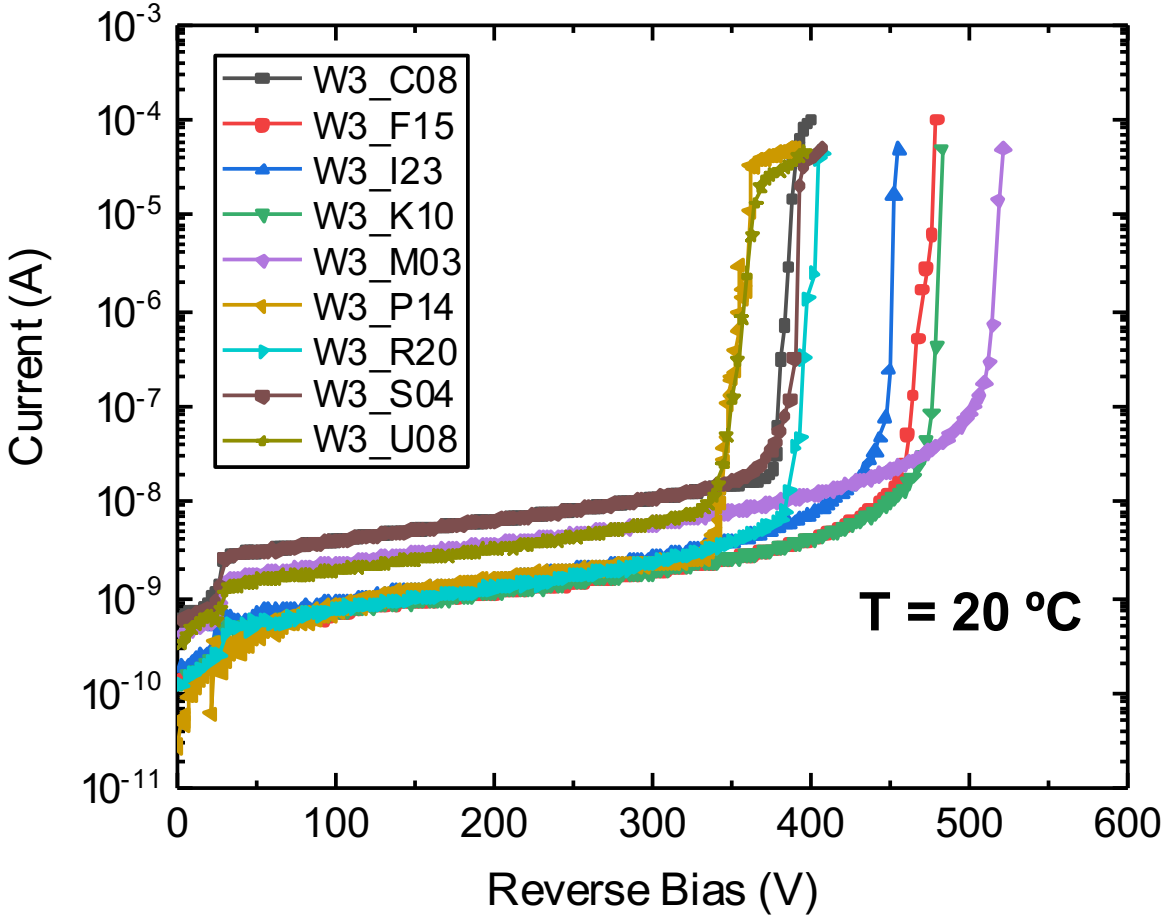

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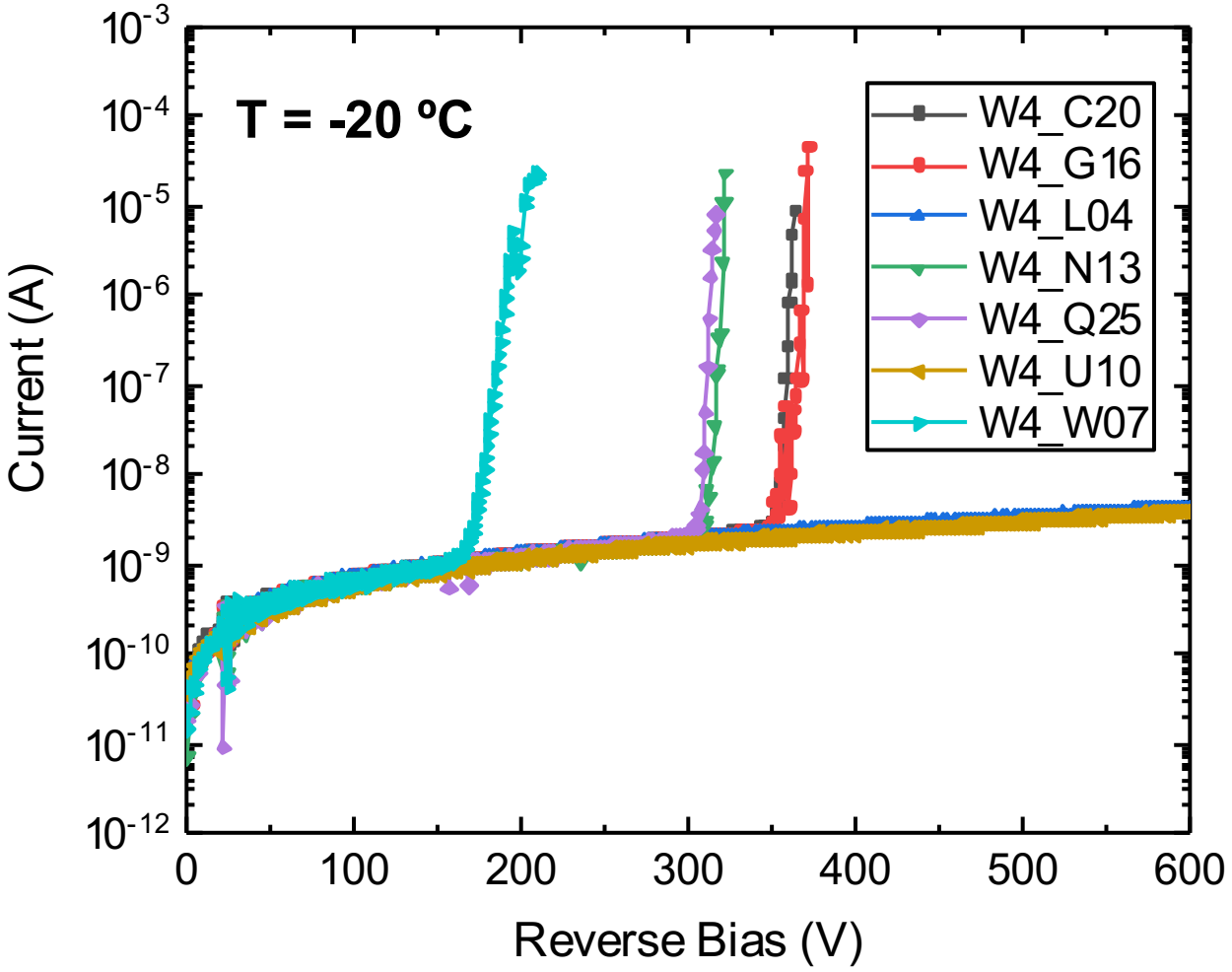
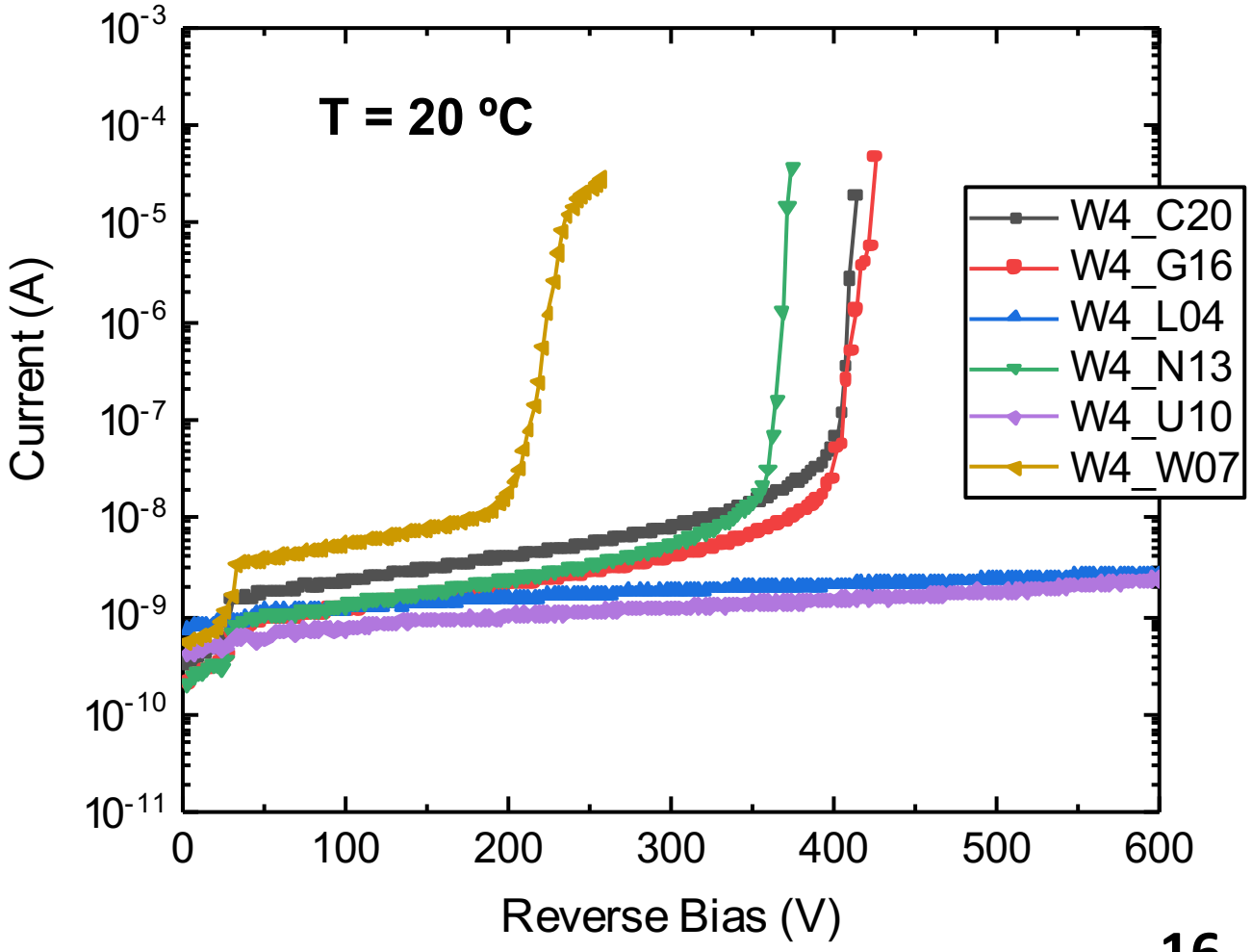
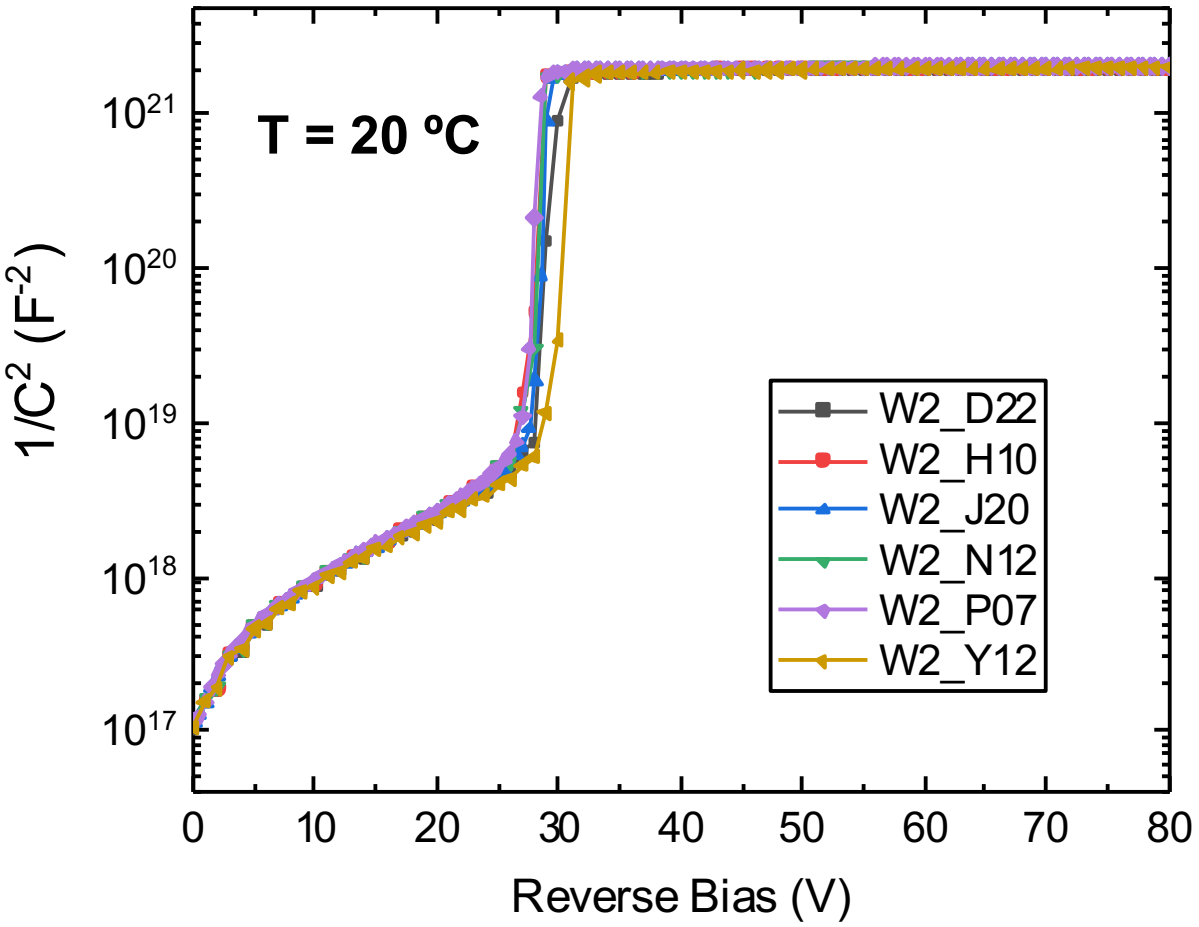
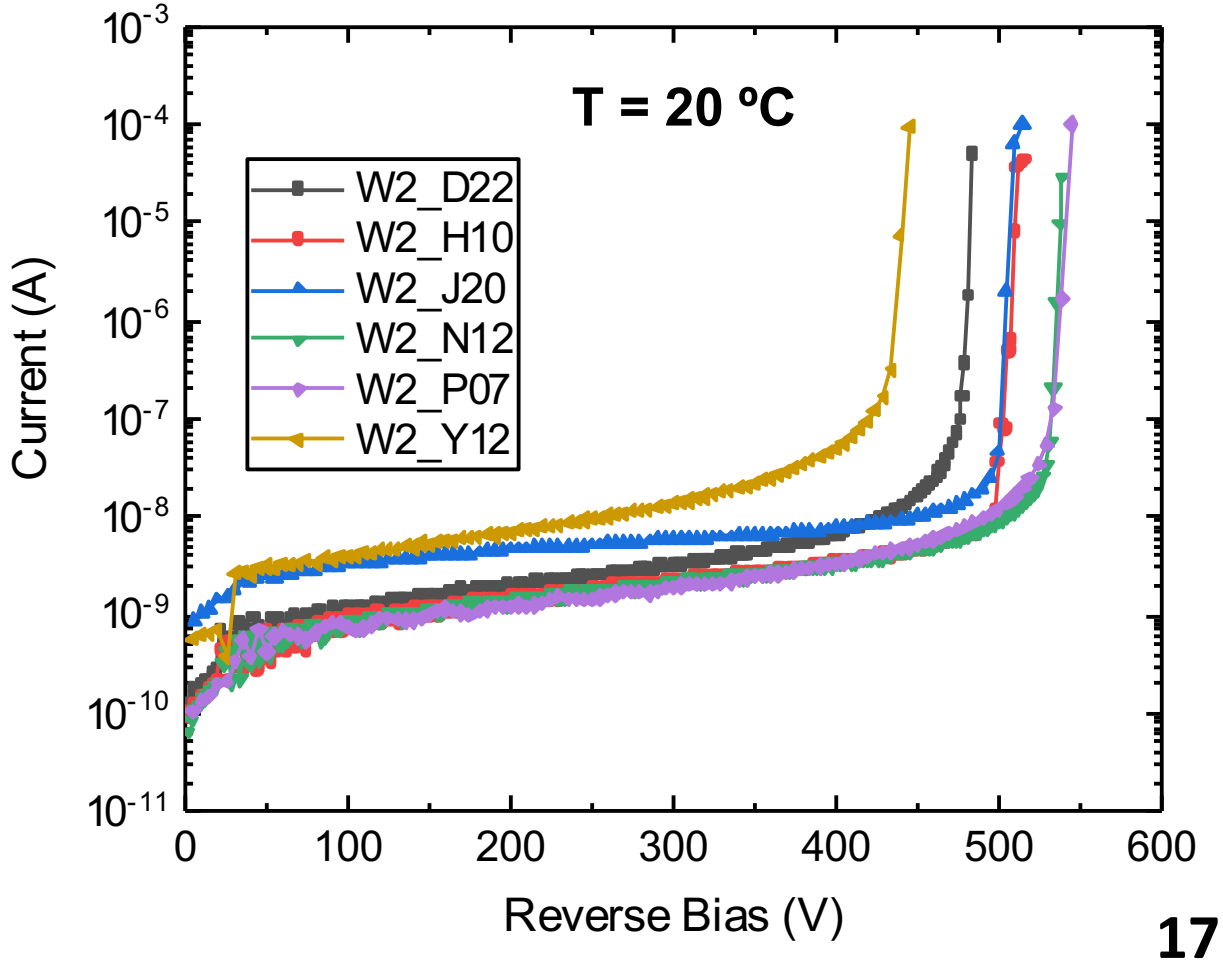




Run 13002 (6LG3): C-V Measurements on Wafer

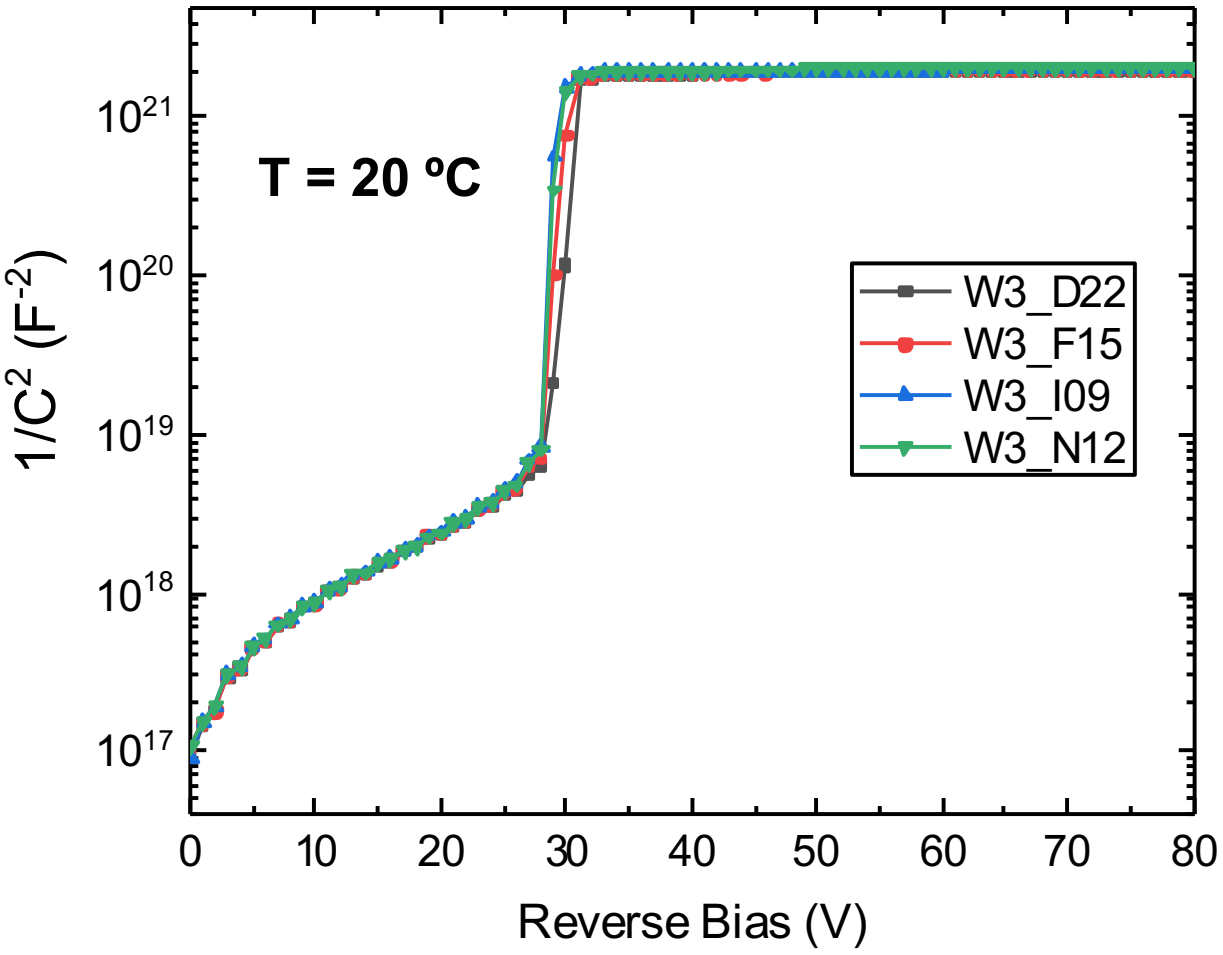
Wafer 2 Single Diode 3.3x3.3 mm²

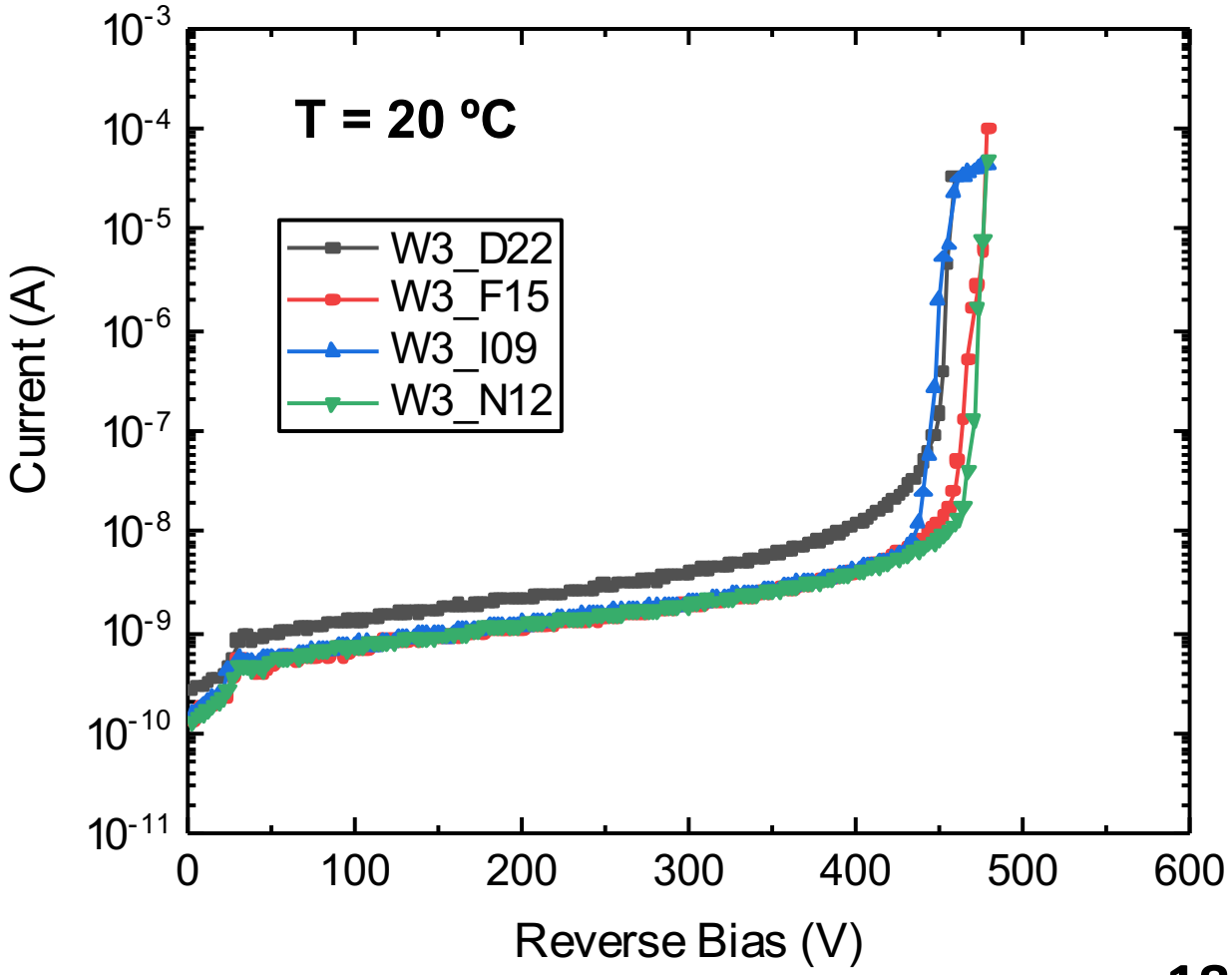




Run 13002 (6LG3): C-V Measurements on Wafer

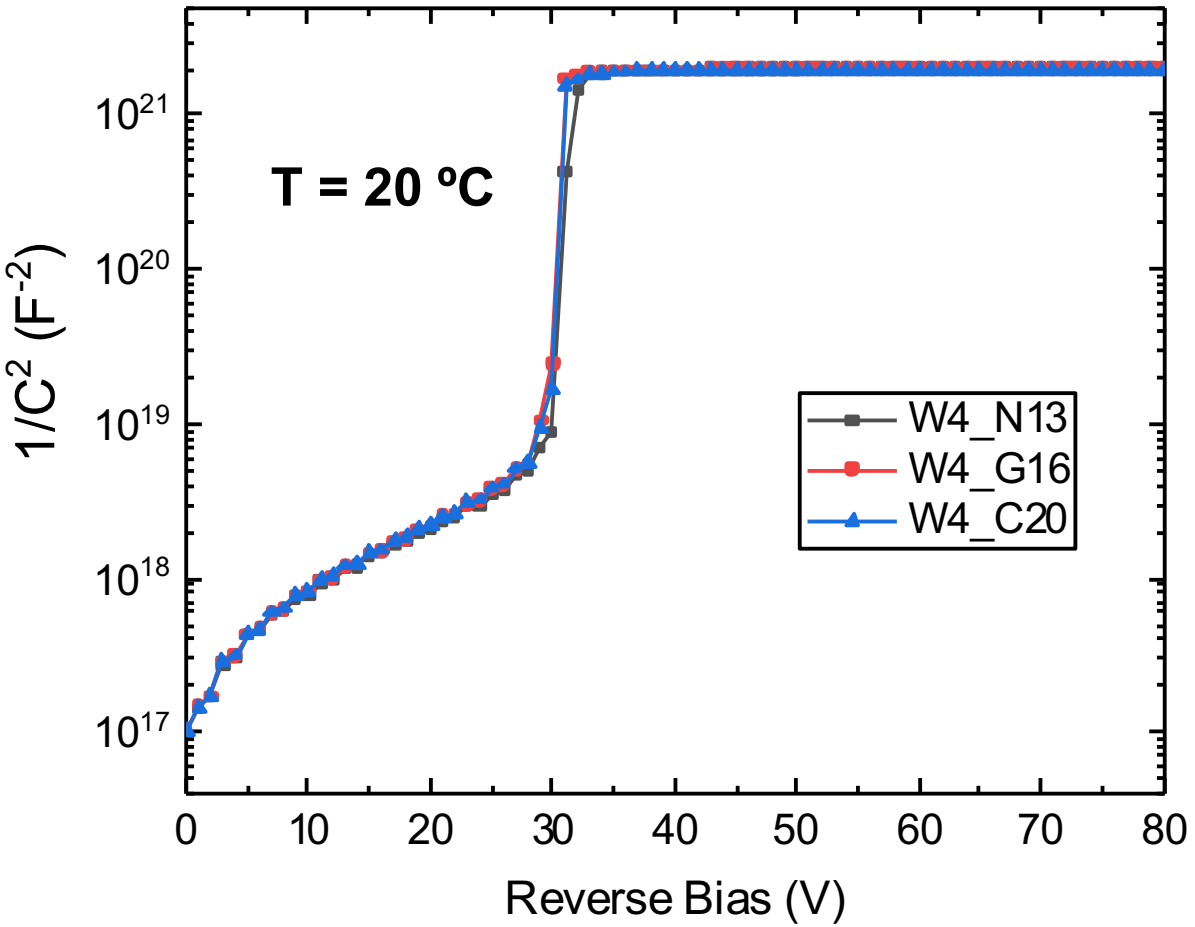
Wafer 3 Single Diode 3.3x3.3 mm²

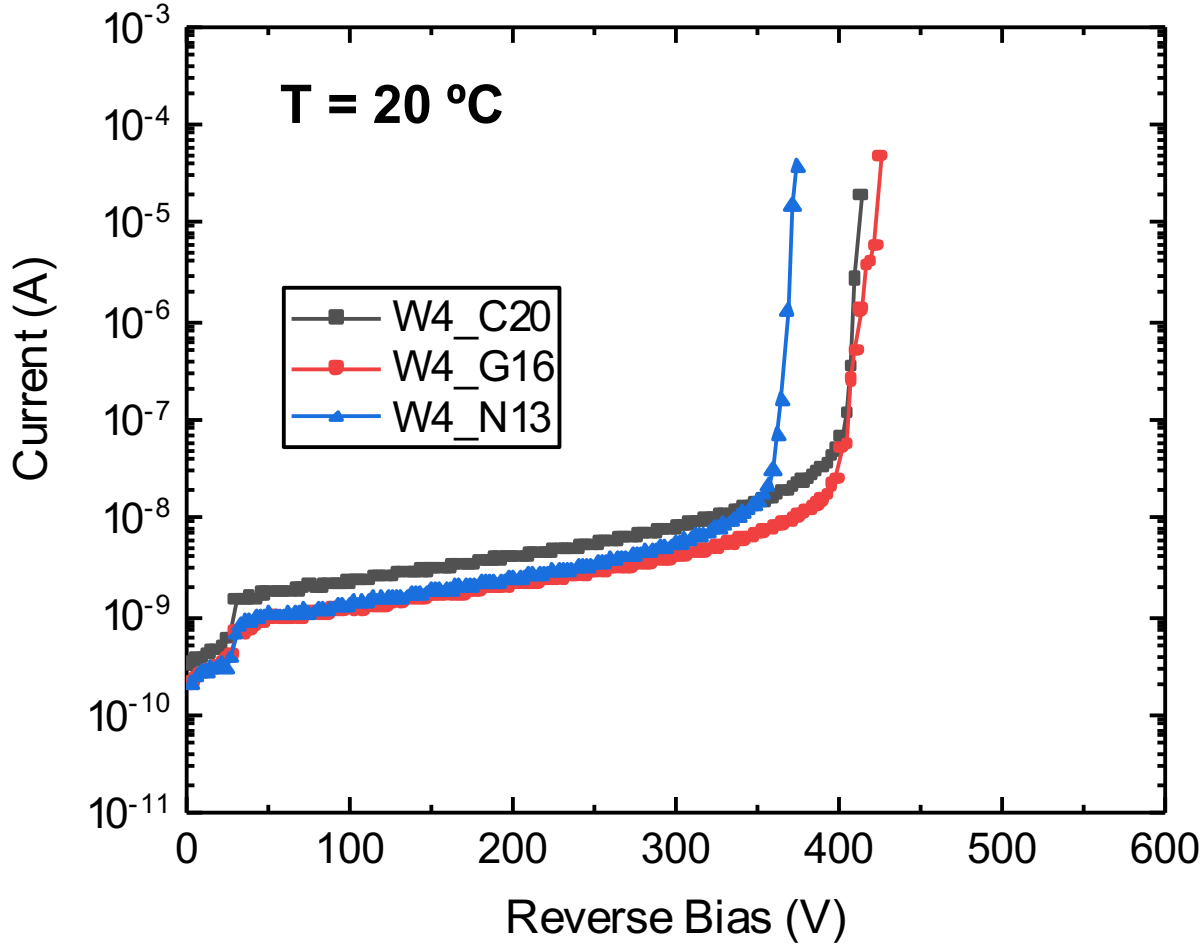




Run 13002 (6LG3): C-V Measurements on Wafer

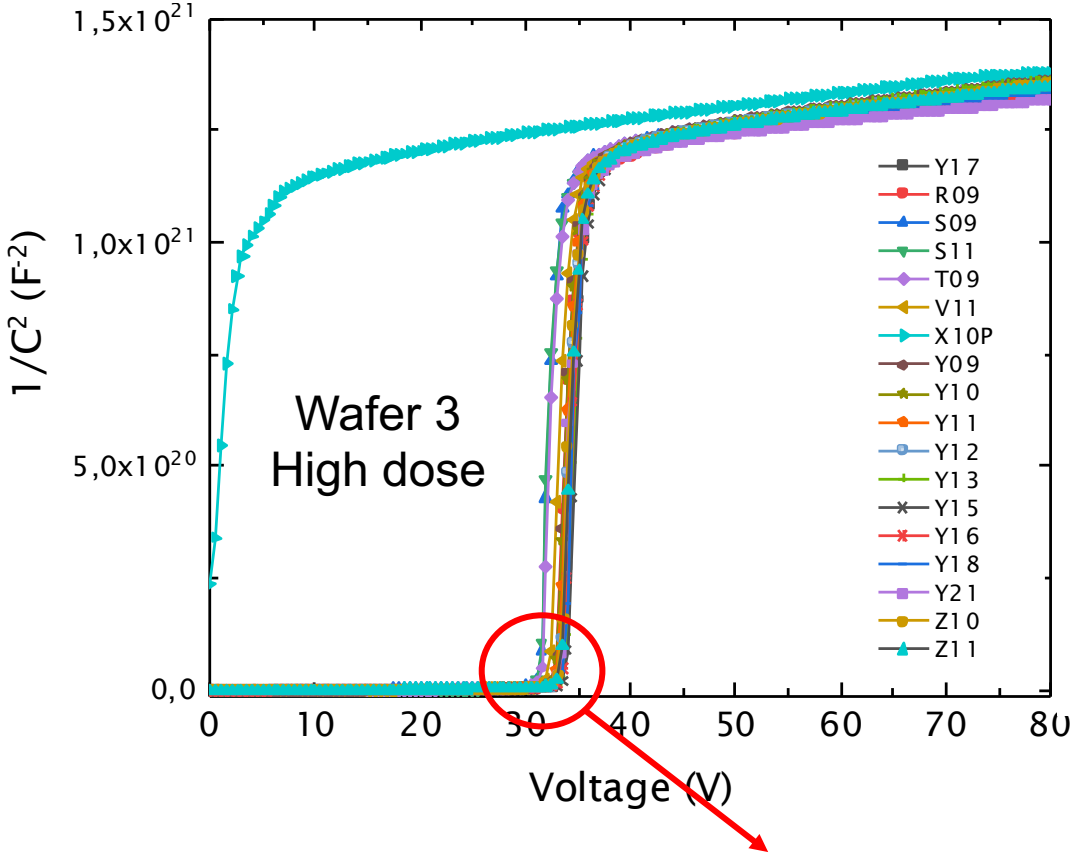
Wafer 4 Single Diode 3.3x3.3 mm²

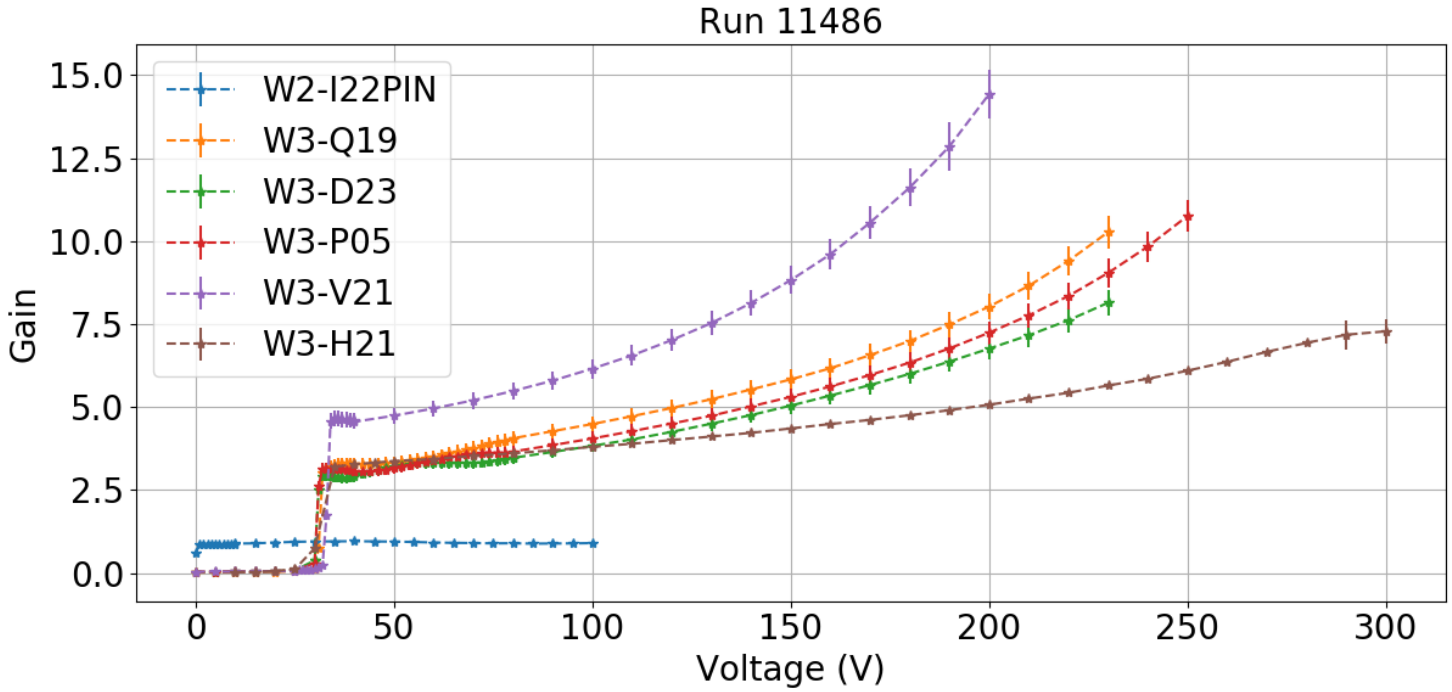




Run 13002 (6LG3) vs Run 11486 (6LG1): CV's and Gain

C-V Measurements Run 11486



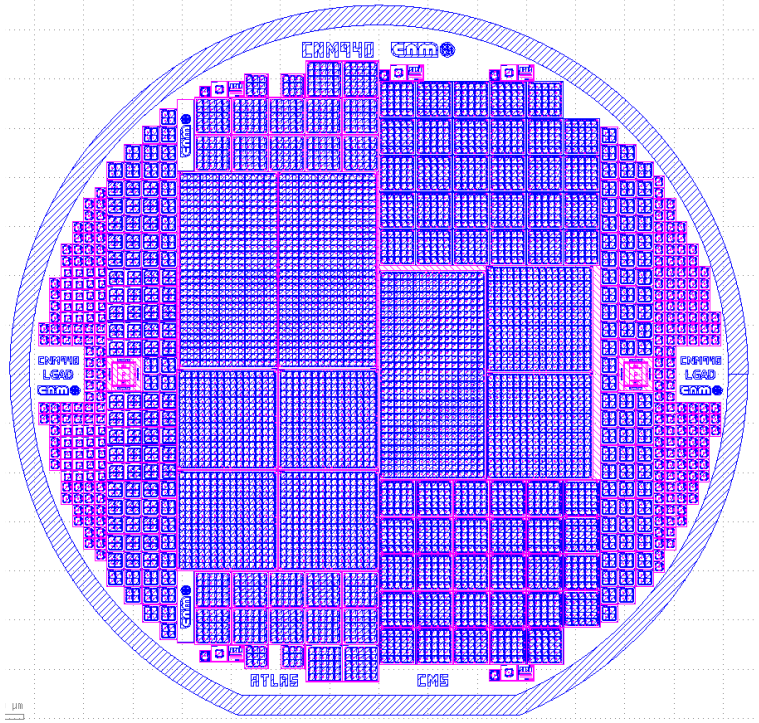


Similar V_D as Run13002

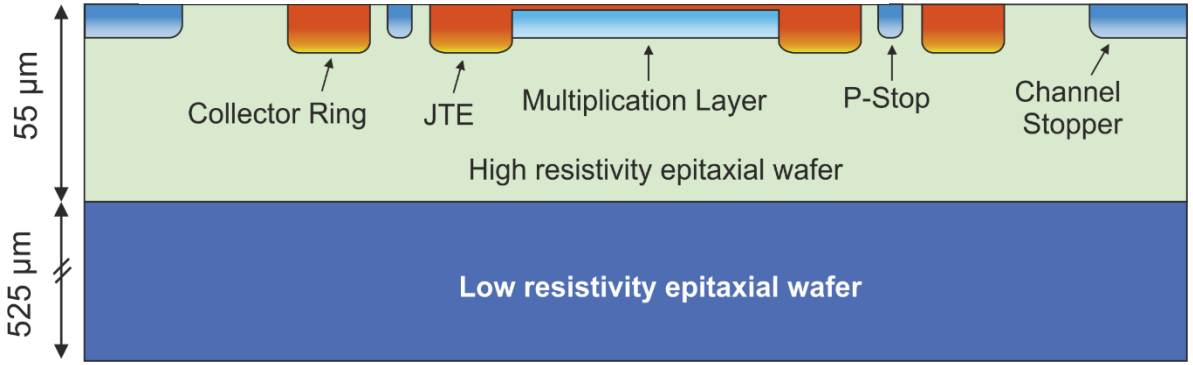
Run 13002 (6LG3): Future Steps

- IV wafer mapping of the wafers.
- Dicing process.
- TCT measurements.
- Irradiation campaigns.

Run 13840 (6LG3): 6” ATLAS-CMS Common Run

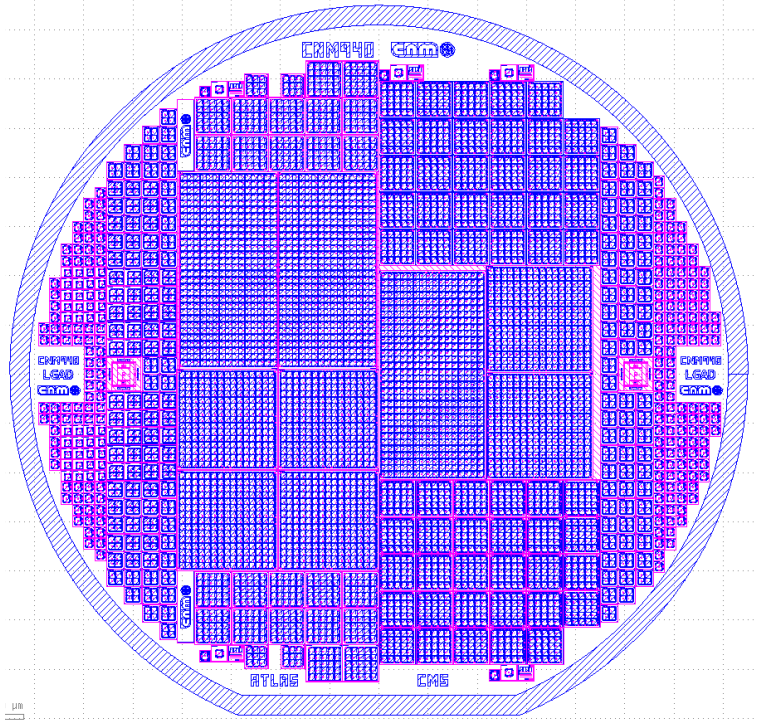


- **10 wafers (9 LGAD + 1 PiN).**
- 6-inch 55/525 µm **epitaxial** wafers.
  - Handle wafer resistivity = 0.001-1 Ohm-cm
  - Substrate resistivity > 200 Ohm-cm
- Same technological process as Run 13002. 6LG3
- 39/97 steps done (JTE)
- Waiting for New Diffusion Furnace (March 2021)
- Higher diffusion processes quality and uniformity
  - Higher Vbr and Gain uniformity

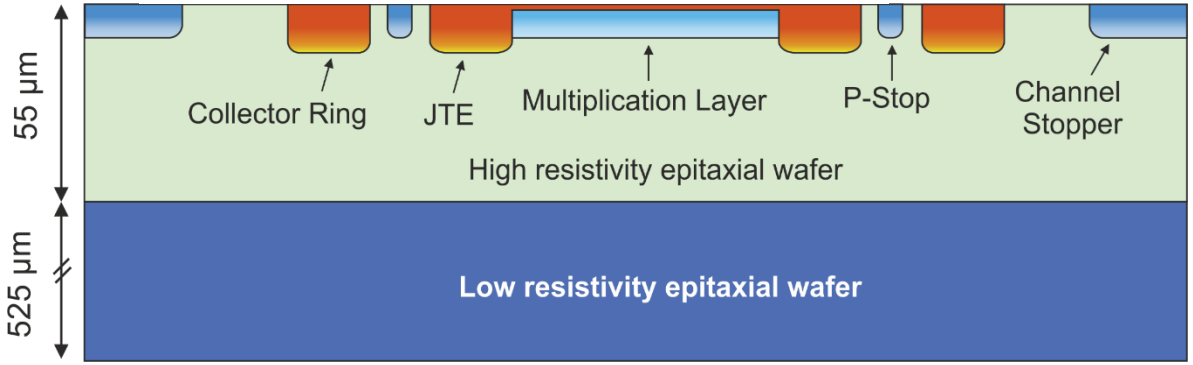


Wafer	Dose (at/cm^2)	Energy (keV)
1	-	-
2,5,8	Medium	Medium
3,6,9	Med-High	Medium
4,7,10	High	Medium

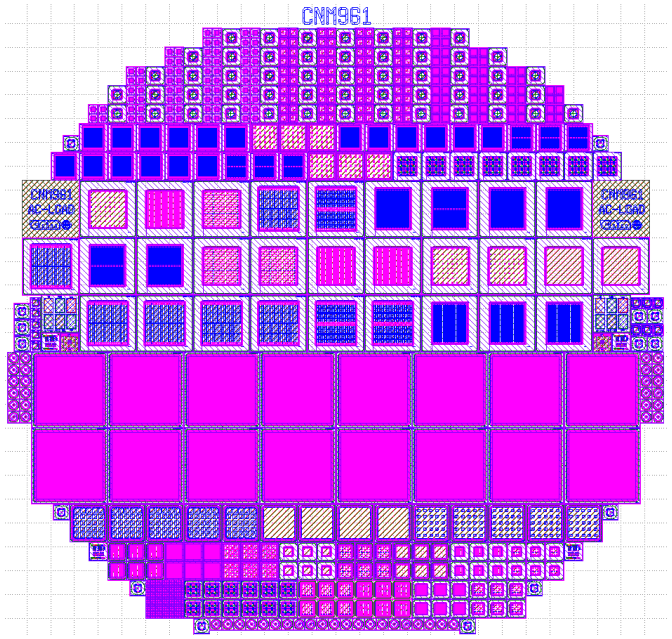
Run 13840 (6LG3): 6” ATLAS-CMS Common Run



- Run 6LG2 (Si-Si wafers):
  - 6-inch Si-Si 50 µm wafers
  - 6-inch 300 µm wafers
- Carbonated wafers included
- Same technological process as Run 13002. 6LG3
- Waiting for New Diffusion Furnace (March 2021)
- Higher diffusion processes quality and uniformity
  - Higher Vbr and Gain uniformity



Run 13911 (6ALG1): 6” AC-LGAD



Wafer	Dose (at/cm²)	Energy (keV)
15	-	-
1,4,7-9,12	Medium	Medium
2,5,10,13	Med-High	Medium
3,6,11,14	High	Medium

- **15 wafers (8+6 AC-LGAD + 1 PiN).**
- 6-inch 50/350 µm, P-type **Si-Si** wafers.
  - Handle wafer resistivity = 0.001-1 Ohm-cm
  - Substrate resistivity > 1 kOhm-cm
- 6-inch, 300 µm thick, P-type silicon wafers.
  - Substrate resistivity 6-12 kOhm-cm
- Technological process based on Run 11486. 6LG1 (50 µm, SOI wafers)
- 23/116 steps done (P-stop)
- Waiting for New Diffusion Furnace (March 2021)
- Higher diffusion processes quality and uniformity
  - Higher Vbr and Gain uniformity

Optimized with TCAD Simulations + PSPICE


Thank you for
your attention!