Radiation tolerant small-pixel passive CMOS sensors with RD53A readout

RD50 Meeting, 20.11.2020

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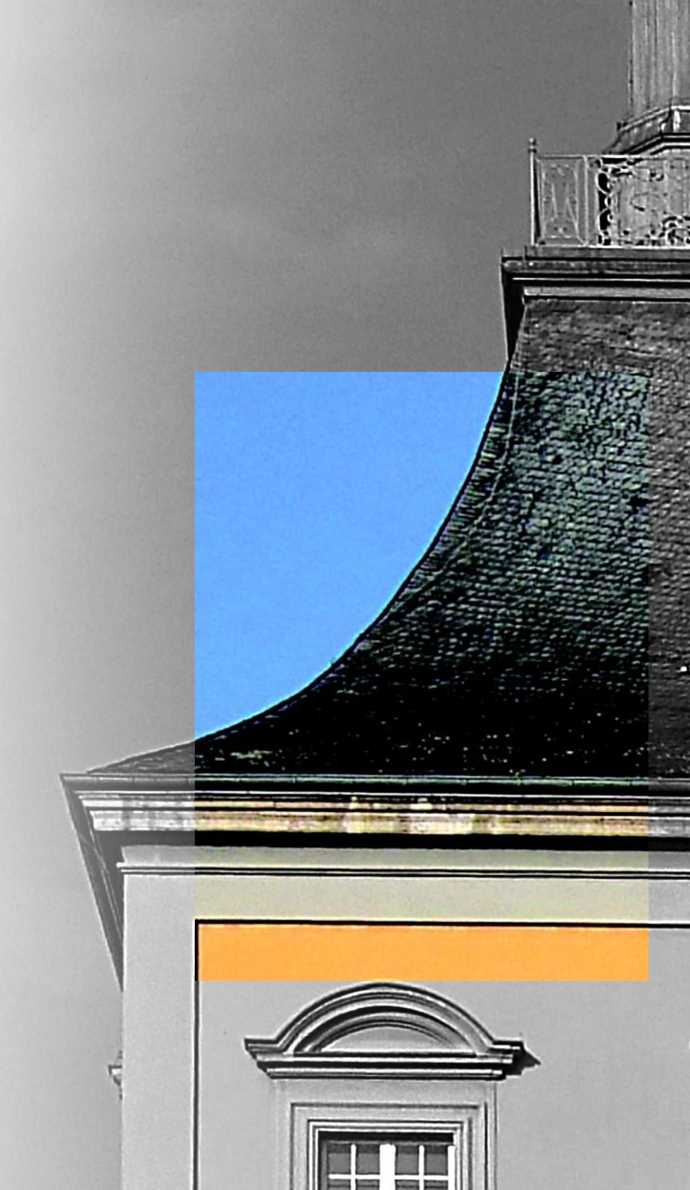
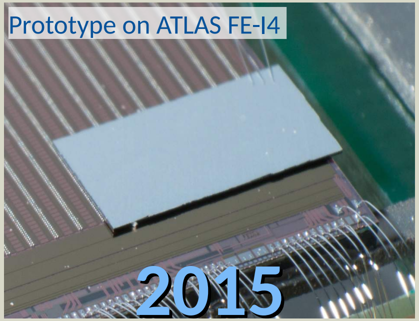


PASSIVE CMOS SENSORS USING LFOUNDRY PROCESS

Large pixel prototype

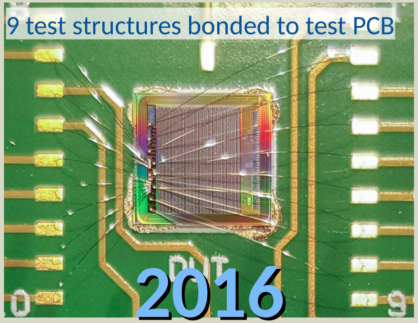
- 50 x 250 um² pixels, ATLAS IBL planar geometry
- Performance comparable to ATLAS IBL sensors after irradiation > 1 x 10^{15} neq/cm²
- Investigation of AC-coupling schema, pixel biasing schemes (bias dot vs. resistor biasing)



Prototype on ATLAS FE-I4

Test structures

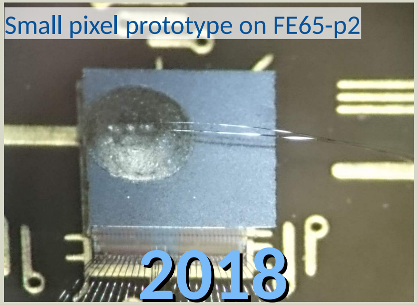
- Many structures produced (> 15)
- Varying designs: guard rings, pixel isolation, implantation geometries
- Investigations of break down with TID (2 master theses)
  → Identified enhanced guard ring structure
- Investigation of sensor capacitances (2 bachelor theses)



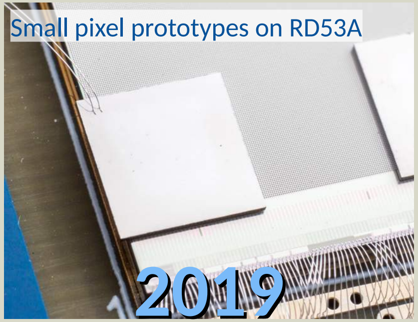
9 test structures bonded to test PCB

Small pixel prototype

- 50 x 50 um² pixels, ATLAS ITk pixel geometry



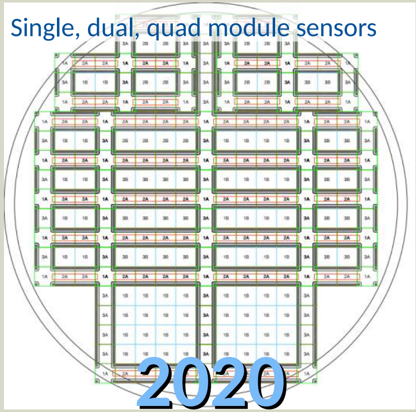
Small pixel prototype on FE65-p2



Small pixel prototypes on RD53A

Sensor for ATLAS ITk modules

- 50 x 50 um² pixels, 25 x 100 um² pixels
- Full-size ATLAS ITk pixel modules
- RD53A and RD53B compatible



Single, dual, quad module sensors

From D.-L. Pohl Trento 2020

Byproducts of DMAPS efforts

This talk

Dedicated design

SMALL PIXEL PROTOTYPE

- Passive CMOS pixel sensor in 150 nm LFoundry technology
- Resistivity of bulk material: 5 – 7 kΩcm (p-type CZ wafer)
- 100 um thick, etching, backside implantation + metallization
- 50 um x 50 um pixels in 64 x 64 matrix
- Different fill-factors realized to maximize efficiency / sensor capacitance:
  - Implant widths of 30 um (std. design), 25 um, 20 um, 15 um
- DC coupled pixels, no biasing structures
- Bump-bonded to RD53A R/O chip
- Measured at different irradiation steps
  - 5×10^{15} n_{eq}/cm^2 , **1×10^{16} n_{eq}/cm^2**

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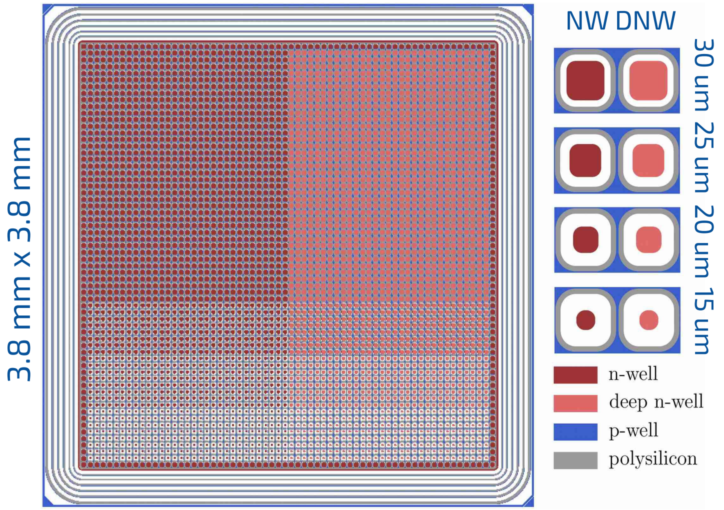
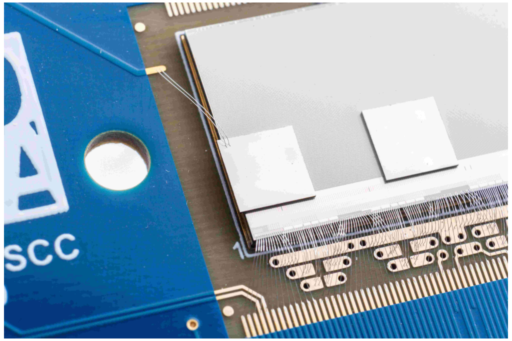
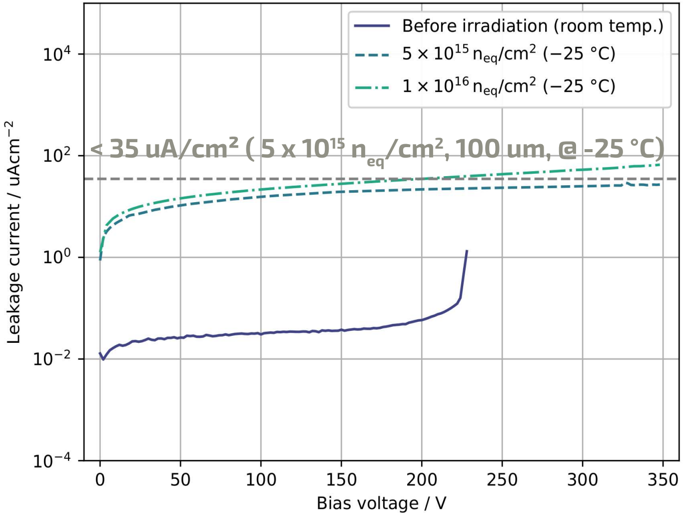
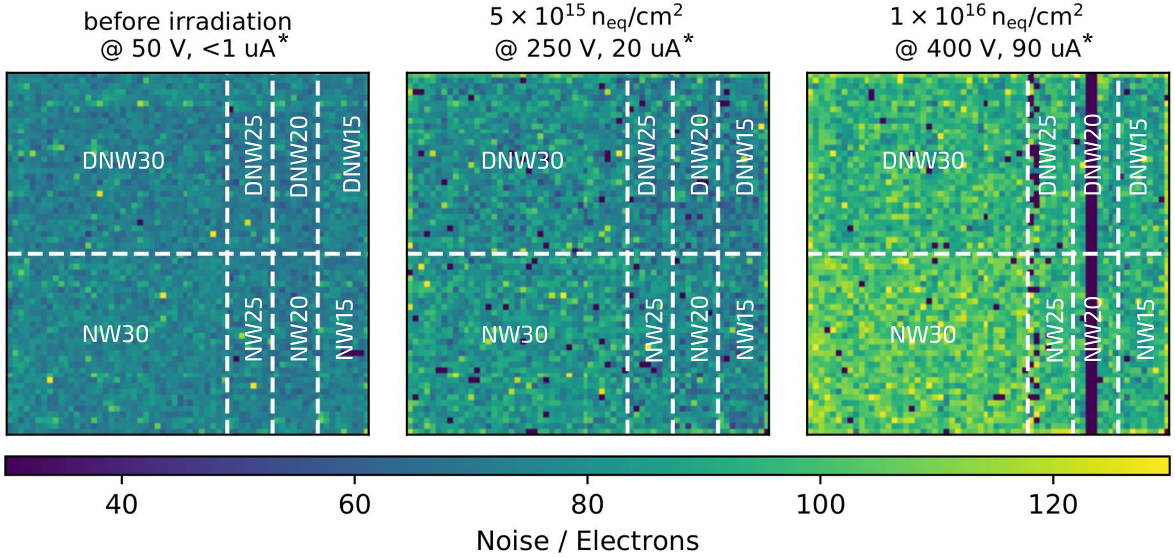
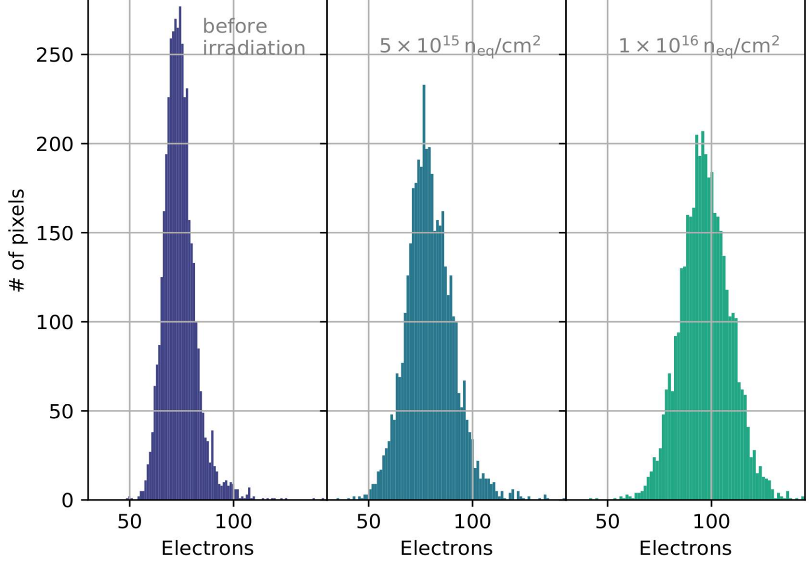






NOISE PERFORMANCE





- Average ENC (before irradiation): ~ 75 e → comparable to other planar sensors

* Measured at -17 °C

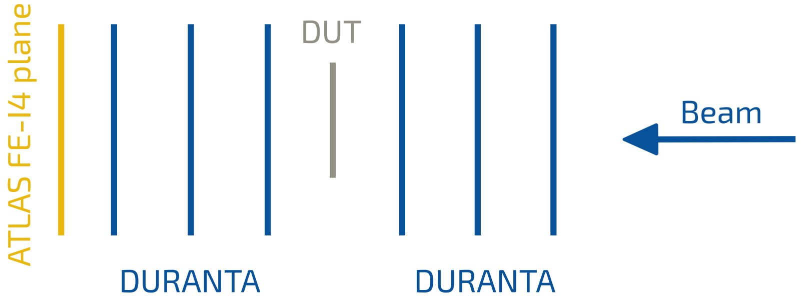
- No difference across different pixel designs in terms of noise

  → Although, pixel cap. is different (C_{NW30} ~25 fF) [H. Krüger, E. Kimmerle, Pixel Capacitance Measurement]

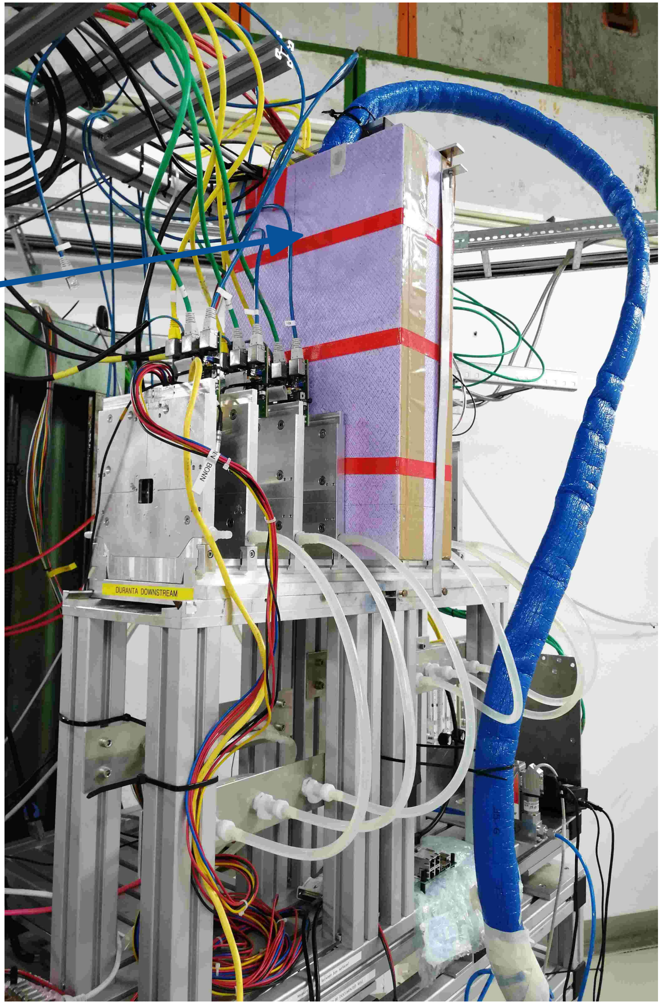
- After 1 x 10^{16} n_{eq}/cm^2: ENC increased to ~100 e (but also higher leakage current + noise of FE included)

TESTBEAM SETUP

- Testbeam done at DESY
  - Perpendicular, 5 GeV electron beam
  - Trigger rate: 3 - 5 kHz
- DUT measured in cooling box:
  - Controllable, stable temperature (ΔT ~ 1 °C)
  - Temperature: -15 °C (NTC on R/O chip)
- DUT read out using BDAQ53 R/O system [10.1016/j.nima.2020.164721]



Cooling box with DUT

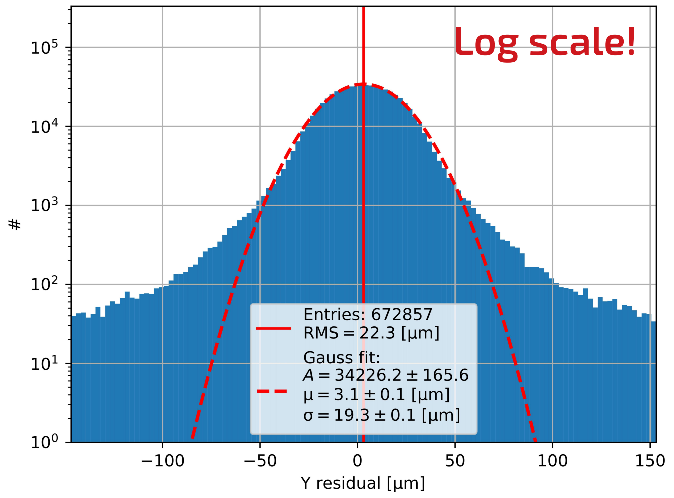


TRACK RECONSTRUCTION

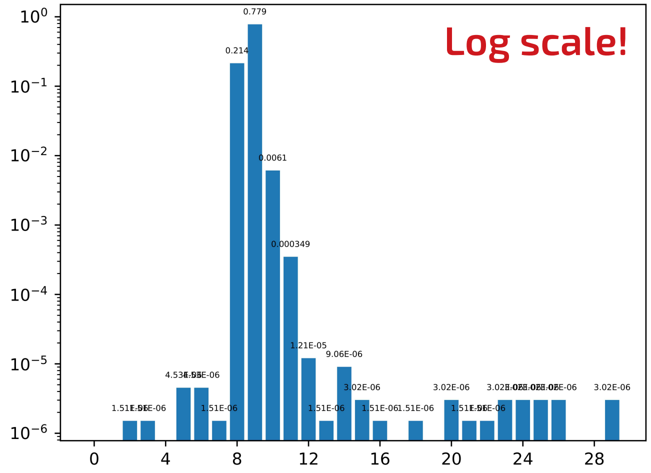
- Testbeam data reconstructed with BTA: https://github.com/SiLab-Bonn/beam_telescope_analysis
- Kalman Filter algorithm used for tracking (unbiased)
- Search radius for efficiency calculation: 200 um
- Alignment: Good
  - Small tails due to multiple scattering in cooling box
- Timing: Good
  - Almost every hit is „in-time“

→ No noise hits included in analysis!

(Unbiased) Residual distribution in y-dir. (for DUT)



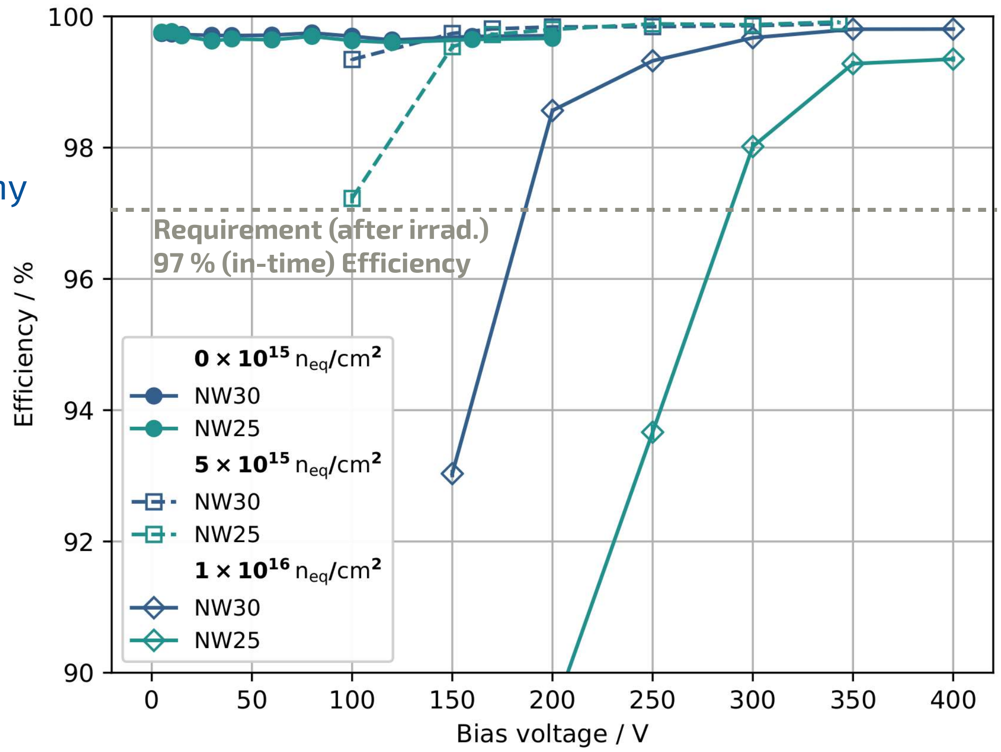
Timing distribution (rel. BCID)



EFFICIENCY MEASUREMENT

- DUT operation conditions:
  - Threshold: ~ 1000 e
  - Noise occupancy: < 10^{-6}
  - Bias voltage > 400 V not possible due to too many noisy pixels
- Before irradiation:
  - Fully efficient (> 99.5 %) at 5 V only
- After irradiation:
  - 5×10^{15} n_{eq}/cm^2: **> 99 % efficiency (@ 100V only)**
  - 1×10^{16} n_{eq}/cm^2: **> 99 % efficiency (@ 400V)**
- **Reminder: NW30 is std. design**

Hit-detection efficiency of 100 um passive CMOS sensor



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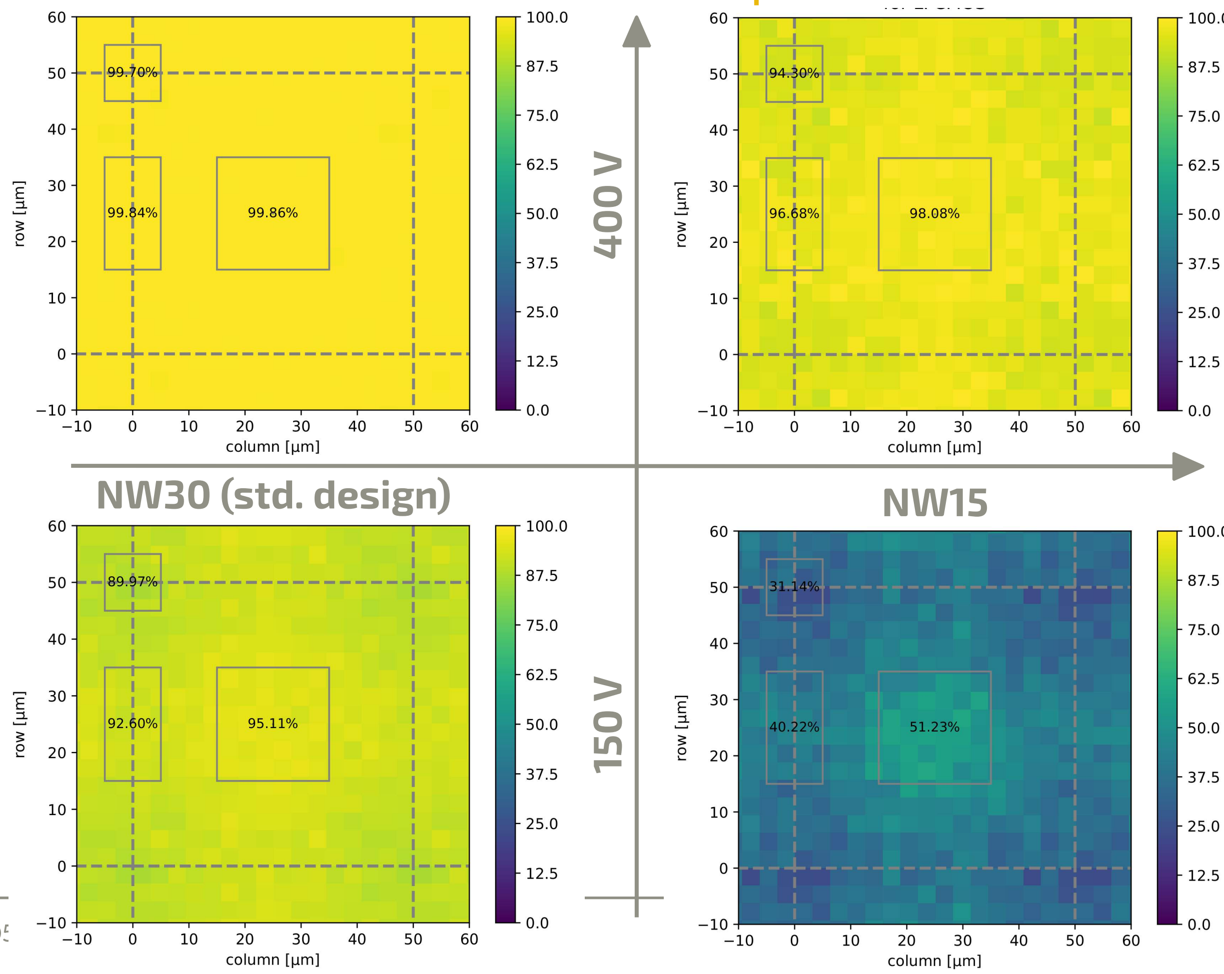
IN-PIXEL EFFICIENCY @ 1 x 10^{16} n_{eq}/cm^2

- High bias voltage + large n-implants
  - Homogeneous efficiency within pixels
- Flavors with small n-implants:
  - Efficiency loss at pixel corners (especially for low bias voltage)

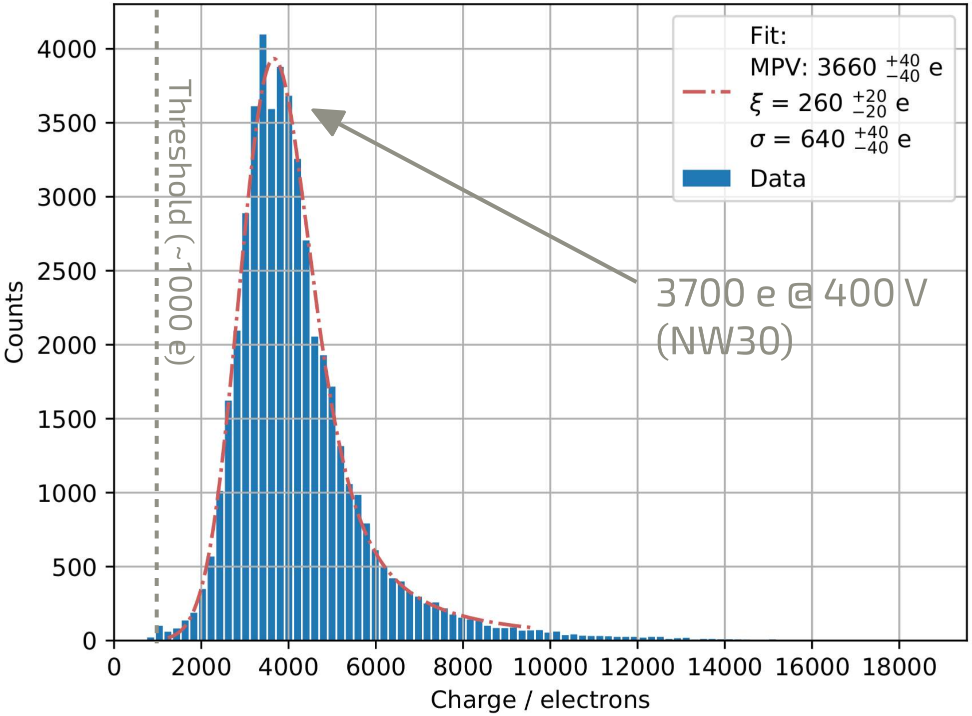
    → Due to low electric field and charge sharing



CHARGE MEASUREMENT

- Charge measurement:
  - Sampling of HitOr with external clock (640 MHz)
    → Length proportional to amount of charge
  - Better charge resolution than TOT
- Assumption: Charge calibration unchanged after irradiation
- Only single-hit events considered for analysis

Charge distr. of 100 um passive CMOS sensor after 1 x 10^{16} n_{eq}/cm^2



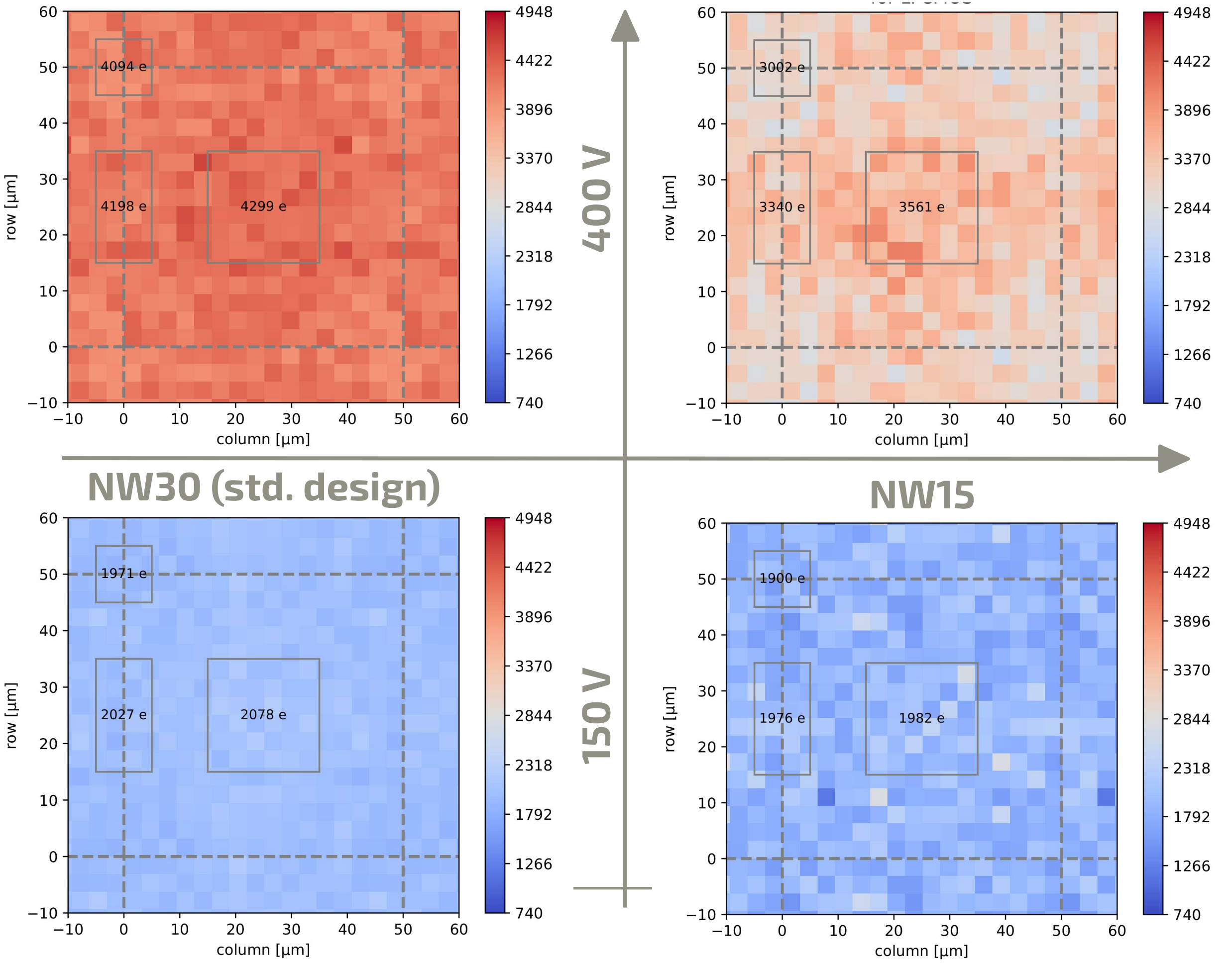
IN-PIXEL CHARGE @ 1 x 10^{16} n_{eq}/cm^2

- High bias voltage + large n-implants
  - Homogeneous charge within pixels
- Flavors with small n-implants:
  - Low charge at pixel corners

    → Due to low electric field and thus, more charge trapping

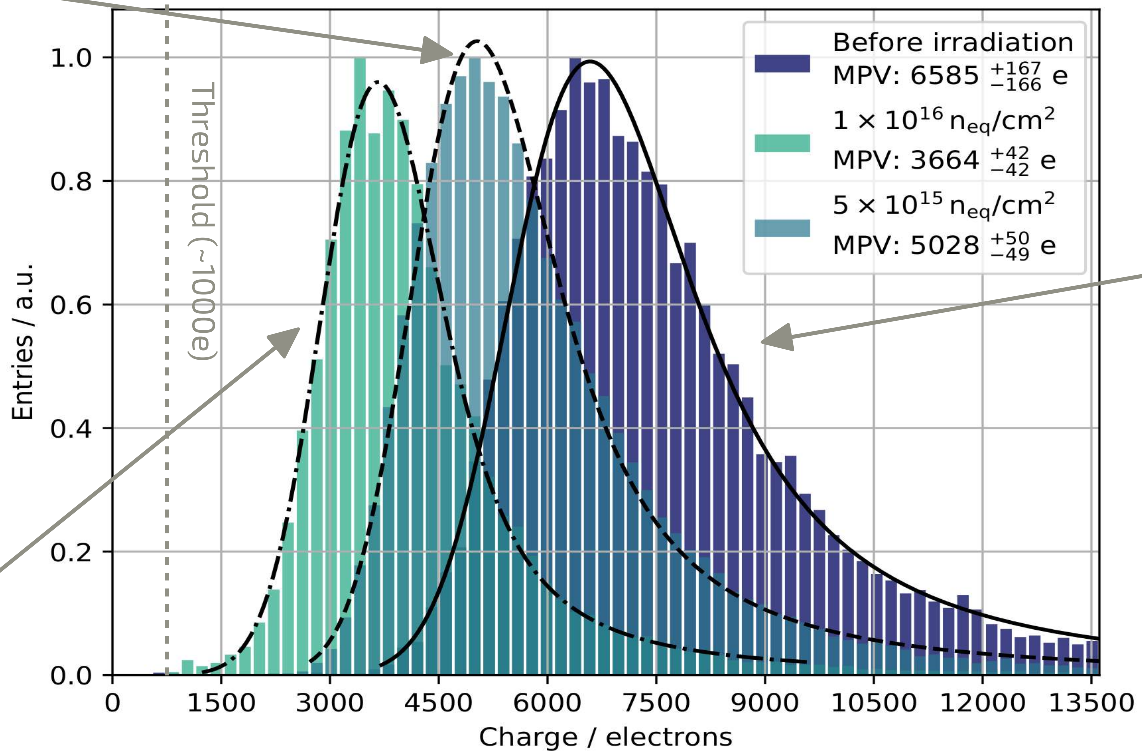
    → Explains efficiency loss
- Amount of charge increases with bias voltage and n-implant size
- @ 150 V: Threshold cuts into Landau

  → No reliable estimation of mean charge



CHARGE: UNIRRADIATED VS IRRADIATED

NW30 @ 350 V
($5 \times 10^{15}\ n_{eq}/cm^2$)



NW30 @ 80 V
(unirradiated)

NW30 @ 400 V
($1 \times 10^{16}\ n_{eq}/cm^2$)

CHARGE VS BIAS VOLTAGE

- Expected charge from MIP (using GEANT4)
  - 73 e/h-pairs per um
  - Before irradiation: 6500 e

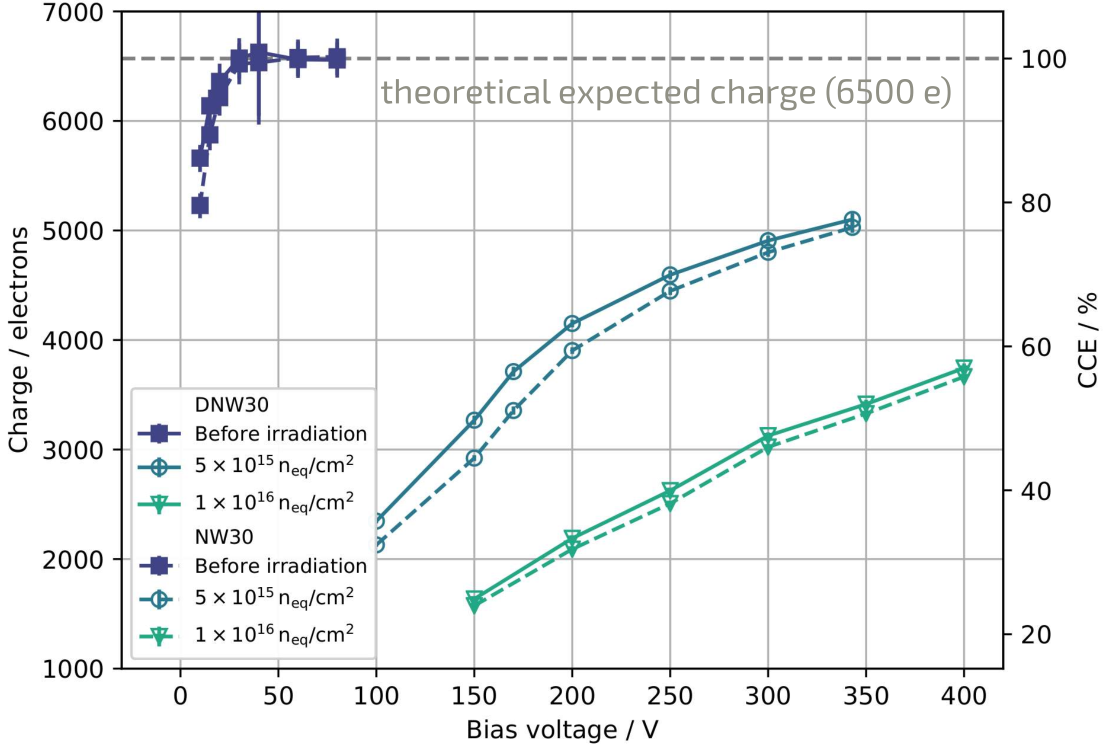
→ 90 um Si (100 um thick incl. metal layers)

- Charge-collection efficiency (CCE):

$$\text{CCE} = \frac{\text{theoretical exp. charge}}{\text{measured charge}}$$

	Charge MPV / e	CCE / %
Before irradiation	~ 6500	100
5×10^{15} n_{eq}/cm^2	~ 5000	~ 80
1×10^{16} n_{eq}/cm^2	~ 3700	~ 60

Collected charge of 100 um passive CMOS sensor



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FULL-SIZE SUBMISSION FOR ATLAS ITK

FULL-SIZE SUBMISSION FOR ATLAS ITK

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- Frontside process: Reticle stitching for large sensors
- Wafers received backside processing
- **150 um thick Float-Zone** wafers instead of Czochralski wafers

Single Sensors

Double Sensors

Quad Sensors

- Not only pixel sensors, also strip sensors: Talk by Jan Cedric Honig

Wafer layout

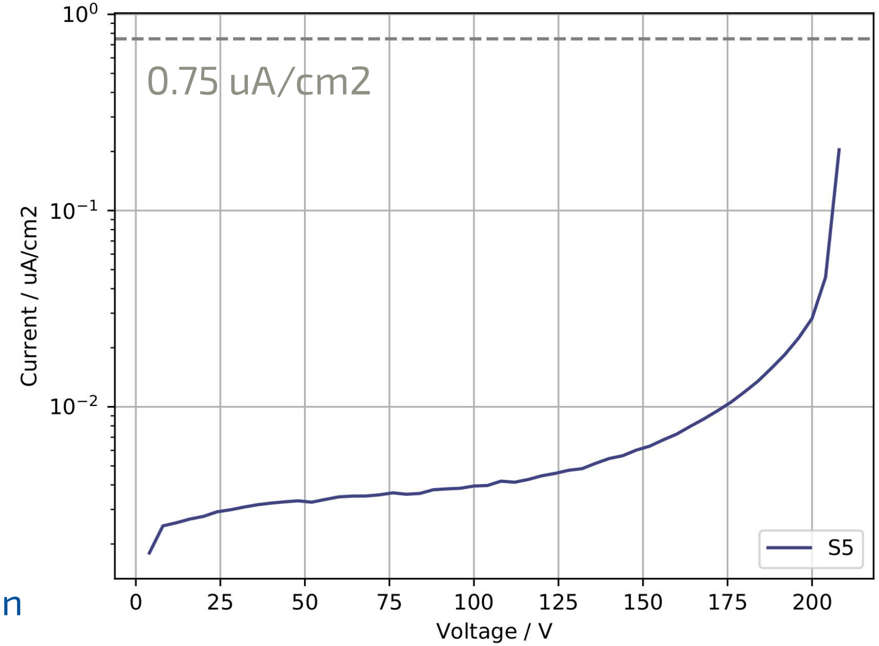
Work done with: A. Macchiolo, D. Münstermann, M. Backhaus

IV-CURVES: FULL-SIZE ATLAS ITK SENSORS

- Had issue with backside processing leading to increase of current when depletion zone touches the backside
- **Solved by increasing the implant-dose of backside implant:**
  - Keeps depletion zone away from damaged silicon at backside
- Sensor requirements:
  - V_{dep} ~ 30V (< 100V, for 150 um) ✓
  - I_{leak} < 0.75 uA/cm² @ 80V (V_{dep} + 50 V) ✓
  - V_{break} ~ 200-180 V (> V_{dep} + 70 V) ✓

  → **Sensors fulfill specifications**
- Measurements on irradiated samples will be performed soon

Example IV-curve



CONCLUSION / OUTLOOK

- Small LF prototype sensor functional and usable after irradiation to **1×10^{16} n_{eq}/cm^2**
- NW30 (std. desgin) after 1×10^{16} n_{eq}/cm^2:
  - @400 V: > 99 % efficiency, 3700 e charge signal

  → Fulfills requirement of > 97 % efficiency after irradiation

  → ~60 % charge-collection efficiency after irradiation
- Nice demonstration that passive CMOS sensors are radiation hard (up to **1×10^{16} n_{eq}/cm^2**)!
- ATLAS-ITk full-size submission:
  - Current increase at full-depletion could be mitigated by increasing the implant dose of the backside implant!
  - Reticle stichting works and first measurements show that sensors fulfill requirements
  - Measurements on irradiated samples will be performed soon