LGADs for 5D Tracking

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Fermilab

- Contributing to aspects of this work - A. Apresyan, R. Heller, G. Gabriele, M. Mannelli, R. Islam, C. Wei, A. Tricoli

Introduction

We describe simulation studies of double sided (inverted) low gain avalanche diodes with small pixel readout on the cathodes. This configuration has the potential to provide 5D (X, Y, Z, T ,θ) tracking information. The concept utilizes:

- 3D integration of electronics for fine pitch, low capacitance pixels and complex on-sensor processing
- Double sided LGADs to provide a distinctive pulse shape and “time expansion” due to slower hole drift
- Substrate engineering with epitaxial and buried layers to allow separate tuning of drift and avalanche fields

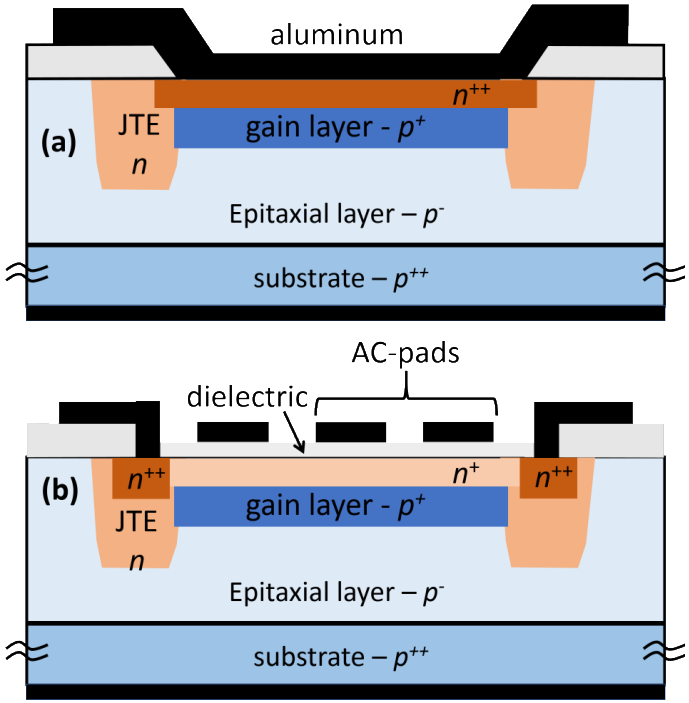
Interest in angle information is motivated by the current CMS track trigger stub concept and possible future FCC-hh and muon collider background reduction applications

This work is based primarily on Silvaco TCAD studies – there is some work shown from an ongoing FNAL/BNL collaboration to study buried layer LGADs

LGADs / AC LGADs

Low gain avalanche diodes now being used for timing layers for CMS and ATLAS have excellent timing capability. But:

- Current versions must have large pixels large due to the areas needed for HV edge termination
- They are not very radiation hard due to low density implants



Gabriele Giacomini et al

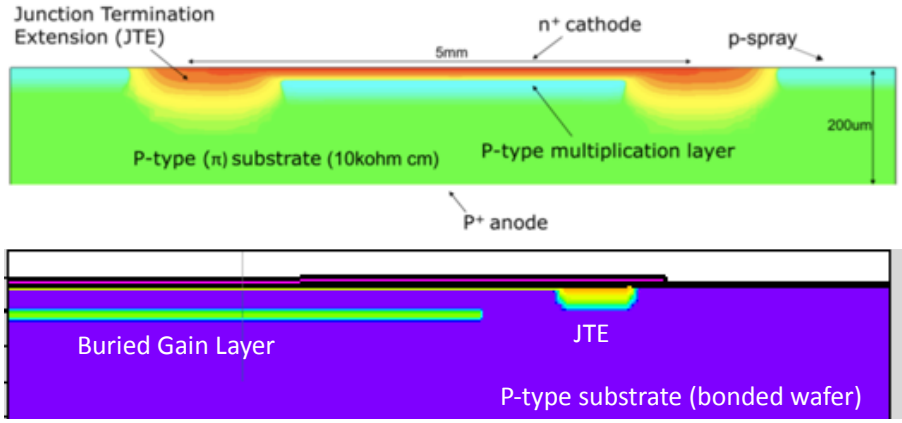
AC-LGADs solve the pixel size problem by adding resistive and capacitive layers and moving the edge terminations from the pixels to the edge of the device.

- Must still be bump or 3D bonded to the readout electronics
- Pixel size and resolution determined by the resistance of the n^+ layer and capacitance from n^+ to the AC pads.

Buried Layers

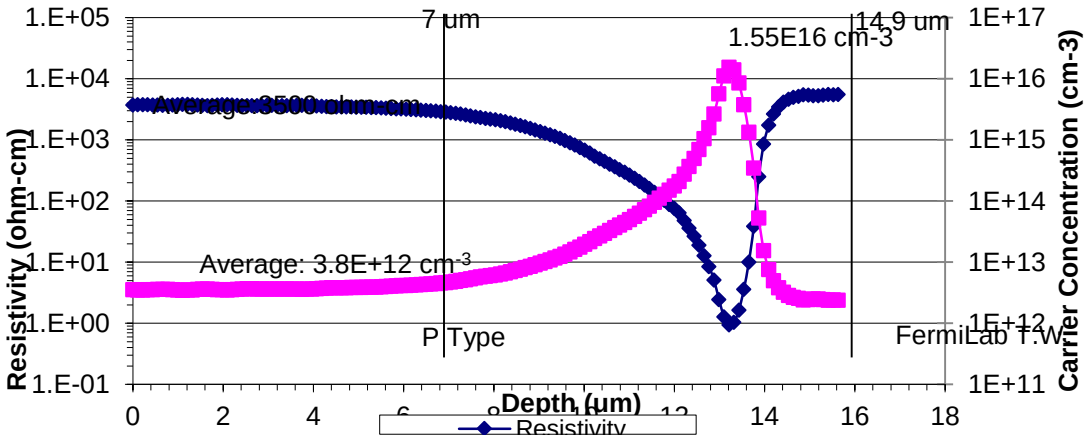
The current generation of LGADs utilize “reach -through” deep implants to provide the high-field gain layer.

- Depth defined/limited by the energies of the implants
- Radiation hardness limited by acceptor removal – related to the gain layer doping density



One can gain flexibility by depositing or implanting a gain dopant, then adding a lightly doped gain layer by epitaxy or wafer bonding.

- Separate control of width and depth of dopant layer
- Can be deposited by implantation or graded epitaxy

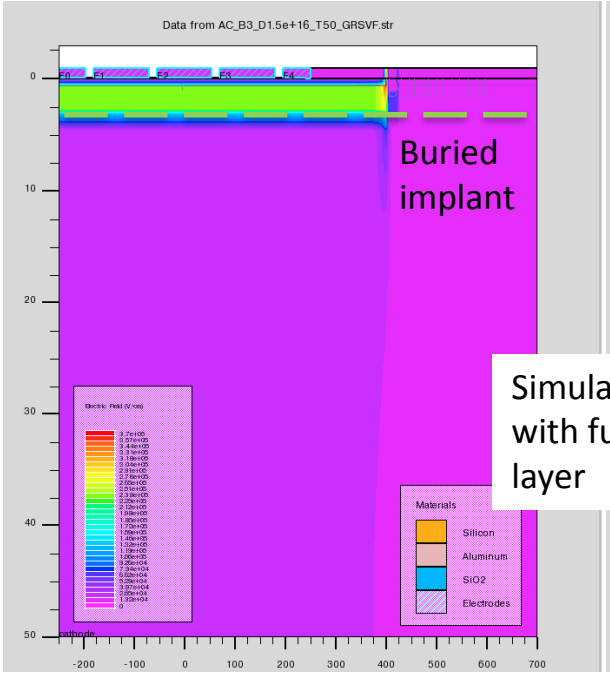


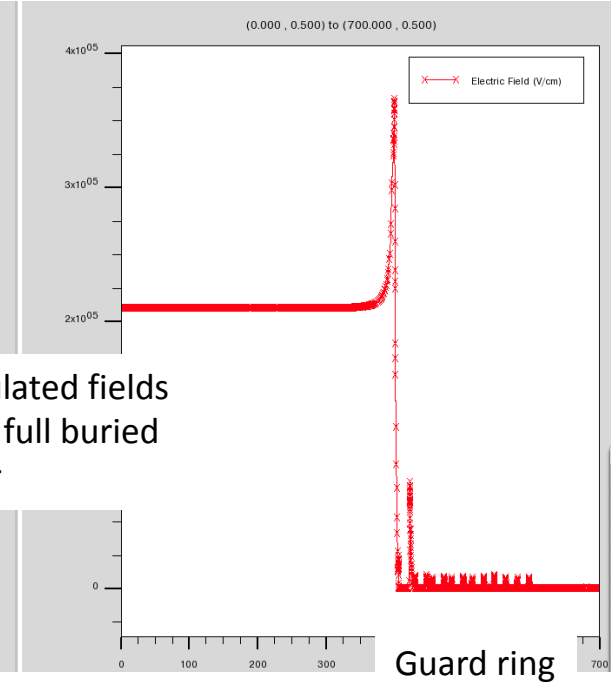
Spreading resistance profile for a graded epitaxy test wafer (Lawrence semiconductor)

Buried Layers (2)

A uniform buried layer is the easiest to achieve by graded epitaxy, but it suffers from the same edge effects as reach-through devices and a deep JTE implant would be needed. Patterning the implant avoids this problem.

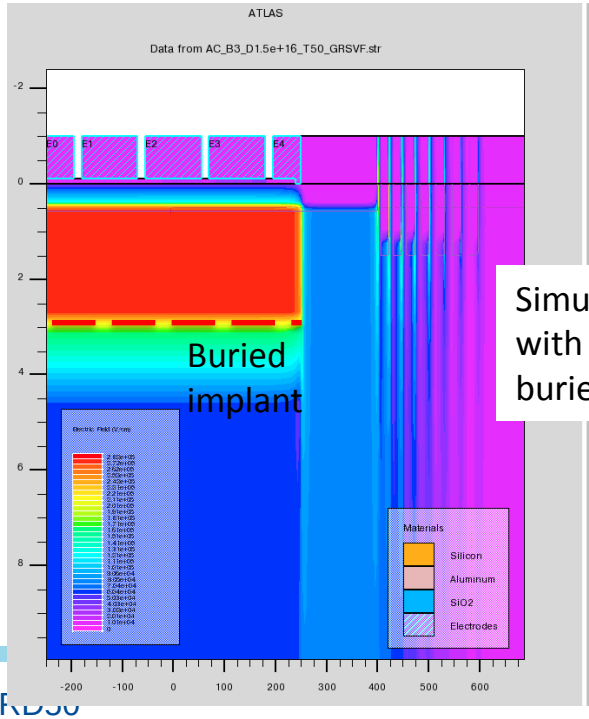
Patterned implantation on the base wafer before epitaxy is more difficult to achieve due to the amorphization of the surface and resulting defects in the epitaxial layer. We see apparent stacking faults in our patterned test devices.

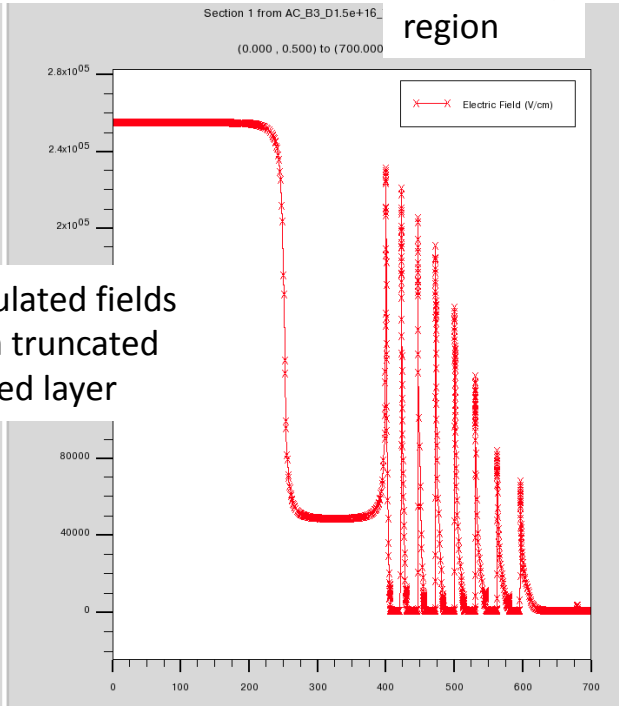




Simulated fields with full buried layer

Guard ring region

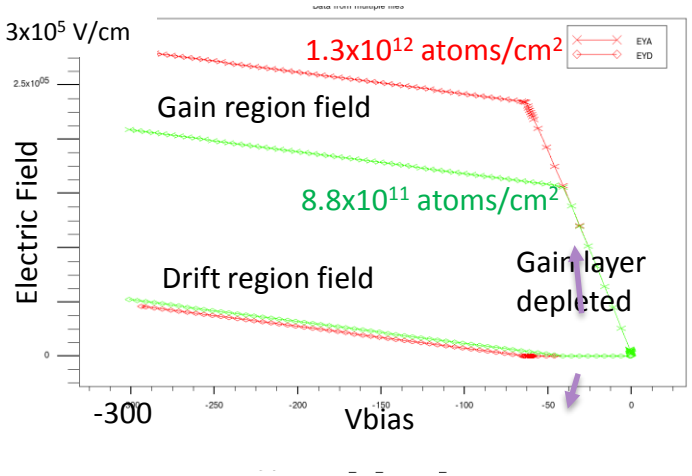


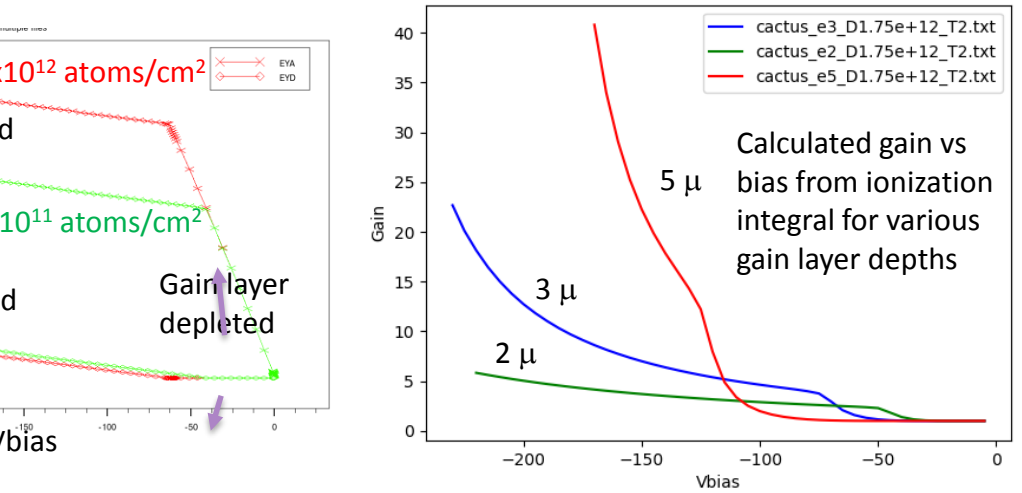


Simulated fields with truncated buried layer

Engineering the Substrate – Buried layers, epitaxy

By engineering the substrate we can design the buried layer LGAD for specific gain, operating voltage, drift field





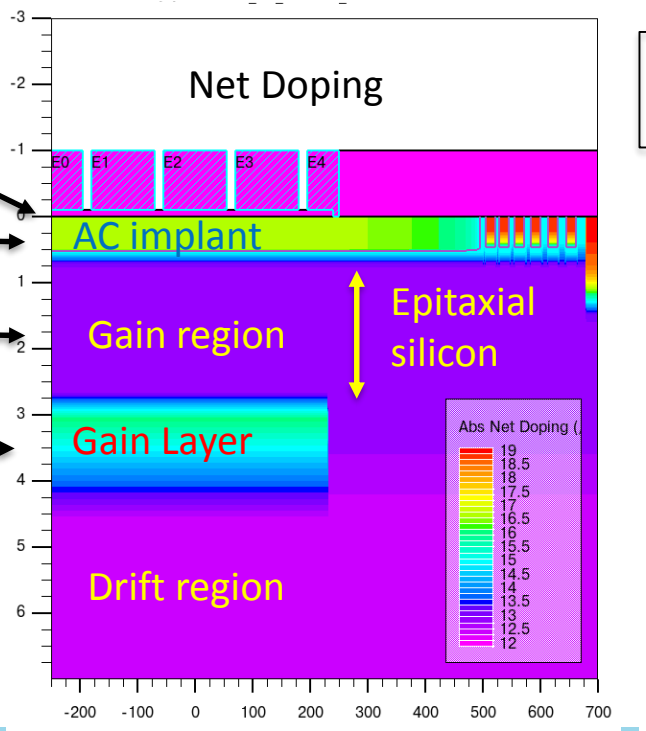
AC oxide – RC time, coupling

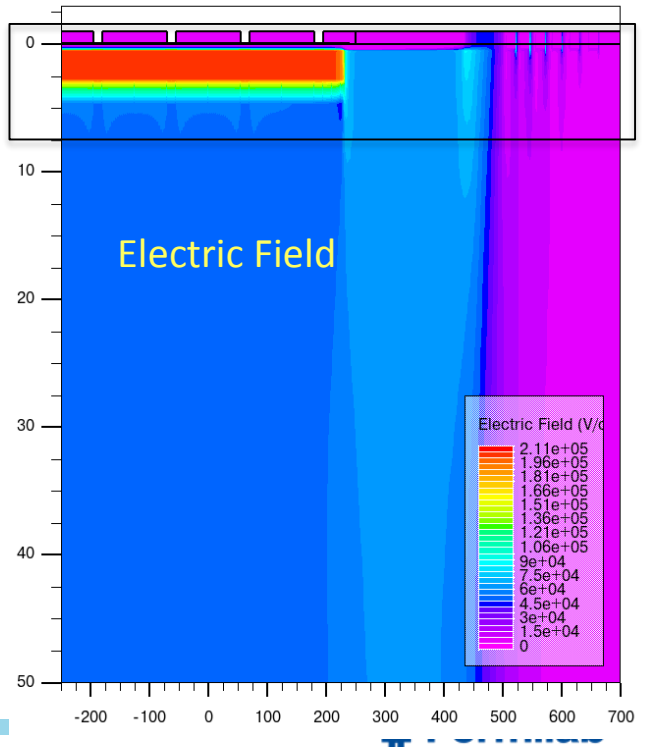
AC layer doping – charge sharing

Gain region – Gain characteristic ~ thickness

Buried gain layer (implanted)

- Total dopant – ratio of drift to avalanche field
- Dopant density – radiation hardness





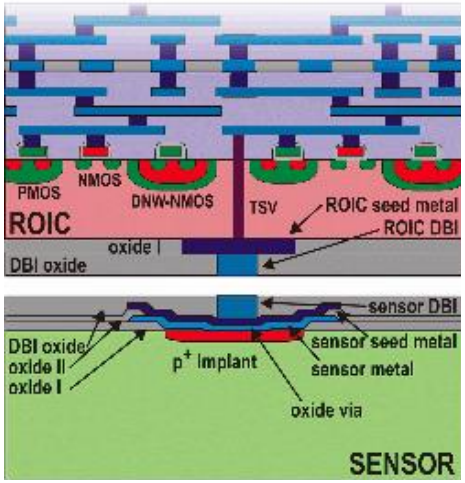
3D Integration (NOT 3D sensors)

A three-dimensional integrated circuit (3D-IC) structure is composed of two or more layers of active electronic components using horizontal intra-tier and vertical inter-tier connectivity by Through-Silicon-Vias (TSVs). We pioneered this for HEP circa 2010-12.

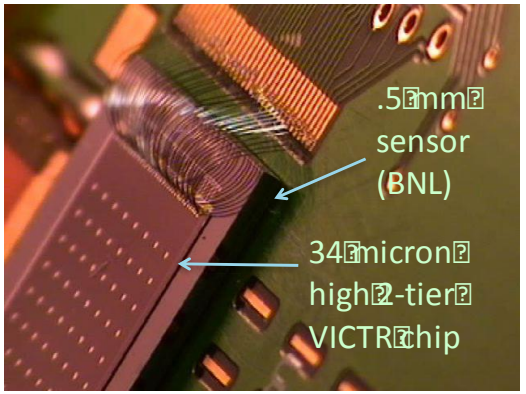
- Very fine pitch (~3 micron)
- Can be rad hard
- Separate optimization of sensors and electronics
  - Sensor optimized for speed and resolution (LGAD or CMOS)
- Multiple layers of electronics would allow processing of fields of pixels – important for angle and charge deposition extraction

Can be combined with MAPS, LGADs, active edge … for optimal combined detector system with complex processing.

"Hybrid Bonding" now a standard technology ("almost all of the stacked CIS manufacturers or their foundries have HB available") DBI licensed to > 20 foundries.

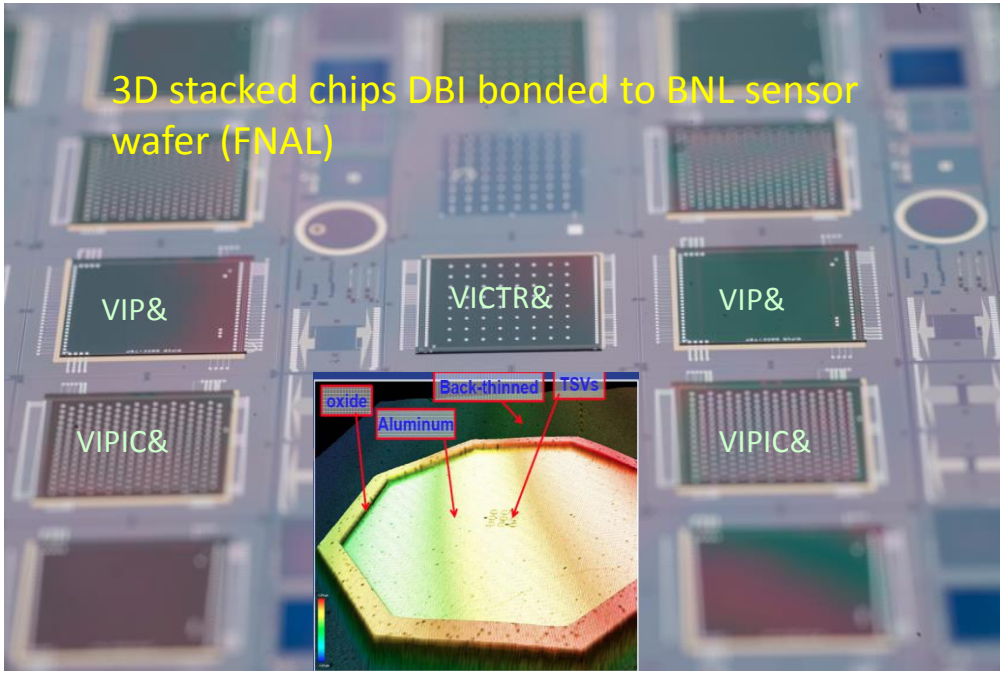


(Deptuch)



Two layers of 130 nm CMOS electronics
Connections from top (or edge)

Possibilities and Challenges

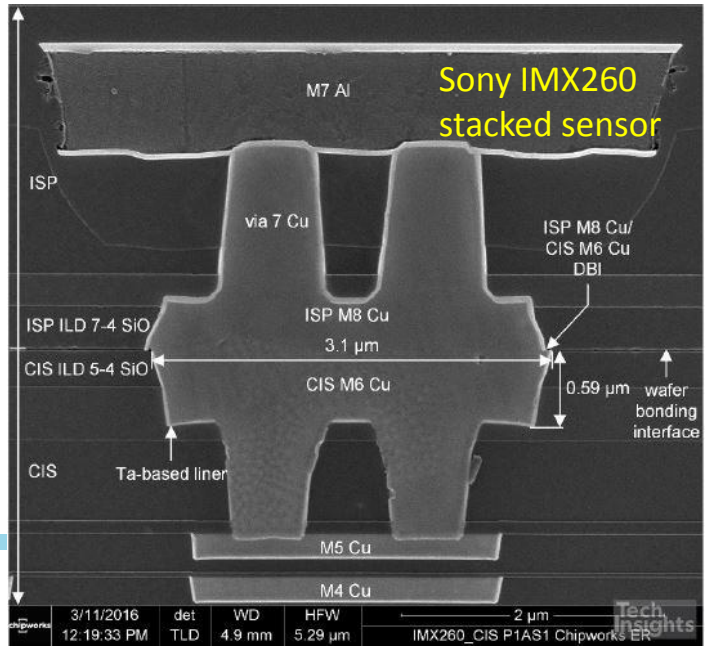


3D integration offers a number of possibilities

- Very fine pitch
- Multiple layers of electronics (analog/digital)
- Low noise (low capacitance interconnect, small pixels)
- Heterogeneous integration (different sensor, IC technologies in a stack)

Challenges

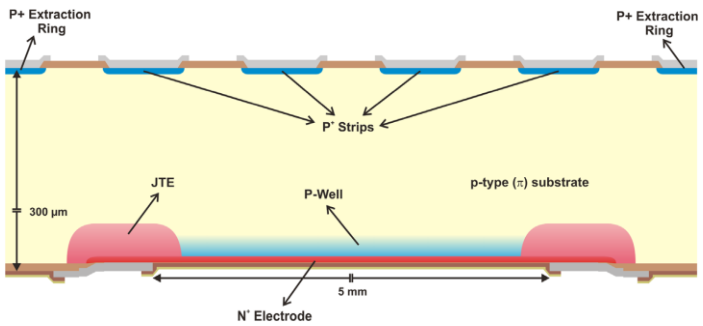
- Access/cost (Nhanced, MIT-LL, Tower/Jazz, Sandia. IZM …)
- TSV integration (only from some foundries)
- Die-to-wafer bonding
- Multi-chip stack yield
- Design tools

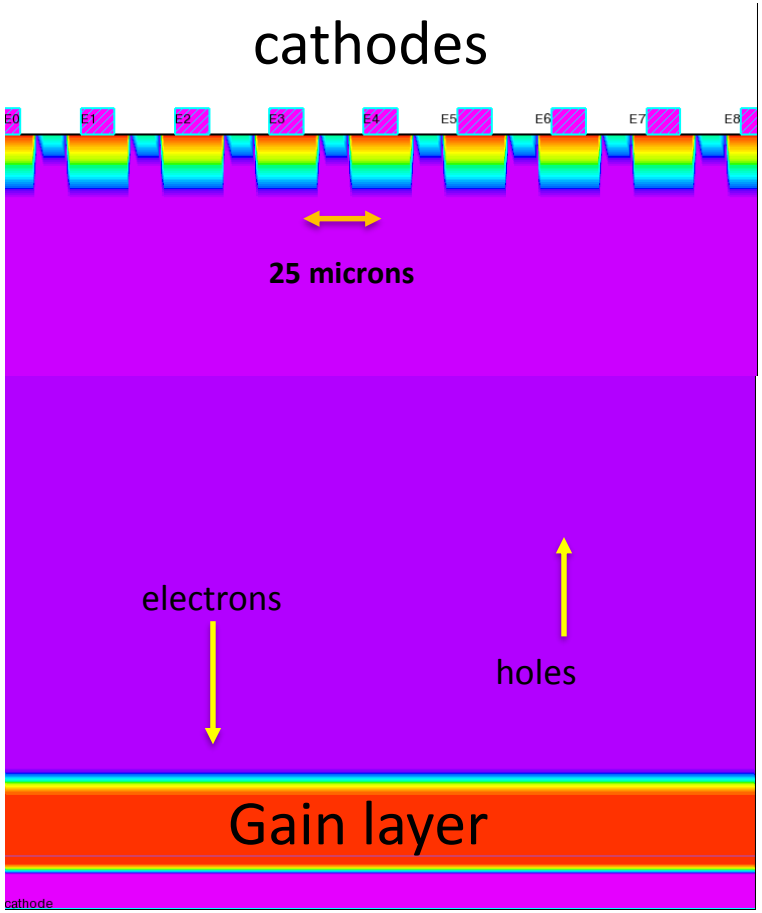


Double Sided (inverse) LGAD – Example of combining Technologies

Low Gain Avalanche Diode with fine pixels on the hole-collecting side (G. Pellegrini et al …)

- Anode can provide timing with coarse pitch
  - Lower total power and complexity
- Cathode subdivided into small pixels
  - Records “primary” hole collection, then holes from gain region – double peak that reflects charge deposition pattern
  - Lower power due to large signal from the gain layer
- Resulting current pattern can be used to measure angle and position.
- A thicker detector can be optimized to measure angle or charge deposit location at some sacrifice to time resolution





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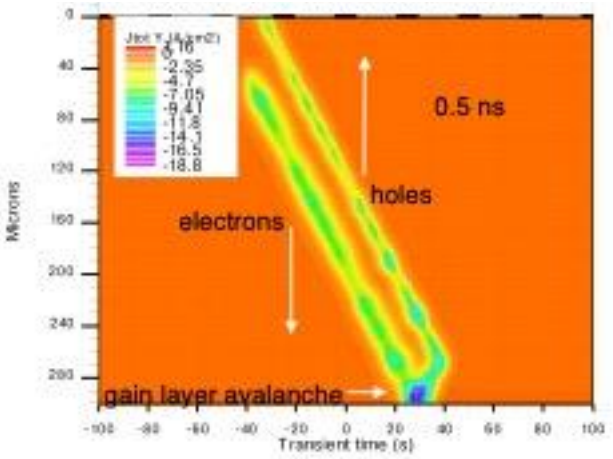
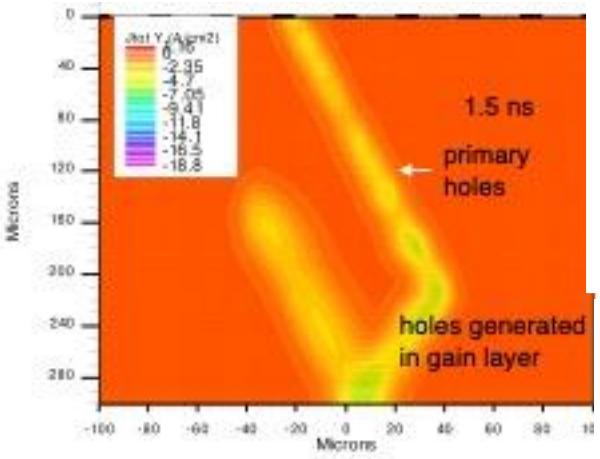
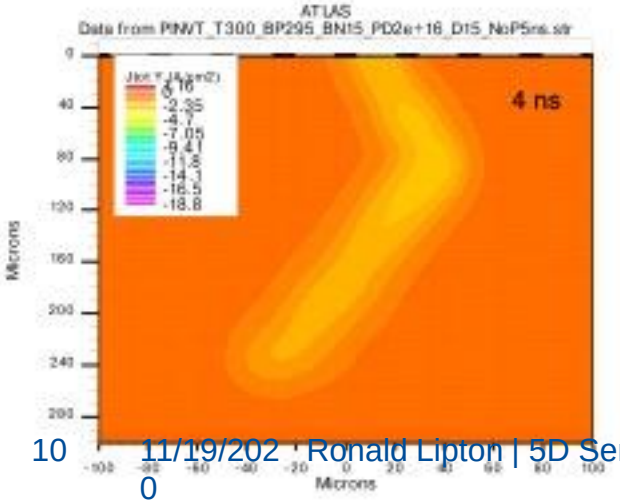
Double Sided LGAD Simulation

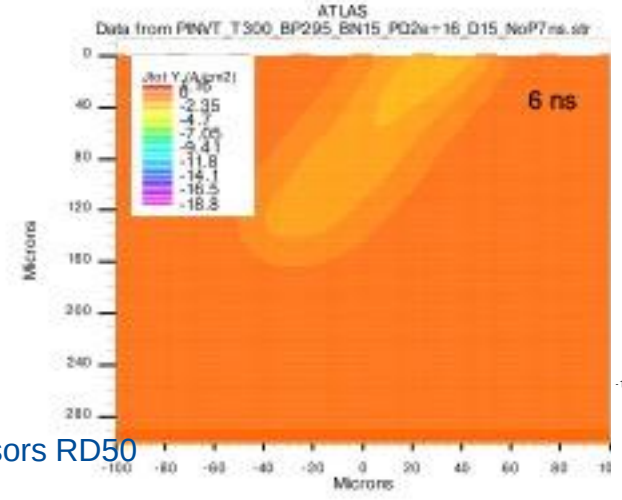
Use anode for timing, cathodes for pulse shape discrimination. Essentially a silicon TPC with gain. Time scale ~ 10 ns rather than 1-2. Significant diffusion.

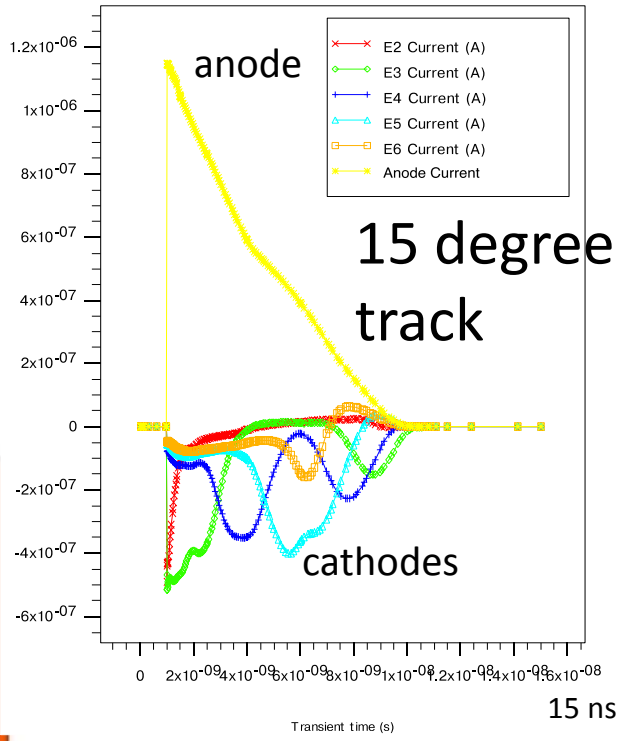
15 degree track detector internal current distributions



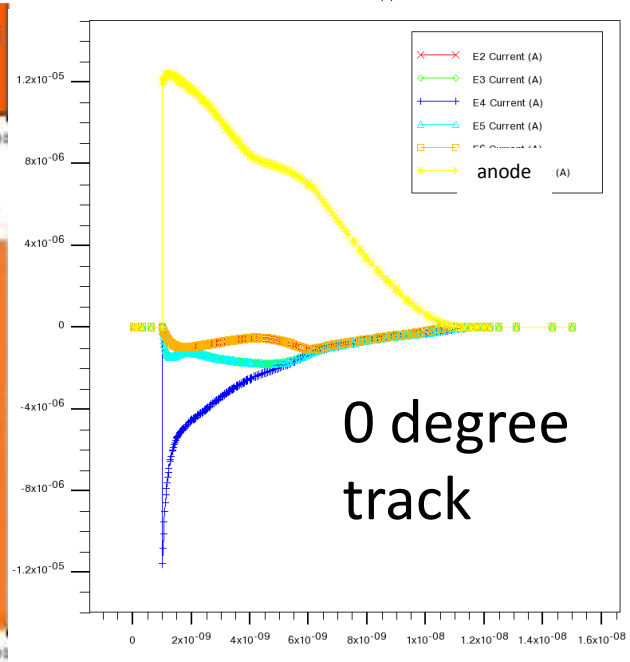






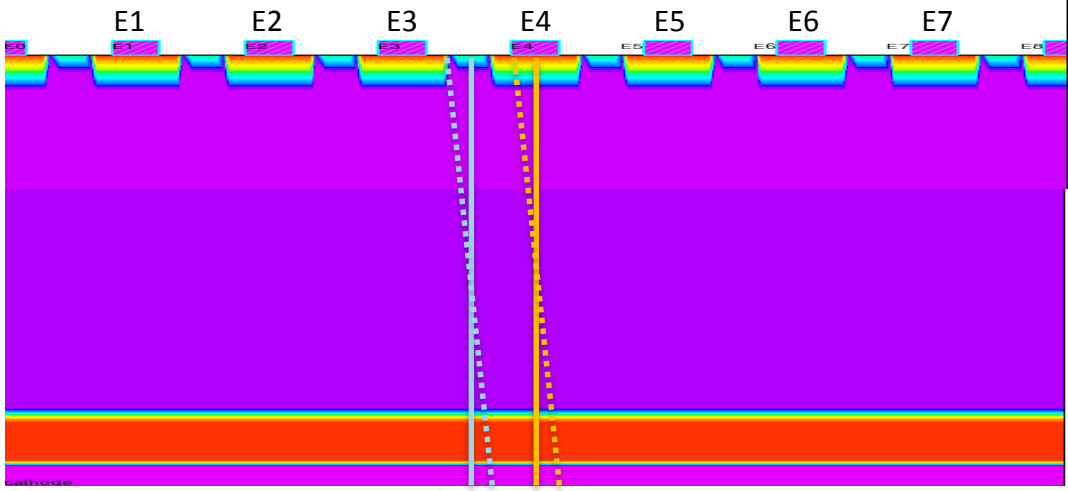


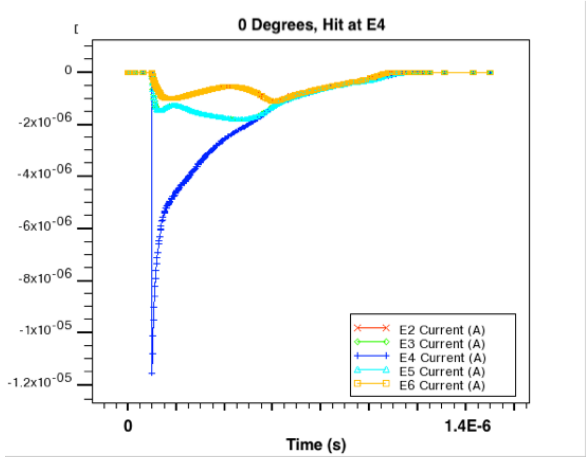
15 ns

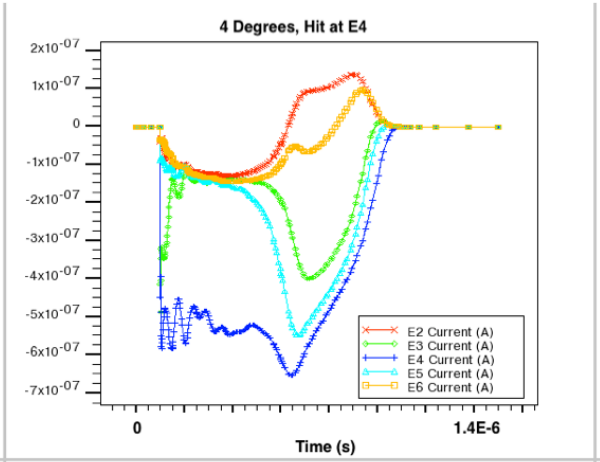


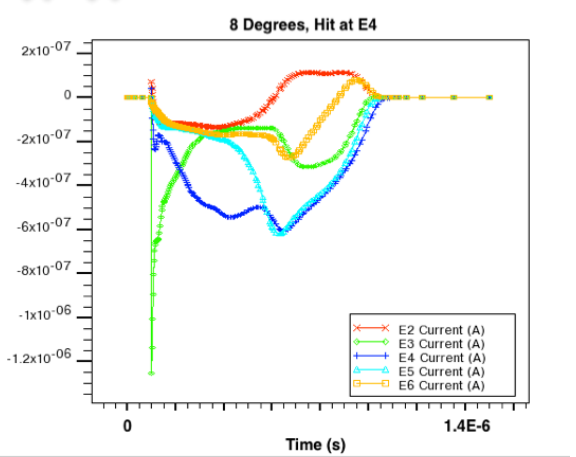
Pulse Shapes

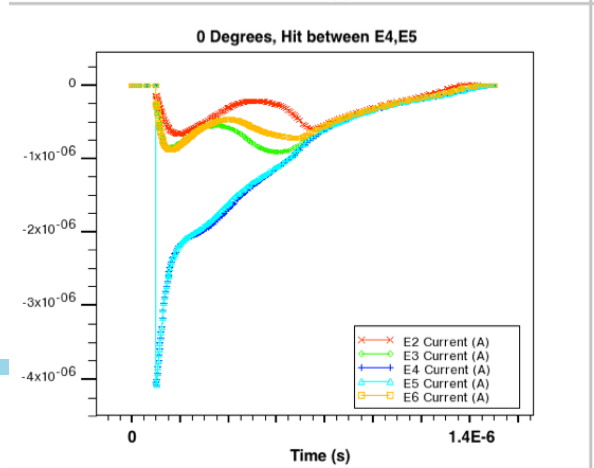
Pulse shapes are complex, may be difficult to unfold the angle, impact position. Much information at 6-7 ns – depends on drift field. Significant induced current signals away from collecting electrodes.

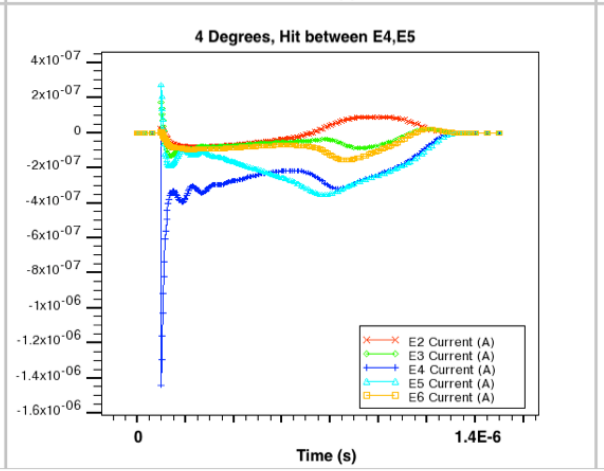


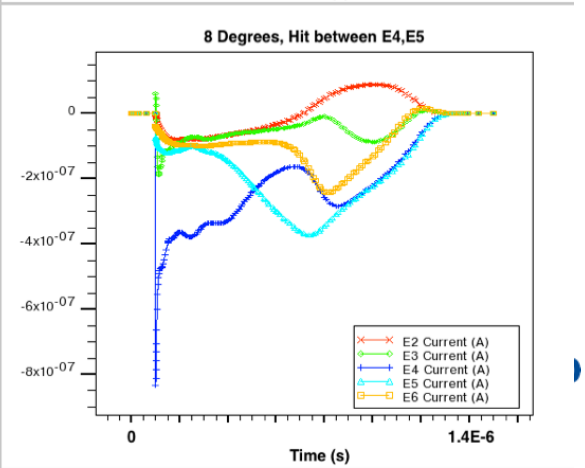








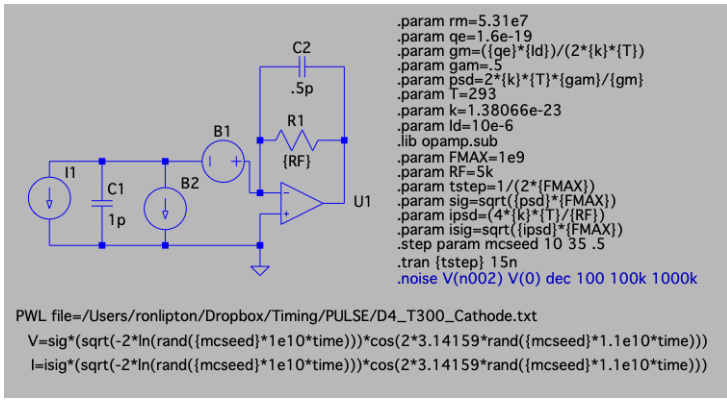


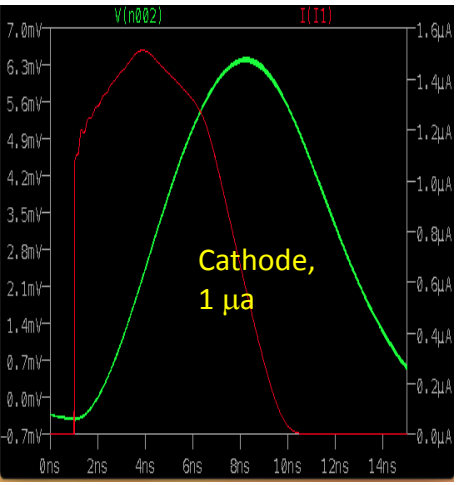


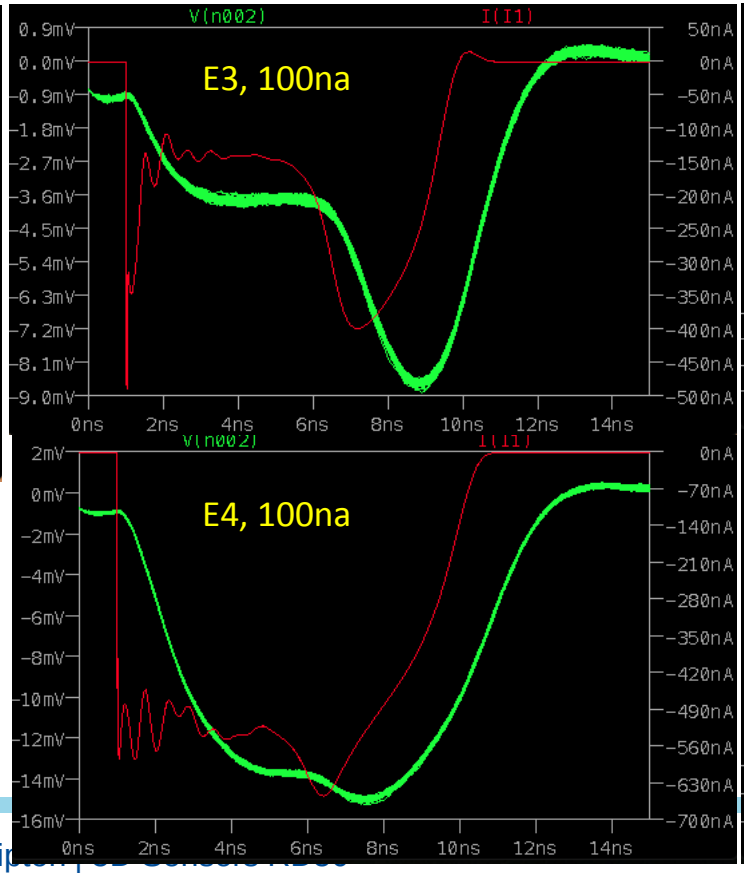
Estimating Amplifier Effects

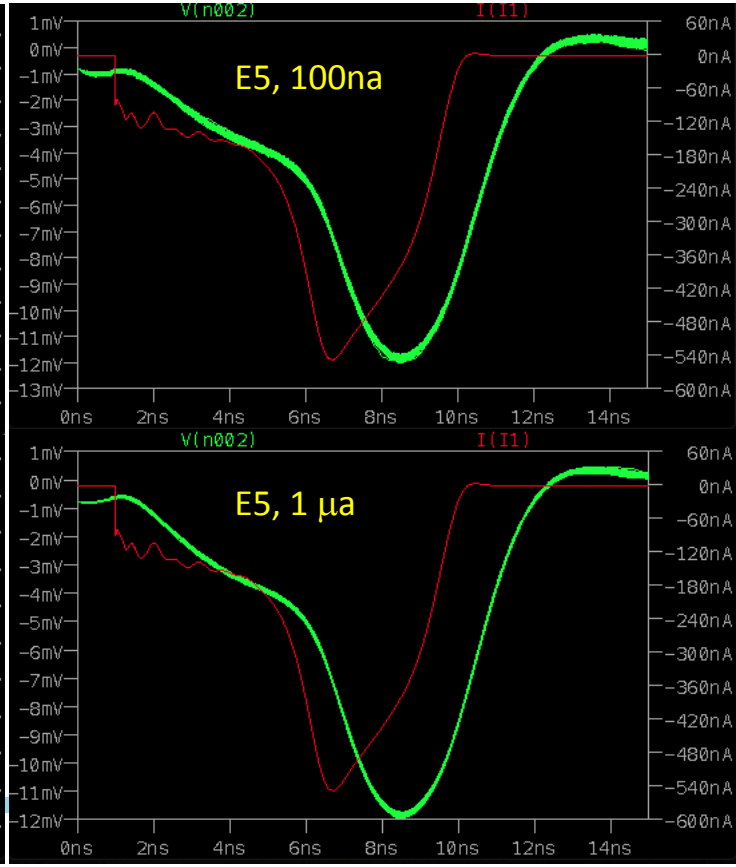
Simple SPICE amp model using TCAD current shapes. Noise parameterized by front-end transistor transductance – 20 ff load – just a BOE estimate

Front end transistor power – 16 mW/cm2 + disc (> 80 mW/cm^2) + digital …





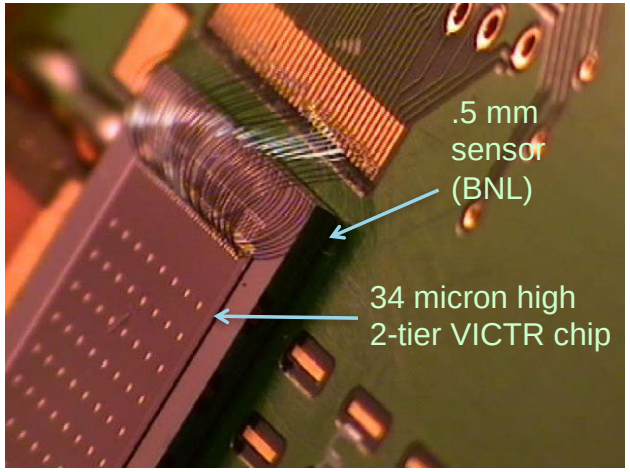


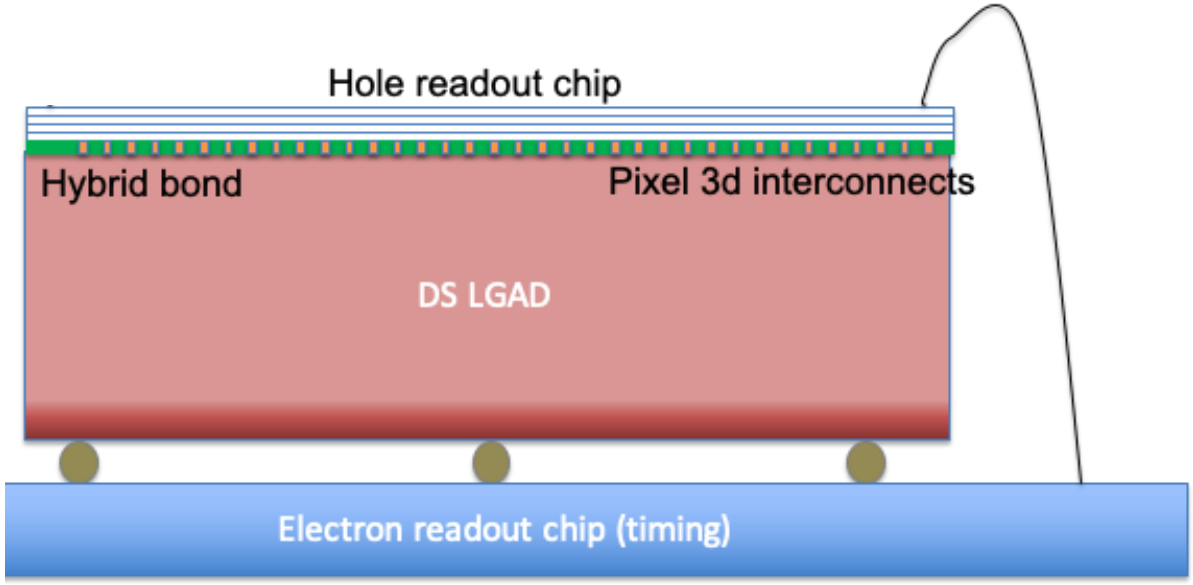


Implementation

- 3D Assembly with electron and hole ROICs
- This is similar to VICTR from the 2012 3D run using chip to wafer bonding

The geometry is admittedly awkward, the anodes must be AC coupled to isolate the bias voltage. Dead regions are needed for top-bottom interconnect. This could be limited to one edge.





Issues

This has been primarily a TCAD exercise to explore the concept. There are several outstanding issues

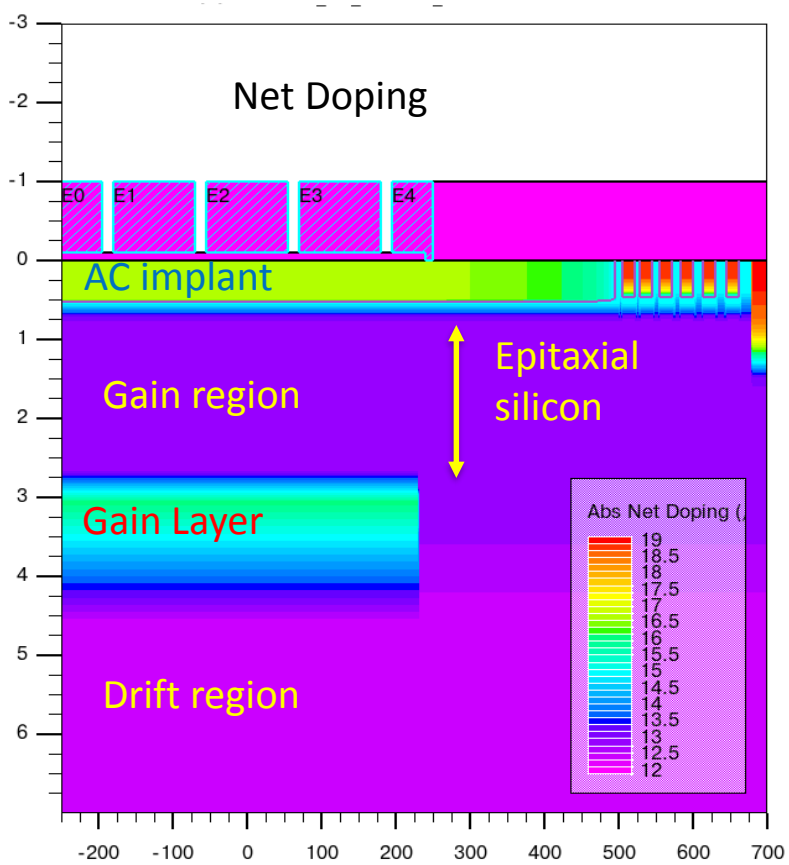
- The pulse shapes are complex – the effort needed to reconstruct angle and accuracy of the results has not been established
- A thicker detector does not provide optimal time resolution.
- Power is an issue anytime one combines fast timing and high pixel density
  - A possible low-ish power mode is to latch several waveform values of the cathode pulses based on an anode trigger with later pulse processing
- The viability of pattered buried layers has yet to be established
- Design optimization would depend on the final application.
- 3D assembly is complex and access limited – I believe this will become easier over time (now limited by TSV insertion)

Current Work

We (FNAL, BNL, Cactus Materials) are prototyping a buried layer device with

- 50 μ drift region FZ wafer Si-Si bonded to the substrate.
- Patterned gain layer implant – removes need for junction termination extension
- 3-4 μ epitaxial gain region over gain layer
- AC coupling top layer

This design allows independent control of the depth of the gain layer; a thin, high density gain layer implant. Recently received a first batch.



Summary

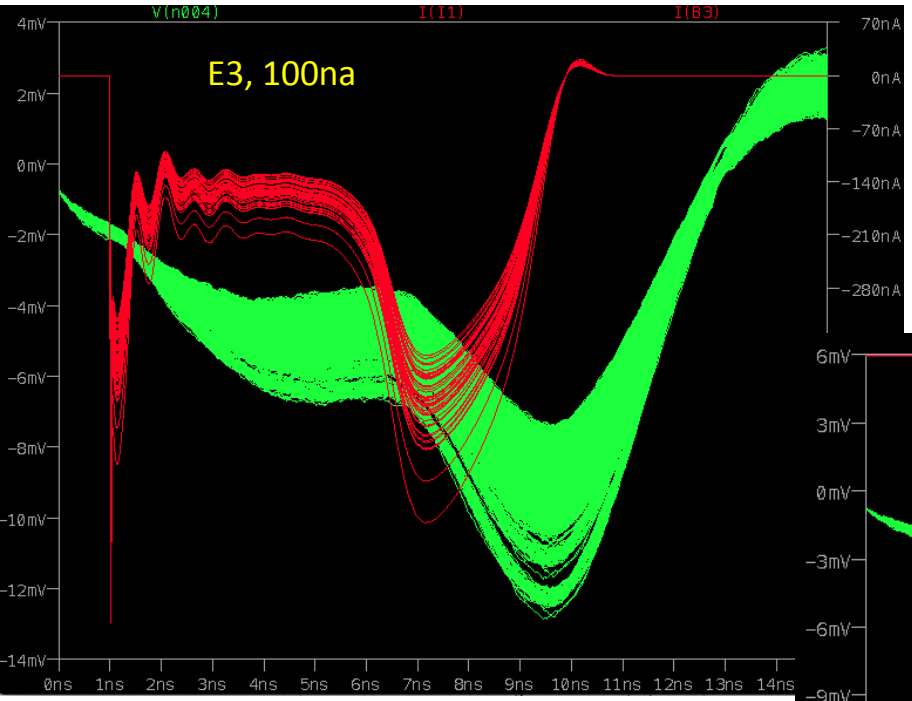
We have described a concept that utilizes 3D integration, substrate engineering and LGAD ideas to potentially reconstruct track angles as well as provide X,Y and time information.

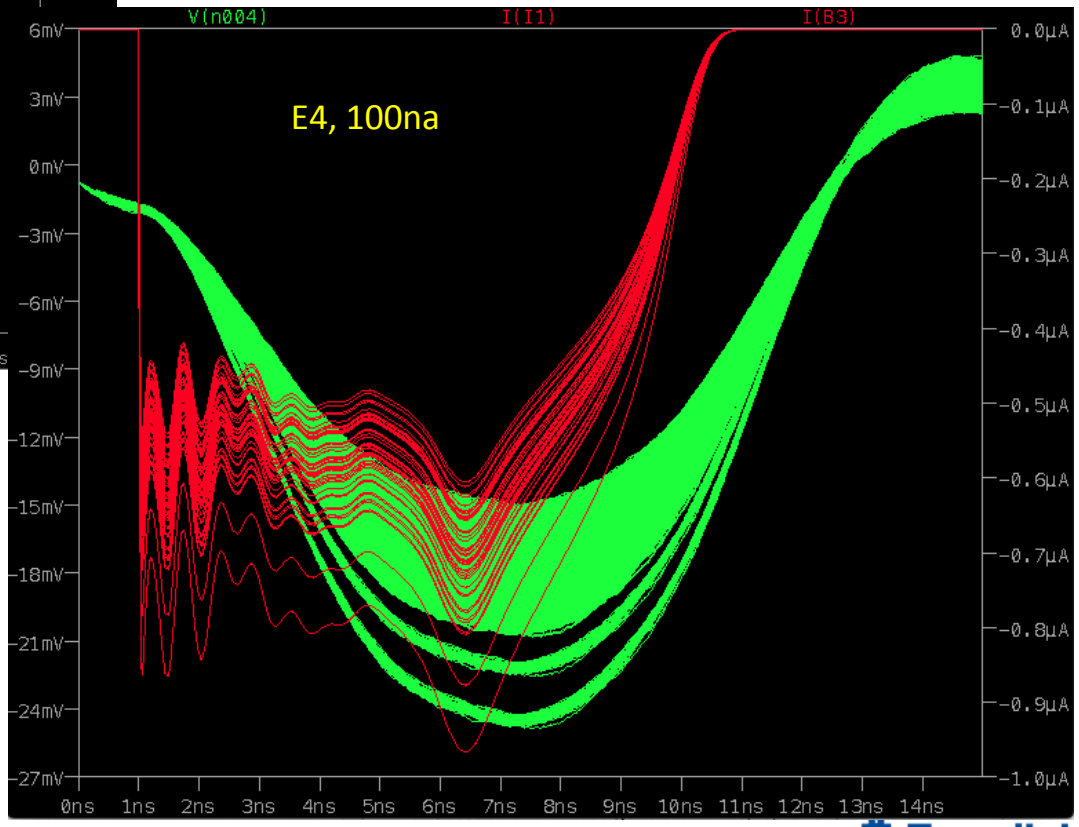
- The buried layer concept has the potential to allow independent tuning of implant density, depth, and drift and gain fields.
- 3D integration allows for dense analog and digital circuitry for post-processing and readout

The 5D LGAD is an example of combining these technologies.

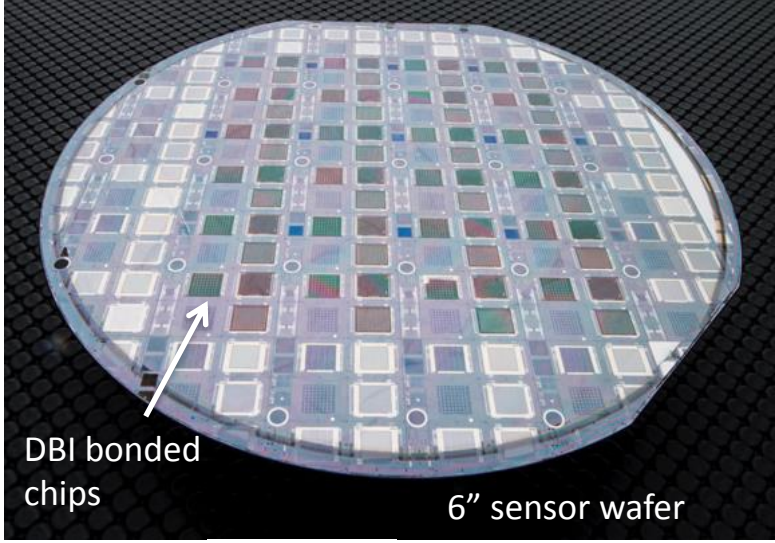
Work is currently underway to explore patterned buried layers.

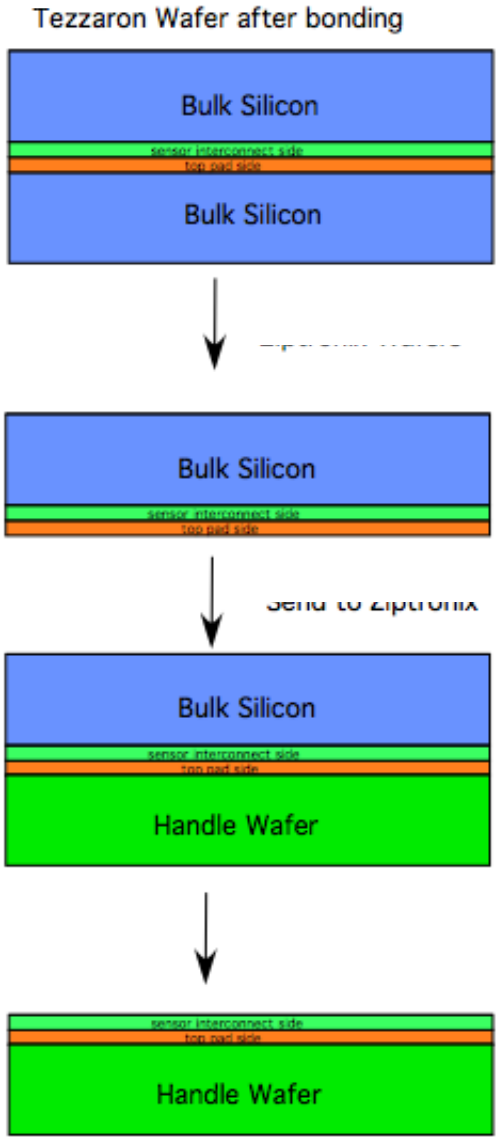
Include Landau Fluctuations of peak





DBI bonding of ROICs (VICTR, VIPIC, VIP) to BNL sensor wafer



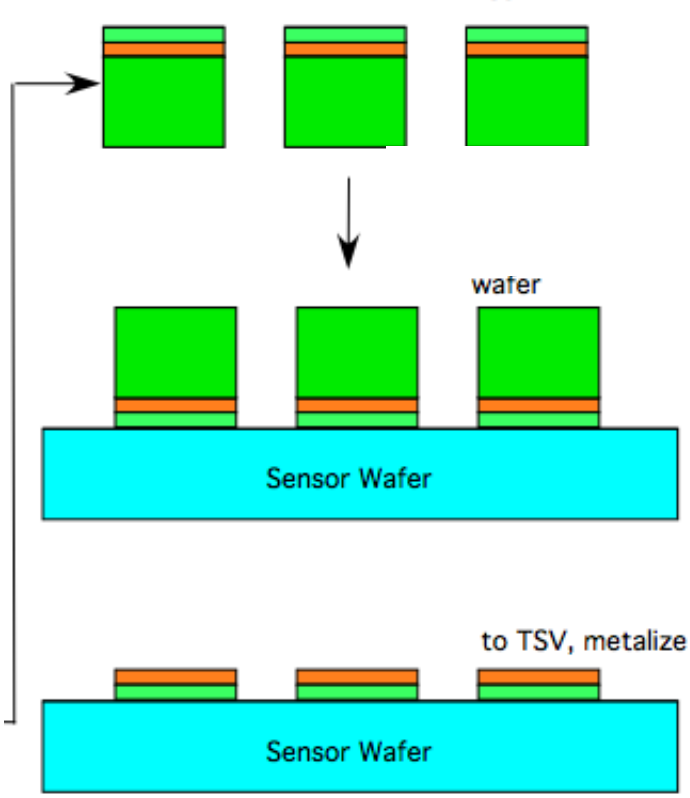


Wafer-wafer 3D Bond

Expose TSVs, pattern Top aluminum

Oxide bond Handle wafer

Expose sensor side TSVs, pattern DBI structures



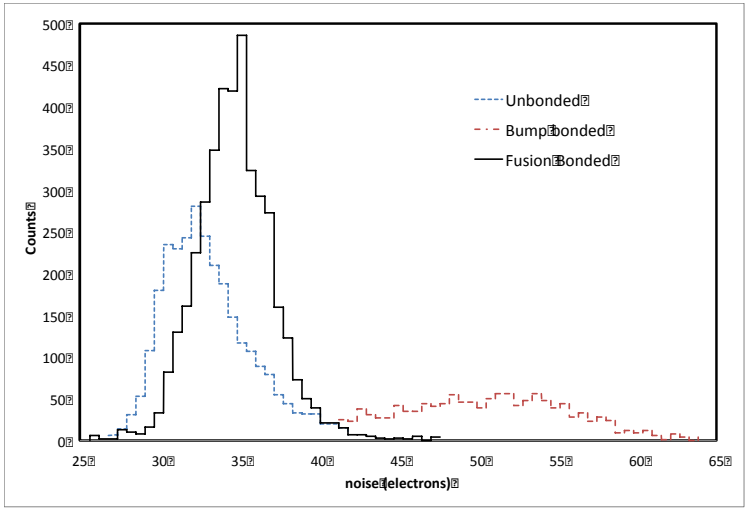
Dice

DBI bond ROIC chips to sensor wafer (RT pick+Place)

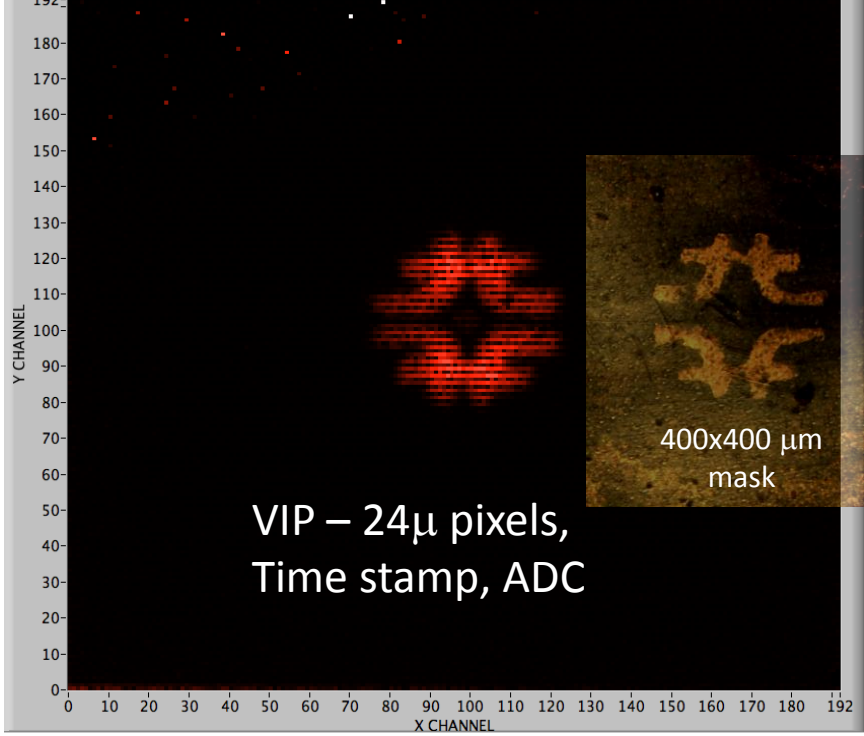
Grind and etch to expose top connections

3D Test Results

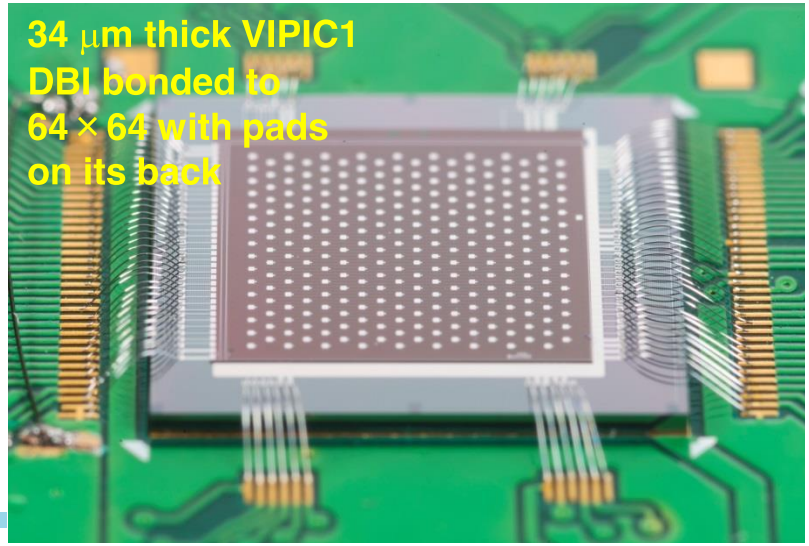
- All three 3D Chips worked – VIP and VICTR tested on the bench. VIPIC was extensively tested in particle and x-ray beams.
- Yields were about 50% - 3D bonding and multiple tier assembly
- VIP(ILC) is on hold – no ILC R&D funds VICTR not relevant to current CMS design



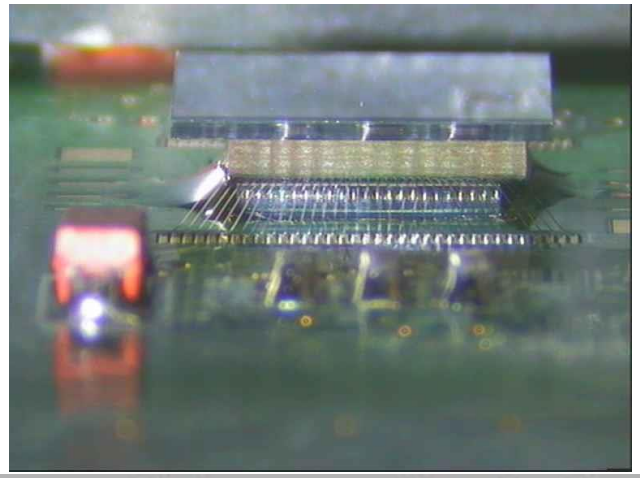
For the VIPIC x-ray imaging chip we were able to compare noise of the oxide-bonded pixels to the same chip with bump bonds. The noise in the oxide bonded pixels is almost a factor of two lower than the conventionally bump bonded parts due to lower capacitance.

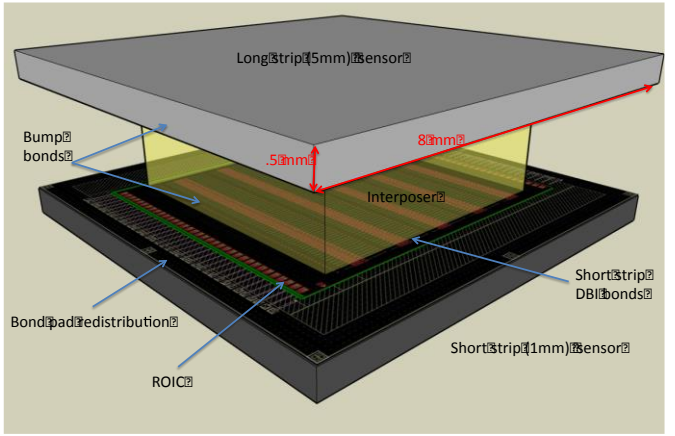


CD109 radiogram of tungsten mask



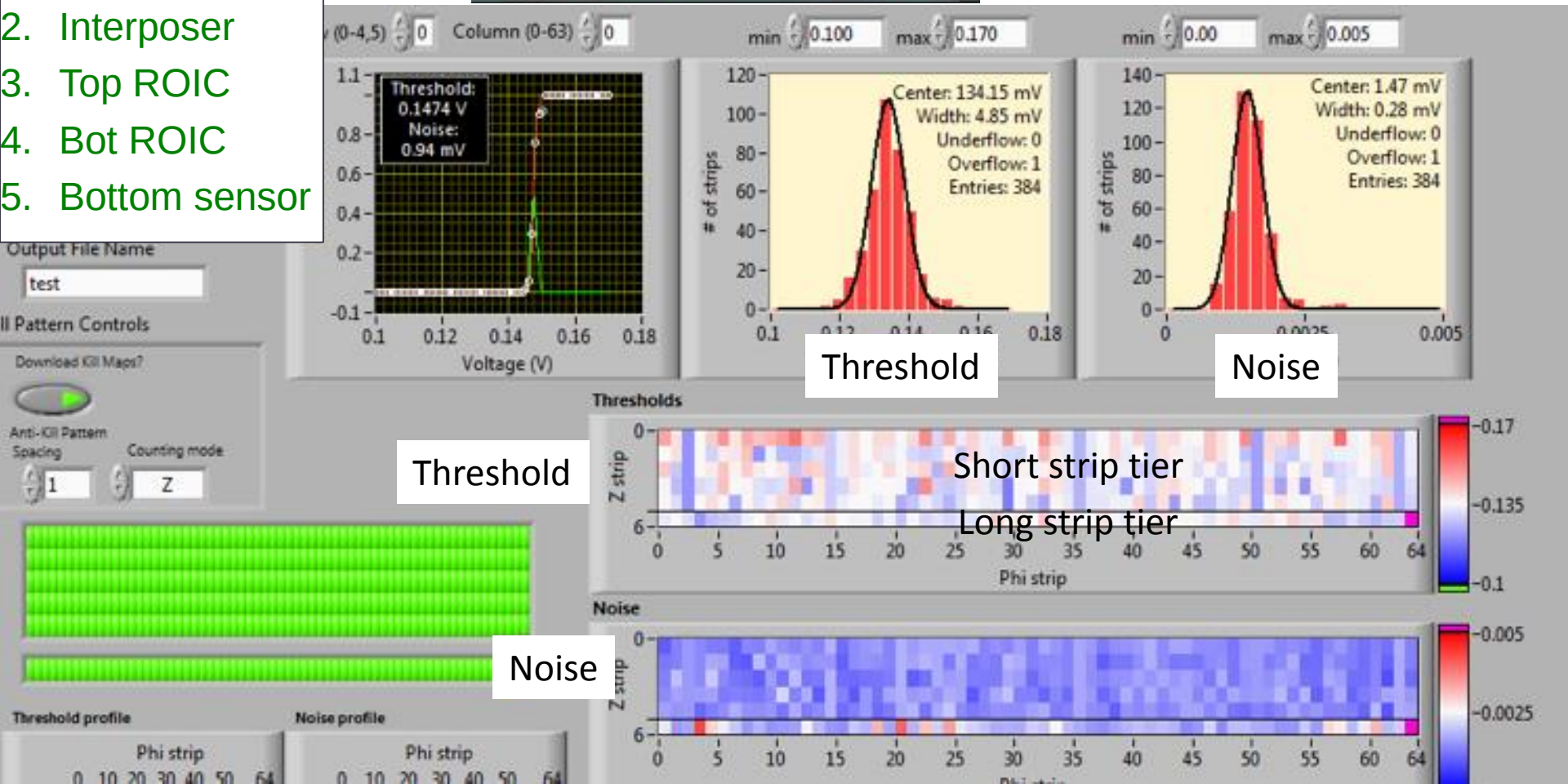
3D Results – VICTR – CMS 5 Tier track trigger chip

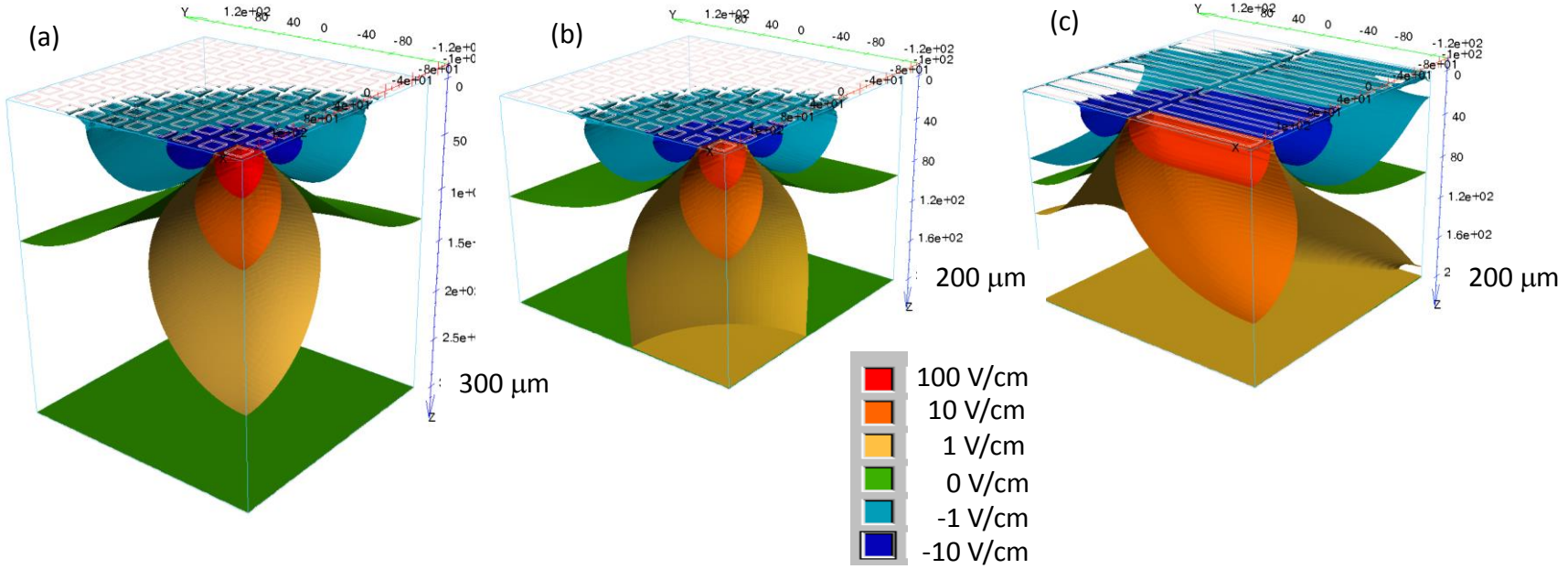




5 layer stack:

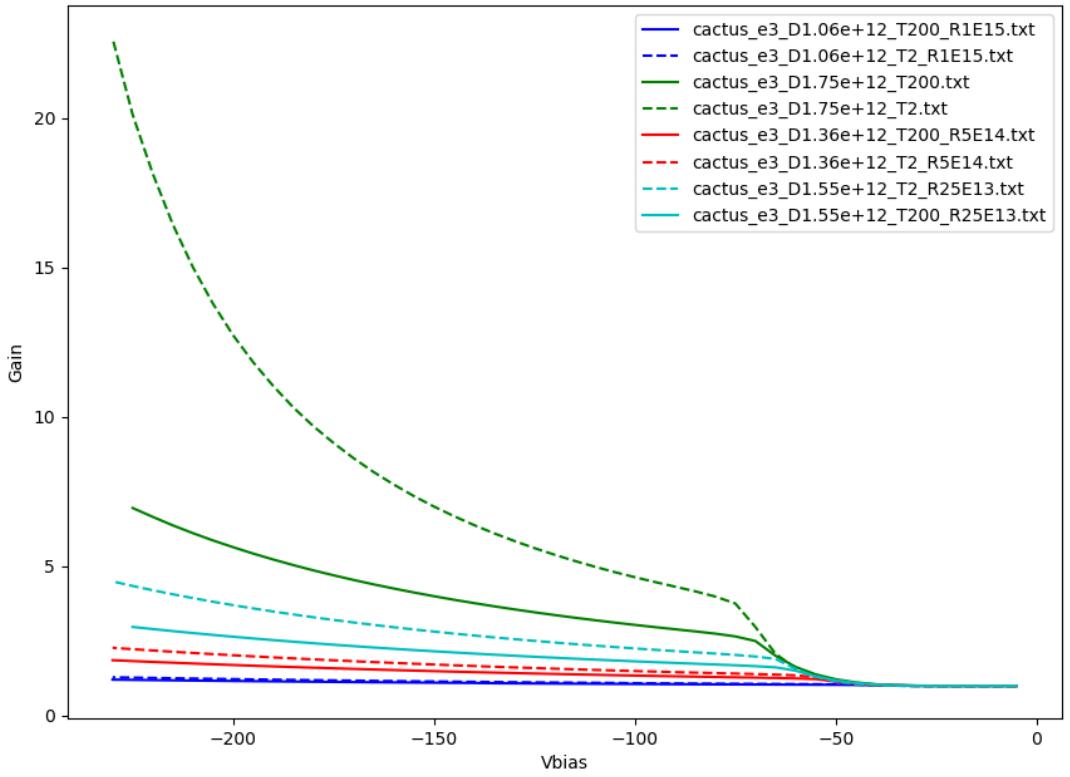
1. Top Sensor
2. Interposer
3. Top ROIC
4. Bot ROIC
5. Bottom sensor

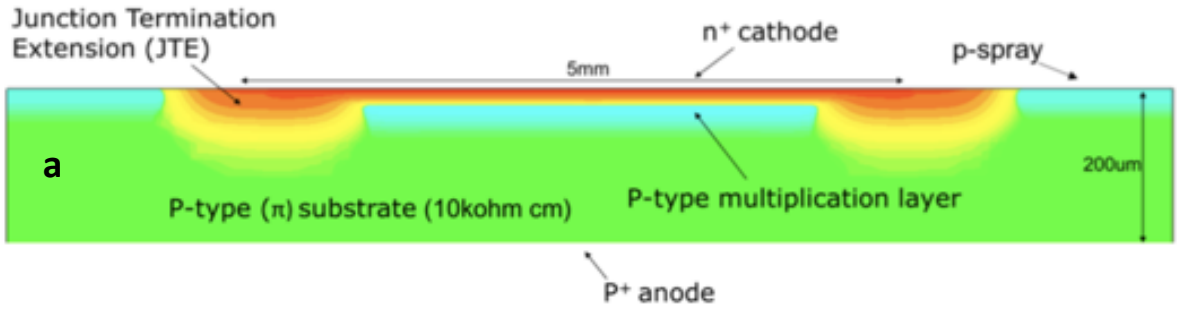


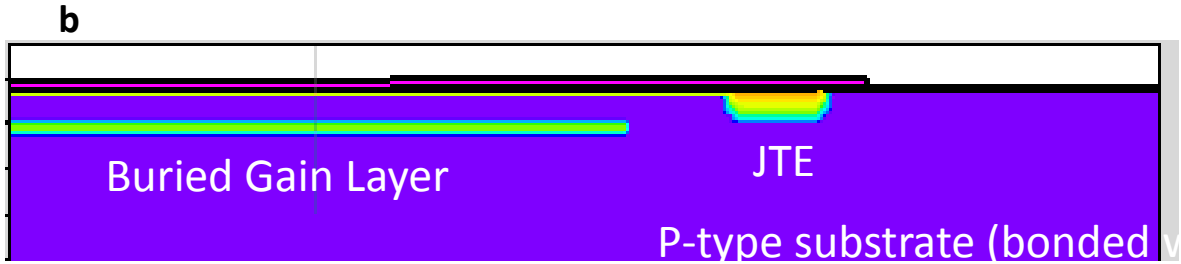

(a)
(b)
(c)
300 μm
200 μm
200 μm
100 V/cm
10 V/cm
1 V/cm
0 V/cm
-1 V/cm
-10 V/cm

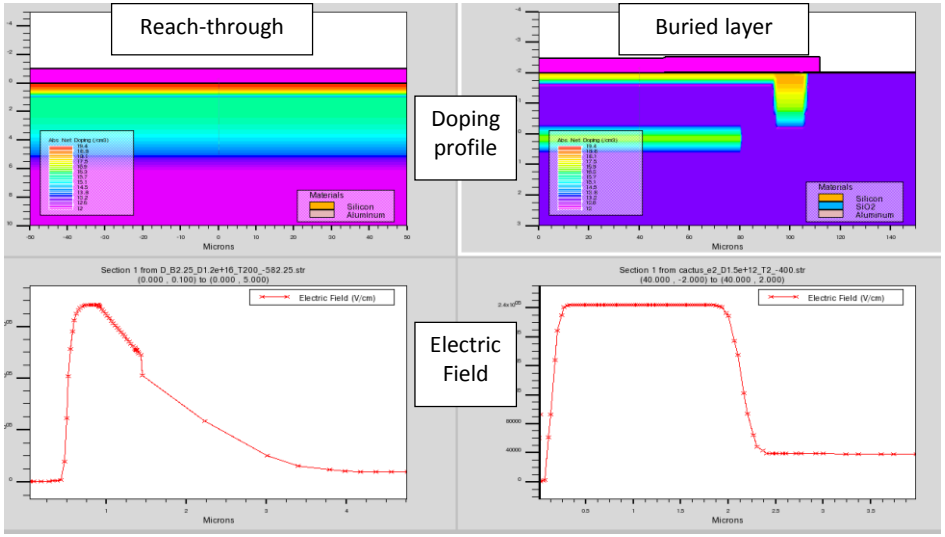
Gain as a function of fluence

- Plot gain for different fluence values for high and low density gain layers with starting dose of $1.75x10^{12}$. All runs ended by compliance limit.
- cactus_e3_D1.36e+12_T2_R5E14
- D = Dose – 1.75x1012 – calculated acceptor removal
- T = Anneal time (minutes)
- R = Radiation fluence




Junction Termination
Extension (JTE)
n+ cathode
5mm
p-spray
a
200um
P-type (π) substrate (10kohm cm)
P-type multiplication layer
P+ anode


b
Buried Gain Layer
JTE
P-type substrate (bonded


Reach-through
Buried layer
Doping profile
Electric Field
Materials
Silicon
Aluminum
SiO2
Microns
Electric Field (V/cm)