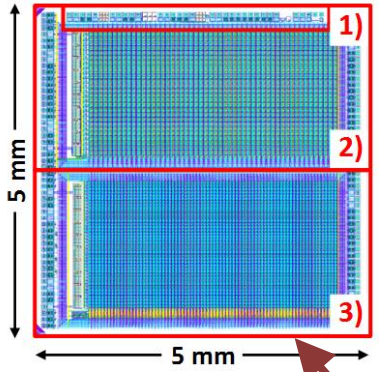
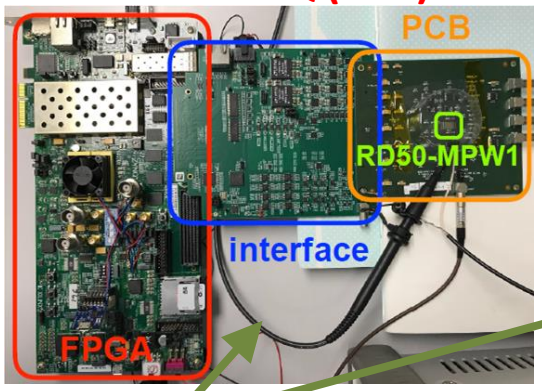
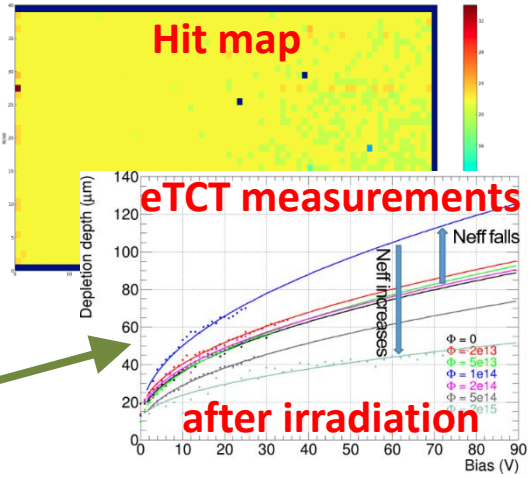
RD50 CMOS timeline

RD50-MPW1



RD50 DAQ (CaR)

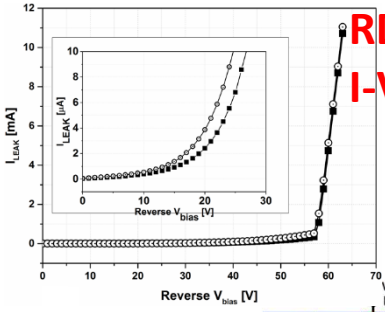




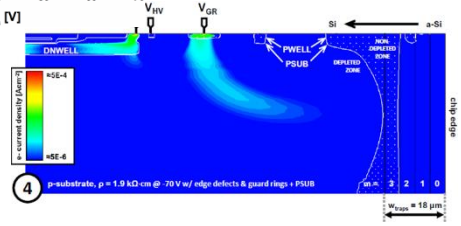
2017 | 2018 | 2019 | 2020 | 2021

RD50-MPW1

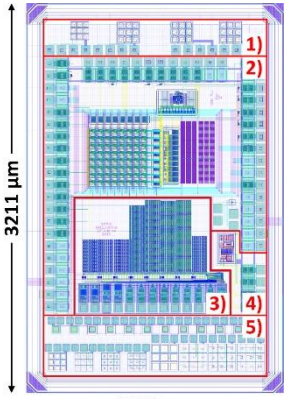
I-V



TCAD

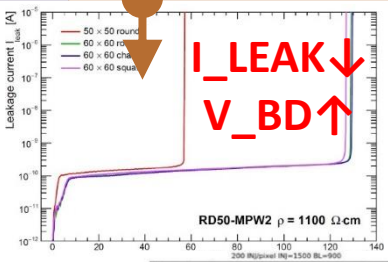


RD50-MPW2

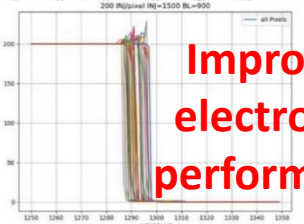


I_LEAK↓

V_BD↑



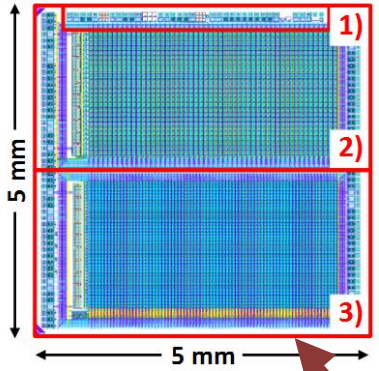
Improved electronics performance



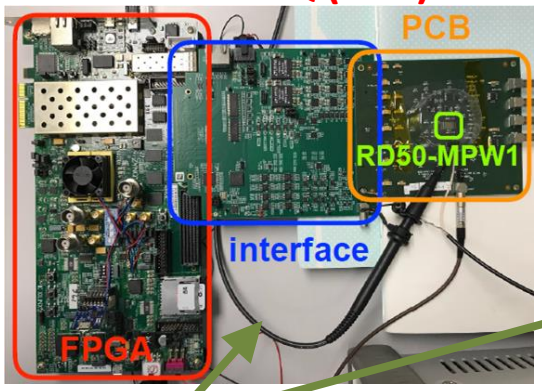
S-curves for all pixels with threshold variation. Trim DAC values adjusted. Injection amplitude 1500 mV.

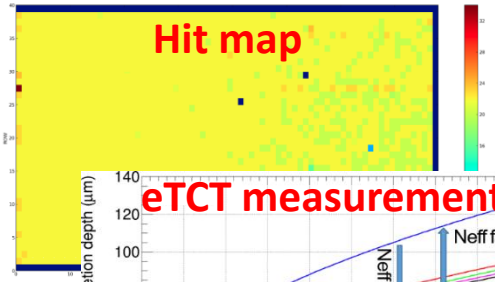
RD50 CMOS timeline

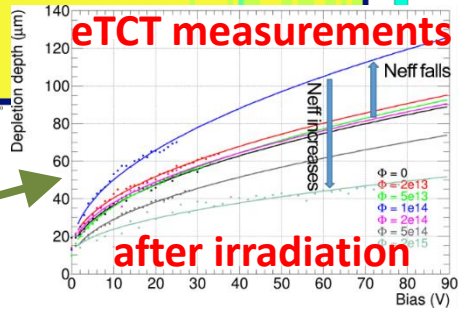
RD50-MPW1



RD50 DAQ (CaR)

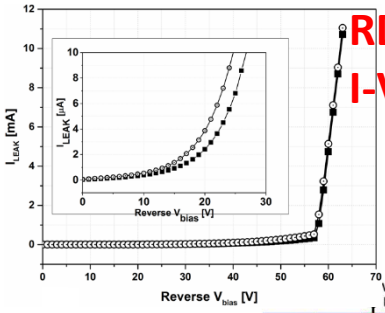




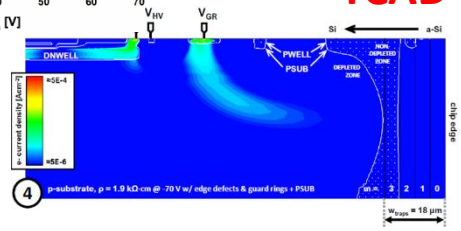


2017 | 2018 | 2019 | 2020 | 2021

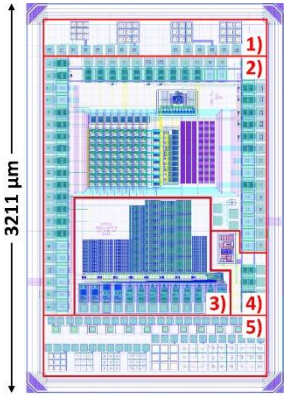
RD50-MPW1
I-V



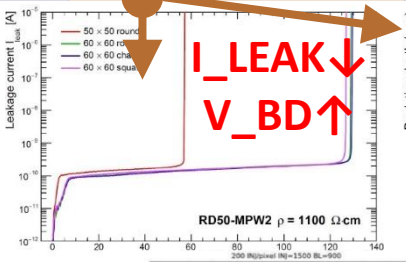
TCAD

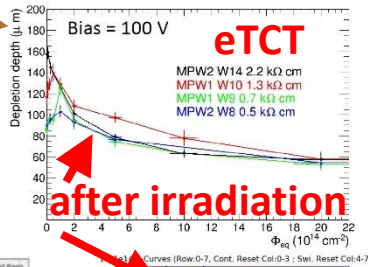


RD50-MPW2

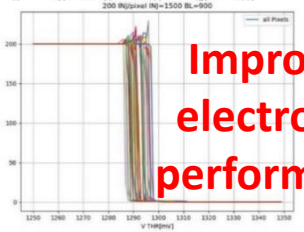


I_LEAK↓
V_BD↑

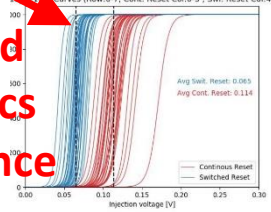




Improved electronics performance



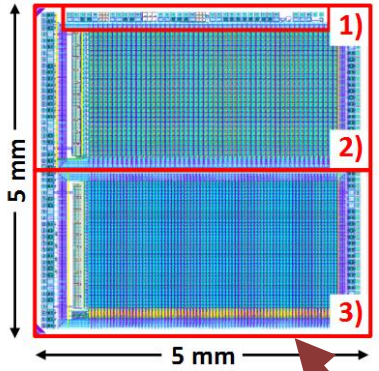
S-curves for all pixels with threshold variation. Trim DAC values adjusted. Injection amplitude 1500 mV.



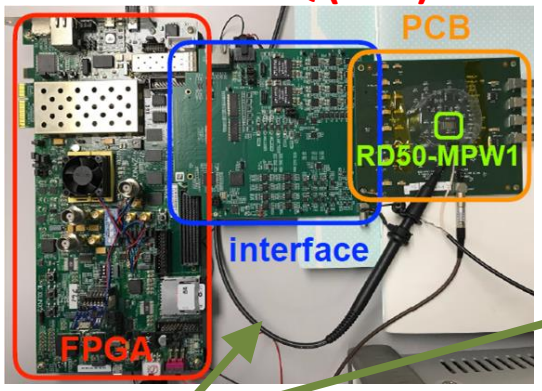
Wafer 13, 1e14N_{eq}

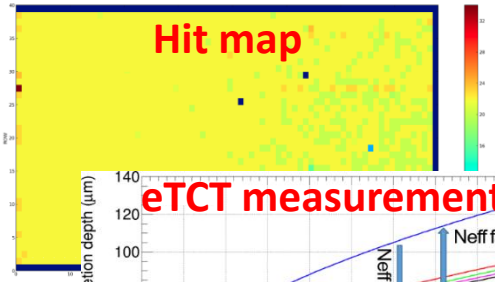
RD50 CMOS timeline

RD50-MPW1

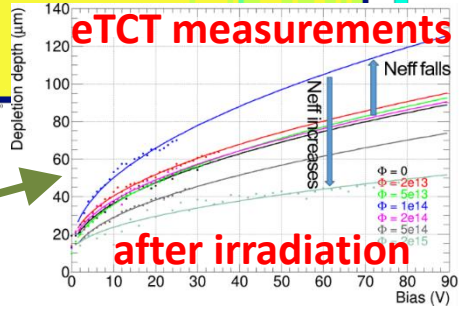


RD50 DAQ (CaR)



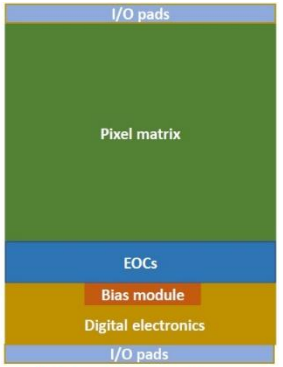


eTCT measurements



after irradiation

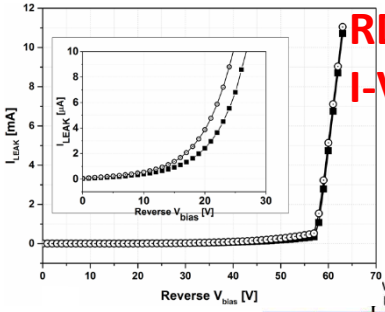
RD50-MPW3



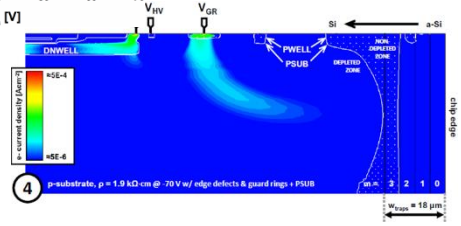
*digital electronics: CU + serializer + configuration registers (slow control)

2017 | 2018 | 2019 | 2020 | 2021

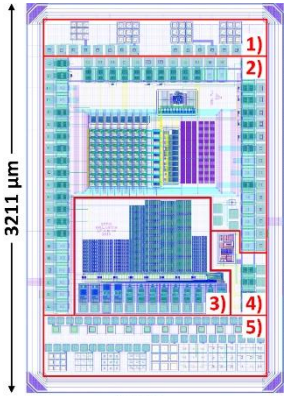
RD50-MPW1 I-V



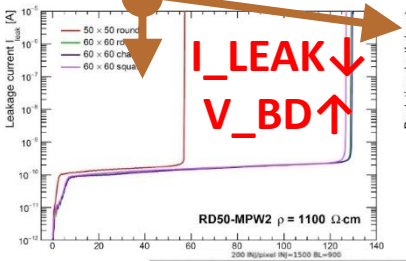
TCAD



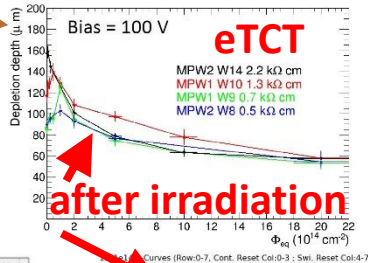
RD50-MPW2



I_LEAK↓ V_BD↑

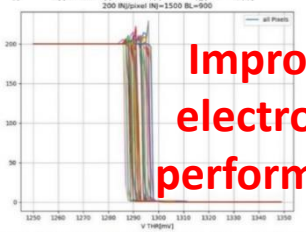


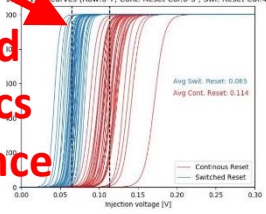
eTCT



after irradiation

Improved electronics performance





S-curves for all pixels with threshold variation. Trim DAC values adjusted. Injection amplitude 1500 mV.

Wafer 13, 1e14N$_{eq}$

RD50 CMOS – Where are we?

- **After a difficult start, we are now in the right direction**
- **RD50-MPW2 performs very nicely**
  - Despite coronavirus and subsequent lockdowns, we have lots of interesting results
  - We expect to have many more results in the near future
    - Test beam
    - Accurate time resolution measurements
    - SEE and CCE measurements
- **We are doing design work towards our next chip submission (RD50-MPW3)**
  - Matrices of pixels
    - FE-I3 style matrix with highly improved readout electronics, especially those at the periphery to make data taking easier
    - Small sensor diodes matrix – To study new sensor cross-sections
    - Sampling matrix – To further improve sensor time resolution
  - The chip will incorporate all the lessons learned with RD50-MPW1/2
    - Small pixels with analogue and digital readout electronics
    - Methods to optimise I_LEAK and V_BD developed for RD50-MPW2
  - The chip submission will be in Q2 2021 (funding request in Q1 2021)

RD50 CMOS – Milestones

- **RD50 prolongation request – May 2018**
  - **M1:** Characterization of the diodes and readout electronics of unirradiated and irradiated RD50-MPW1 samples (Q4/2018) → **Achieved**
    - **M1.2 (new):** Design and submission of RD50-MPW2 (Q1/2019) → **Achieved**
    - **M1.3 (new):** Characterization of unirradiated and irradiated RD50-MPW2 samples (Q1+Q2/2020) → **Ongoing**
    - **M1.4 (new):** Design and submission of RD50-MPW3 (Q2/2021) → **Ongoing**
  - **M2:** Design and submission for fabrication of RD50-ENGRUN1 (Q4/2018)
  - **M3:** Characterization of unirradiated and irradiated RD50-ENGRUN1 samples (Q3/2019, Q3/2020)
  - **M4:** Characterization of irradiated backside biased RD50-ENGRUN1 samples for operation beyond 10^{16} n_{eq}/cm (Q4/2020)
  - **M5:** Studies of stitching process options (Q4/2021)
  - **M6:** Characterization of unirradiated and irradiated stitched samples (Q4/2022)