37th RD50 Workshop

RD50 project proposal

Passive CMOS submission for sensors and test structures

David-Leon Pohl

20.11.2020

pohl@physik.uni-bonn.de

Reminder

- „Passive“ CMOS sensors profit from CMOS process features:
  - Cost-effective, large-scale sensor production
  - Large 8“ wafer processing (various post-processing capabilities)
  - Many metal layers; deep implants
  - AC coupling capacitors, bias resistor in each channel
  - Field plates (Sinuos talk)
  - Potential integration of RO electronics

- Experience from former pixel sensor submissions:
  - Large sensor tiles (up to 4 x 4 cm^2) using reticle stitching demonstrated (Cedrics talk)
  - Up to 1e16 n_{eq} / cm^2 seems to work (Yannicks talk)
  - Thinning to 100 um in TAIKO process + flip-chip established
  - 205 k€ costs for 12 x 8“ wafer <u>including</u> reticle stitching (recent ATLAS order)

Proposal

- One submission (~ end next year):
  - Start after current submission is characterized
  - Share a reticle (~26 x 32 mm²) for many test structures and (pixel/strip) sensors
  - One thin full-size, RD53 compatible pixel-sensor
  - Using LFoundry process: 150 - 200 k€
  - Backside process, TAIKO thinning with IBS
  - Bonn can support design process, anybody wants to join?

- What could we do? (just some ideas, feasibility to be checked...)
  - Thinning to different thicknesses in TAIKO process (50 um - 100 um)
  - Inter-channel isolation techniques (field plates, narrow p-stop), to reduce pixel capacitance
  - Testing at extreme fluences >> 1e16 n_{eq} / cm²
  - Optimization of guard ring structures for higher break down / slim edge
  - Small 25 x 25 um² pixels (with fan-out using metal layers for RO chip compatibility)
  - Sub-pixel coding
  - Produce „reference“ diodes for NIEL measurements
  - Vary the wafer material (resistivity, CZ/FZ)
  - ...