Towards a Mighty Tracker

Uli Uwer, Matt Needham, Chris Parkes

Mighty Tracker: Design studies for the downstream silicon tracker in Upgrade Ib and II

Preliminary Specification of a HV-CMOS Pixel Chip for LHCb Upgrade II

In preparation

Slides based on Matt Needham’s draft
Today

**Middle-Inner Tracker, MIT, Mighty**

- Combined project incorporating **Scintilating Fibres & CMOS Silicon**

Potentially strong synergy on CMOS with UT, where studies are starting

Chris Parkes, March 2020
Tracking

 LG + Vadym Denysenko, Irene Cortinovis (Zurich), Zakariya Aliouche (Manchester), Thomas Ackernley (Liverpool) Yunlong Li, Alessandro Scarabotto, Laurent Dufour (CERN), MN,CP

• Design based on simplified simulation studies of tracking
  (Fibre geometry to give MCHits, smear to simulate pixel resolution)

  • Join the dots studies to inform choice of pixel size

  • Momentum resolution for high p tracks

  • Track matching

  • Forward like tracking (Vadym Denysenko)

A lot to be done and a lot of room for contributions but already clear first impressions

Inner tracker in Ib

• ghost rejection and momentum resolution at high p gains

• Finding tracks in mighty tracker simplified by small pixels
  • Good precision in y, which is non-bending plane
  • Promising studies of upstream/downstream matching (UT design critical also)
    • Do not anticipate need for timing

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• **Full simulation studies underway**
  – DD4HEP
  – will facilitate radiation/interaction rate studies
  – Tracking studies
**Layout: current baseline**

- **Inner Tracker (LS3, Upgrade Ib)**
  - Rebuild two inner modules per layer in SciFi
  - CMOS Silicon ~ 4m²
- **Outer Tracker (LS4, Upgrade II)**
  - Entirely new Sci-Fi
  - CMOS Silicon ~ 18m², reusing 4m² of Upgrade Ib
  - Smaller Si would rely on improvements in SciFi rad. hardness

**Size drivers:**
- **Inner Tracker Upgrade 1b**: ghost rate + minimal modification to SciFi
  - Approx. 50% tracks pass through IT
- **Middle Tracker Upgrade II**: Radiation damage and occupancies in SciFi at Upgrade I level

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**Six layers of CMOS assumed**
- Pixels measure x and y
  - don’t need 12 layers
  - Need to account for inactive regions
  - X-stations of Sci-Fi

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**IT**
- Area per layer = 6 lots of 20x54 cm = 0.7 m² (minus beam hole)
- Total Area = 6 layers of 0.7 m² = 3.9 m² (minus beam hole)

**IT+MT**
- Area per layer = 28 lots of 20x54 cm = 3.0 m² (minus beam hole)
- Total Area = 6 layers of 0.7 m² = 18.1 m² (minus beam hole)
• Build Upgrade Ib Silicon at correct dimensions for inner Sci-Fi modules
  • May reduce CMOS rework later, SciFi will need rebuilding for U2 anyway
  • May reduce number of SciFi modules to be rebuilt in Ulb?
  • Build four layers not six of CMOS, Ulb area fairly similar
SciFi is limiting factor at Upgrade I in track multiplicity coverage

IT will assist significantly

Extending IT in UIb would allow centrality 0 to be reached.

**Same CMOS areas as prev. alternative**

- BUT next SciFi modules must also be rebuilt
  - Hence significant increase in effort required

<table>
<thead>
<tr>
<th>Detector Configuration</th>
<th>Upgrade Ib</th>
<th>Upgrade II</th>
</tr>
</thead>
<tbody>
<tr>
<td>SciFi only</td>
<td>3.2 ± 0.2</td>
<td>18.4 ± 0.4</td>
</tr>
<tr>
<td>SciFi with IT</td>
<td>1.4 ± 0.1 (×1/2.3)</td>
<td>6.8 ± 0.3 (×1/2.7)</td>
</tr>
<tr>
<td>SciFi with extended-X IT</td>
<td>0.8± 0.1 (×1/4)</td>
<td>4.2 ± 0.2 (×1/4.4)</td>
</tr>
</tbody>
</table>
Radiation dose

- IT, Run 4-6 377 fb\(^{-1}\), 3\(\times\)10\(^{14}\) 1 MeV neq/cm\(^2\)
- MT, Run 5-6 350 fb\(^{-1}\), 2\(\times\)10\(^{13}\) 1 MeV neq/cm\(^2\)

Well within demonstrated capabilities of suggested HV-CMOS sensor technology

[UT is one order of magnitude higher]

- SciFi radiation dose in U2 for fibres kept at level of Upgrade I by design
  - BUT neutron dose on SiPMs major challenge
  - Improvements in fibre rad. tolerance might allow silicon area to be reduced?
Hybrid module design

- Hybrid modules
- Shortened SciFi Modules
  - Improve tracking in SciFi region (lower occupancy)
  - Minimize material
  - Small overlap with hybrid modules

- Challenge to provide services for silicon with limited space
- Careful integrated design is needed
- Upgrade 1b timescale (TDR/build) means this work needs to start soon
Example module concept

- Si / CF sandwich
  - Embedded pipes
- Si both sides
  - dead-area free module
- Readout runs along module
  - Transition to optical on stave
- Mechanical, Thermal, Services Integration with SciFi Critical
  - Services fit in z-space critical
  - Cooling options Include air cooling, heatpipes
- ALICE ITS closest existing system
- ALICE, ATLAS inspiration
- CEPC Synergy

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HV-CMOS MAPS

Ivan Peric (KIT), Andre Schoening (Heidelberg)
Eva Villela (Liverpool) and others…

- Monolithic Active Pixel Sensor (MAPS)
- Integrated pixel sensor & chip on single piece of silicon
  - Low-cost commercial process
  - e.g. used for mobile phone cameras
  - First radiation hard CMOS tracker at LHC

- Chip based on existing MuPix/ATLASPix
  - “MightyPix” Specification document in preparation

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Depleted CMOS Sensors for LHCb</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip Size</td>
<td>( \sim 2 \text{ cm} \times 2 \text{ cm} )</td>
</tr>
<tr>
<td>Sensor Thickness (( \mu \text{m} ))</td>
<td>200 (ATLASPix3)</td>
</tr>
<tr>
<td>Pixel Size (( \mu \text{m} ))</td>
<td>100 \times 300 (with smaller sizes to be explored)</td>
</tr>
<tr>
<td>Time Resolution (ns)</td>
<td>Must be within 25 ns window</td>
</tr>
<tr>
<td>Inactive area</td>
<td>(&lt; 5%)</td>
</tr>
<tr>
<td>Power Consumption (W/cm²)</td>
<td>0.15</td>
</tr>
<tr>
<td>Data transmission (Gbps)</td>
<td>4 links of 1.28 Gb/s each, multiplexed to 2 and 1 links</td>
</tr>
<tr>
<td>NIEL (TBC)</td>
<td>(3 \times 10^{14} ) (6 \times 10^{14} with safety factor)</td>
</tr>
</tbody>
</table>
### HV-CMOS Chip Timeline (pre- covid-19)

<table>
<thead>
<tr>
<th>Period</th>
<th>Tasks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q1 2020</td>
<td>Specifications document&lt;br&gt;Design work for MPW1 to prototype matrices with a few pixel sizes</td>
</tr>
<tr>
<td>Q2 2020</td>
<td>Submission of MPW1</td>
</tr>
<tr>
<td>Q3 2020</td>
<td>Reception and evaluation of MPW1&lt;br&gt;Design work for MPW2 to prototype a matrix with one pixel size and LHCb compatible readout electronics</td>
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<tr>
<td>Q1 2021</td>
<td>Submission of MPW2</td>
</tr>
<tr>
<td>Q2 2021</td>
<td>Reception and evaluation of MPW2&lt;br&gt;Design work for ENG1 to demonstrate a full reticle size detector</td>
</tr>
<tr>
<td>Q1 2022</td>
<td>Submission of ENG1</td>
</tr>
<tr>
<td>Q2 2022</td>
<td>Reception and evaluation of ENG1&lt;br&gt;Design work for ENG2 (production chip)</td>
</tr>
<tr>
<td>Q3 2022</td>
<td>Evaluation of detector module based on ENG1</td>
</tr>
<tr>
<td>Q1 2023</td>
<td>Submission of ENG2</td>
</tr>
<tr>
<td>Q2 2023</td>
<td>Evaluation in full detector system of ENG2</td>
</tr>
<tr>
<td>Q4 2023</td>
<td>Production readiness based on ENG2</td>
</tr>
</tbody>
</table>

- Initial submission to explore alternative pixel sizes
- Time-walk is likely most challenging specification
- Compatibility with LHCb readout scheme in specification (thanks to Ken Wylie)
- Multiple sites setting up / planning to undertake chip testing
Electronics: CMOS Data rates

Important input to RTA and to project costing.
First numbers on rates/link requirements

>25 bits will be required per hit, one hit per interaction

- 9 bits are needed to timestamp the pixel (same as in VELOPix)
- 13 bits ($2^{13} = 8192$) are needed to encode the pixel address
- Parity bits will be required for error detection, here 4 bits are assumed.

**UIb conditions:** 70 Gb/s per layer
**UII conditions:** 415 Gb/s per layer

Preliminary – bits/hit underestimated, may wish to go closer than SciFi to beam
Number of LpGBTx, pcie40 also estimated

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SciFi Region

- Major challenge is radiation damage to fibres & SiPMs
  - Fibres: Ionising dose leads to loss of transparency
    - Current design assuming current fibres
    - NOL fibres – potentially faster and higher light yield
  - SiPMs: neutron fluence leads to increased dark count rate
    - Controls: cryogenic cooling, additional shielding, shaper time-constant
Summary

• Integrated SciFi and CMOS technologies in **single project**
• Initial stage Upgrade Ib
  – 2 SciFi modules/layer, 4m² CMOS
• Full Upgrade II modification
  – New SciFi and 18m² CMOS
• First rad. hard large scale CMOS tracker in HEP
• Neutron fluence major challenge for SciFi SiPMs
• Interested ?
  – Email list: LHCb-mighty-tracker@cern.ch
  – Meetings: Wednesday at 10:00 CET, bi-weekly
  – Wiki: [https://twiki.cern.ch/twiki/bin/viewauth/LHCb/U2Tracking](https://twiki.cern.ch/twiki/bin/viewauth/LHCb/U2Tracking)