Institutes at Feb. LHCb week kick-off meeting – not complete

Towards a Mighty Tracker

Uli Uwer, Matt Needham, Chris Parkes

LHCb-INT-2019-007

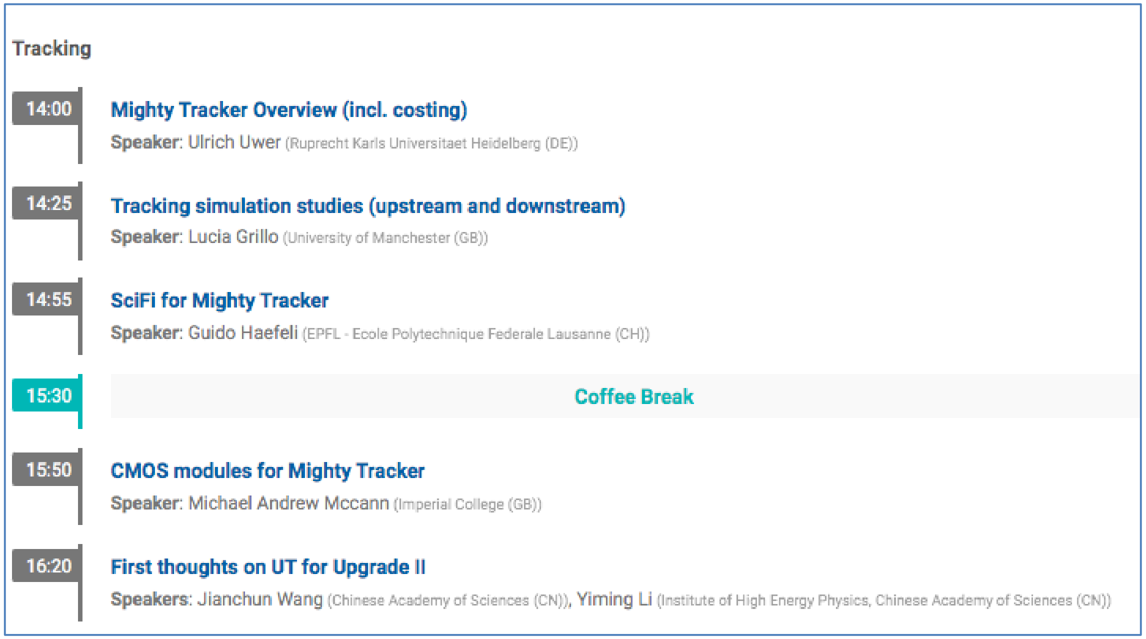
Mighty Tracker: Design studies for the downstream silicon tracker in Upgrade Ib and II

In preparation

Preliminary Specification of a HV-CMOS Pixel Chip for LHCb Upgrade II

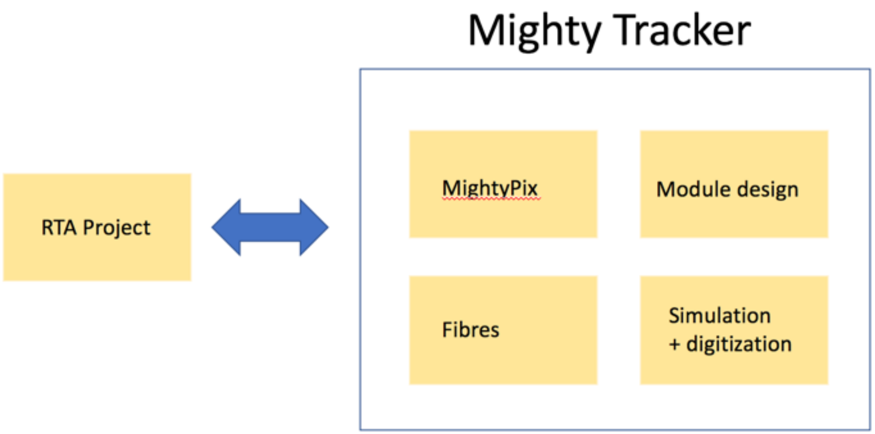
Slides based on Matt Needham's draft

Today



Tracking

14:00	**Mighty Tracker Overview (incl. costing)** Speaker: Ulrich Uwer (Ruprecht Karls Universitaet Heidelberg (DE))
14:25	**Tracking simulation studies (upstream and downstream)** Speaker: Lucia Grillo (University of Manchester (GB))
14:55	**SciFi for Mighty Tracker** Speaker: Guido Haefeli (EPFL - Ecole Polytechnique Federale Lausanne (CH))
15:30	Coffee Break
15:50	**CMOS modules for Mighty Tracker** Speaker: Michael Andrew Mccann (Imperial College (GB))
16:20	**First thoughts on UT for Upgrade II** Speakers: Jianchun Wang (Chinese Academy of Sciences (CN)), Yiming Li (Institute of High Energy Physics, Chinese Academy of Sciences (CN))



- Middle-Inner Tracker, MIT, Mighty
  © Fred Blanc
  - Combined project incorporating **Scintilating Fibres & CMOS Silicon**

Potentially strong synergy on CMOS with UT, where studies are starting

Tracking

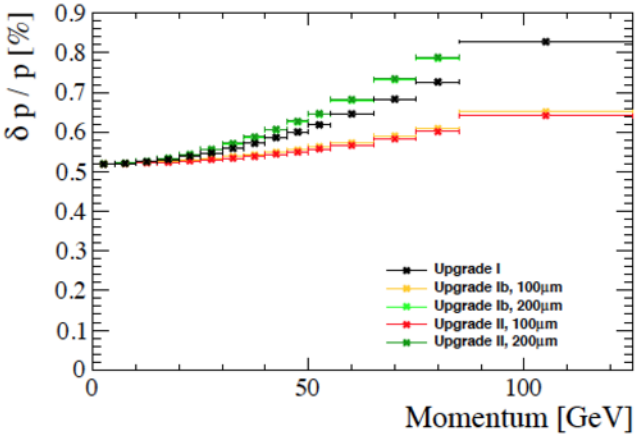
See talk of Lucia Grillo

LG + Vadym Denysenko, Irene Cortinovis (Zurich), Zakariya Aliouche (Manchester), Thomas Ackernley (Liverpool)
Yunlong Li, Alessandro Scarabotto, Laurent Dufour (CERN), MN,CP

- **Design based on simplified simulation studies of tracking**

  (Fibre geometry to give MCHits, smear to simulate pixel resolution)

  - Join the dots studies to inform choice of pixel size
  - Momentum resolution for high p tracks
  - Track matching
  - Forward like tracking (Vadym Denysenko)



A lot to be done and a lot of room for contributions but already clear first impressions

Inner tracker in Ib

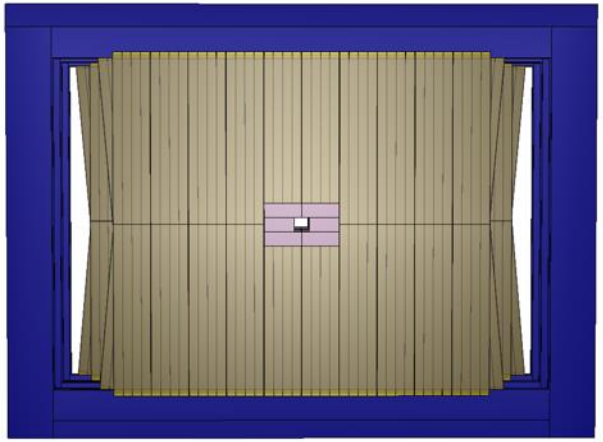
- ghost rejection and momentum resolution at high p gains

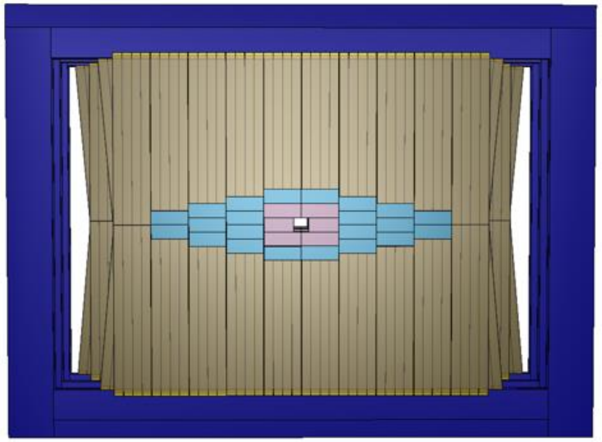
- Finding tracks in mighty tracker simplified by small pixels
  - Good precision in y, which is non-bending plane
  - Promising studies of upstream/downstream matching (UT design critical also)
    - Do not anticipate need for timing

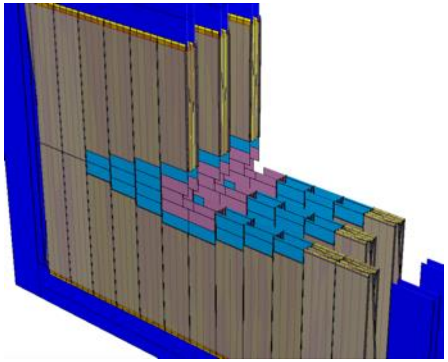
Simulation

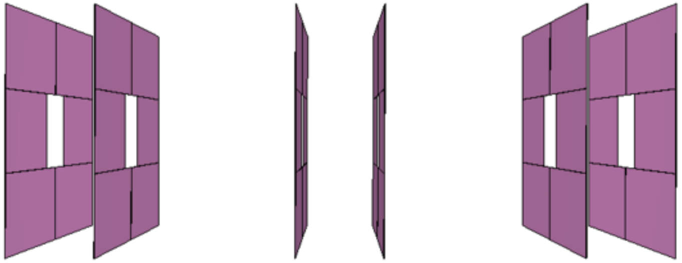
Tai-Hua Lin (Imperial)
Earlier work Donal Murray, Chris Burr, Jeff Koppanyi

- Full simulation studies underway
  - DD4HEP
  - will facilitate radiation/interaction rate studies
  - Tracking studies

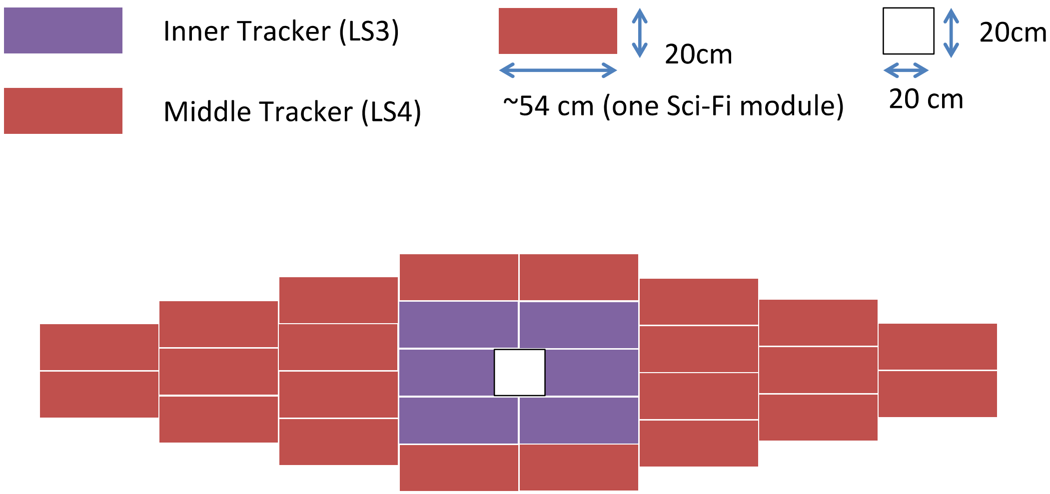








Layout: current baseline



IT
Area per layer = 6 lots of 20x54 cm = 0.7 m^2 (minus beam hole)
Total Area = 6 layers of 0.7 m^2 = 3.9 m^2 (minus beam hole)

IT+MT
Area per layer = 28 lots of 20x54 cm = 3.0 m^2 (minus beam hole)
Total Area = 6 layers of 0.7 m^2 = 18.1 m^2 (minus beam hole)

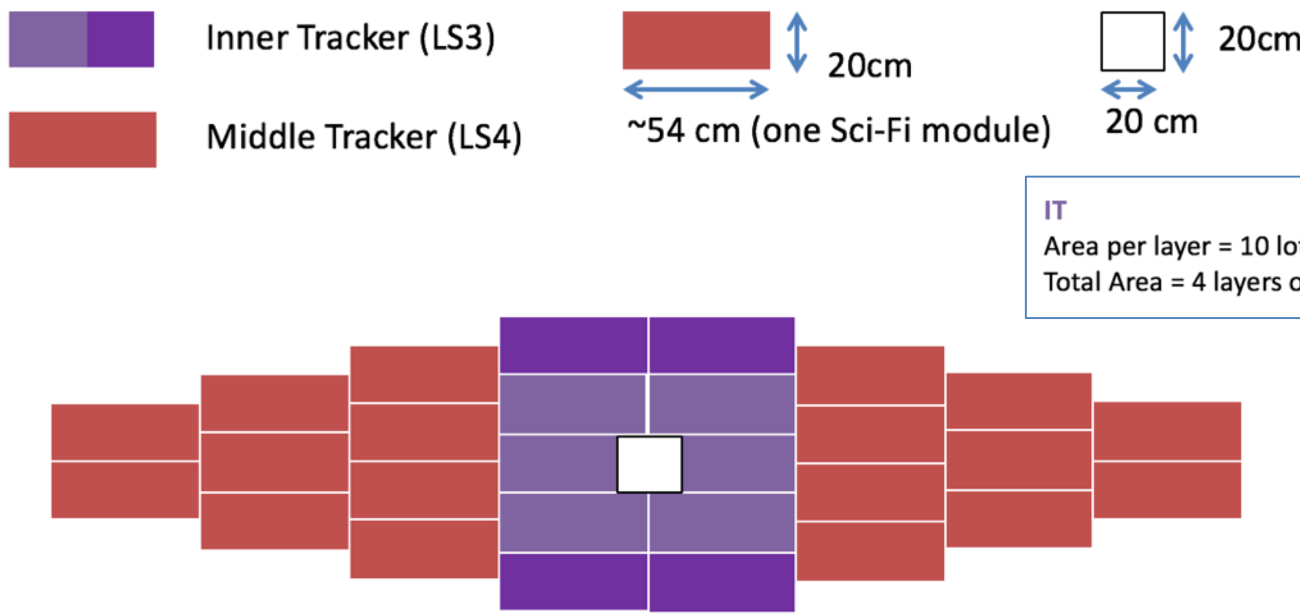
Six layers of CMOS assumed
- Pixels measure x and y
  - don't need 12 layers
  - Need to account for inactive regions
  - X-stations of Sci-Fi

- Inner Tracker (LS3, Upgrade Ib)
  - Rebuild two inner modules per layer in SciFi
  - CMOS Silicon ~ 4m^2
- Outer Tracker (LS4, Upgrade II)
  - Entirely new Sci-Fi
  - CMOS Silicon ~ **18m^2**, reusing 4m^2 of Upgrade Ib
    - Smaller Si would rely on improvements in SciFi rad. hardness

Size drivers:
- Inner Tracker Upgrade 1b: ghost rate + minimal modification to SciFi
  - Approx. 50% tracks pass through IT
- Middle Tracker Upgrade II: Radiation damage and occupancies in SciFi at Upgrade I level

Layout Alternative – Limiting rework

Uli Uwer

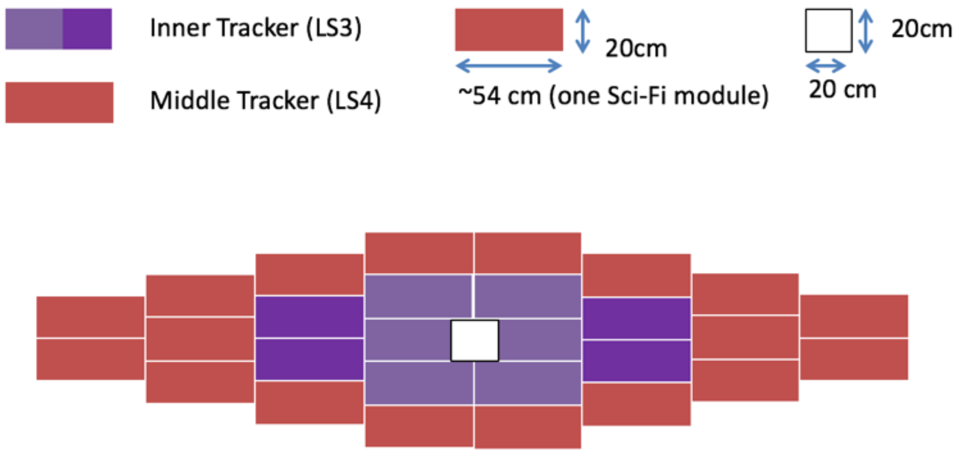


IT
Area per layer = 10 lots of 20x54 cm = 1.1 m^2 (minus beam hole)
Total Area = 4 layers of 1.1 m^2 = 4.3 m^2 (minus beam hole)

- Build Upgrade Ib Silicon at correct dimensions for inner Sci-Fi modules
  - May reduce CMOS rework later, SciFi will need rebuilding for U2 anyway
  - May reduce number of SciFi modules to be rebuilt in UIb ?
  - Build four layers not six of CMOS, UIb area fairly similar

Layout: Alternative – Heavy Ions

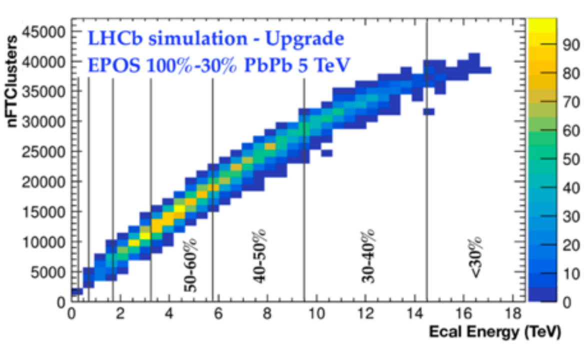
Benjamin Audurier
LHCb-INT-2020-004



IT
Area per layer = 10 lots of 20x54 cm = 1.1 m^2 (minus beam hole)
Total Area = 4 layers of 1.1 m^2 = 4.3 m^2 (minus beam hole)

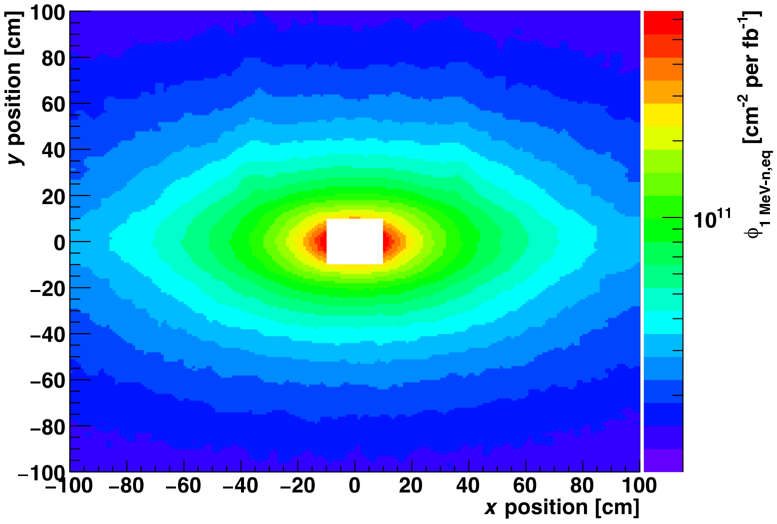
Same CMOS areas as prev. alternative
- BUT next SciFi modules must also be rebuilt
  - Hence significant increase in effort required

- SciFi is limiting factor at Upgrade I in track multiplicity coverage
- IT will assist significantly
  - Extending IT in UIb would allow centrality 0 to be reached.



detector configuration	Upgrade Ib	Upgrade II
SciFi only	3.2 ± 0.2	18.4 ± 0.4
SciFi with IT	1.4 ± 0.1 ($\times 1/2.3$)	6.8 ± 0.3 ($\times 1/2.7$)
SciFi with extended-X IT	0.8 ± 0.1 ($\times 1/4$)	4.2 ± 0.2 ($\times 1/4.4$)

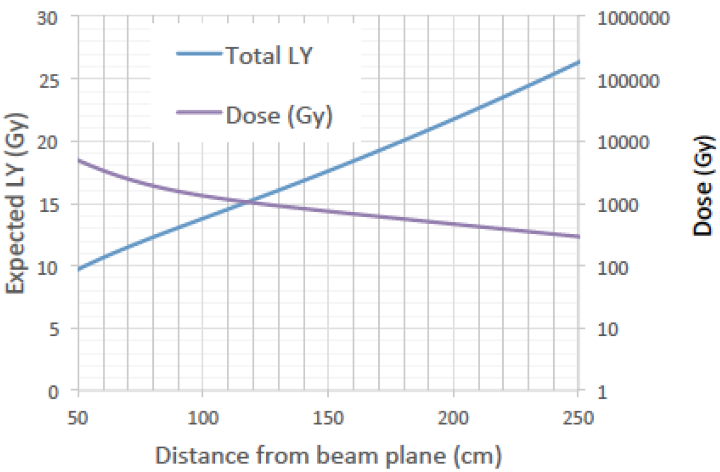
Radiation dose



- IT, Run 4-6 377 fb^{-1}, $3x10^{14}$ 1 MeV neq/cm^2
- MT, Run 5-6 350 fb^{-1}, $2x10^{13}$ 1 MeV neq/cm^2

Well within demonstrated capabilities of suggested HV-CMOS sensor technology

[UT is one order of magnitude higher]

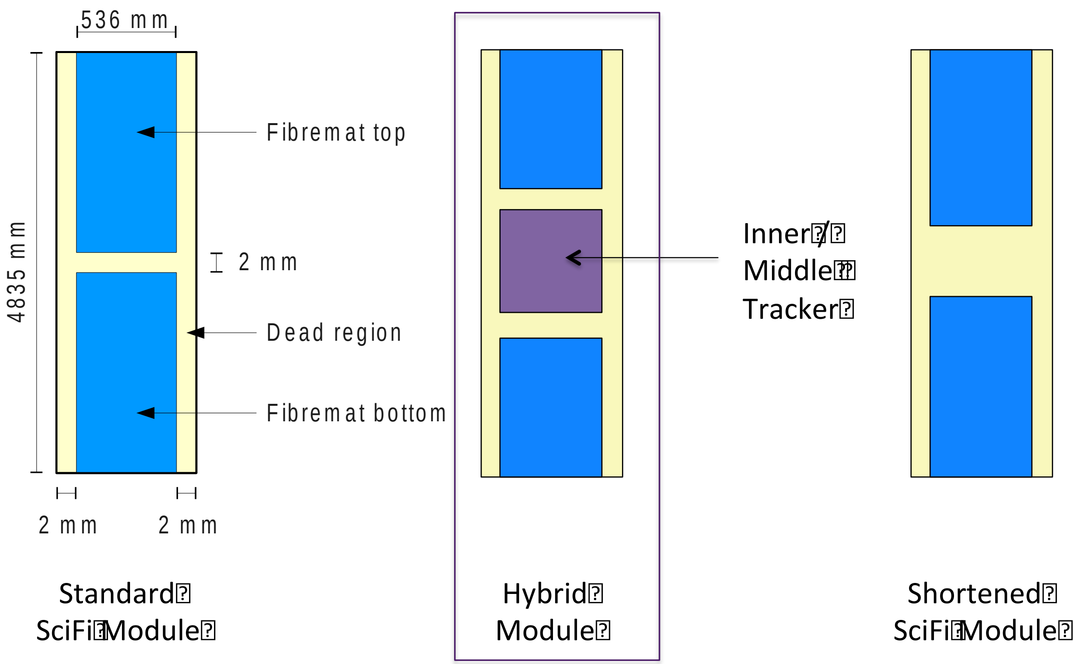


- SciFi radiation dose in U2 for fibres kept at level of Upgrade I by design
  - BUT neutron dose on SiPMs major challenge
  - Improvements in fibre rad. tolerance might allow silicon area to be reduced ?

Hybrid module design

See talk of Mike McCann later in session

- Hybrid modules
- Shortened SciFi Modules
  - Improve tracking in SciFi region (lower occupancy)
  - Minimize material
  - Small overlap with hybrid modules



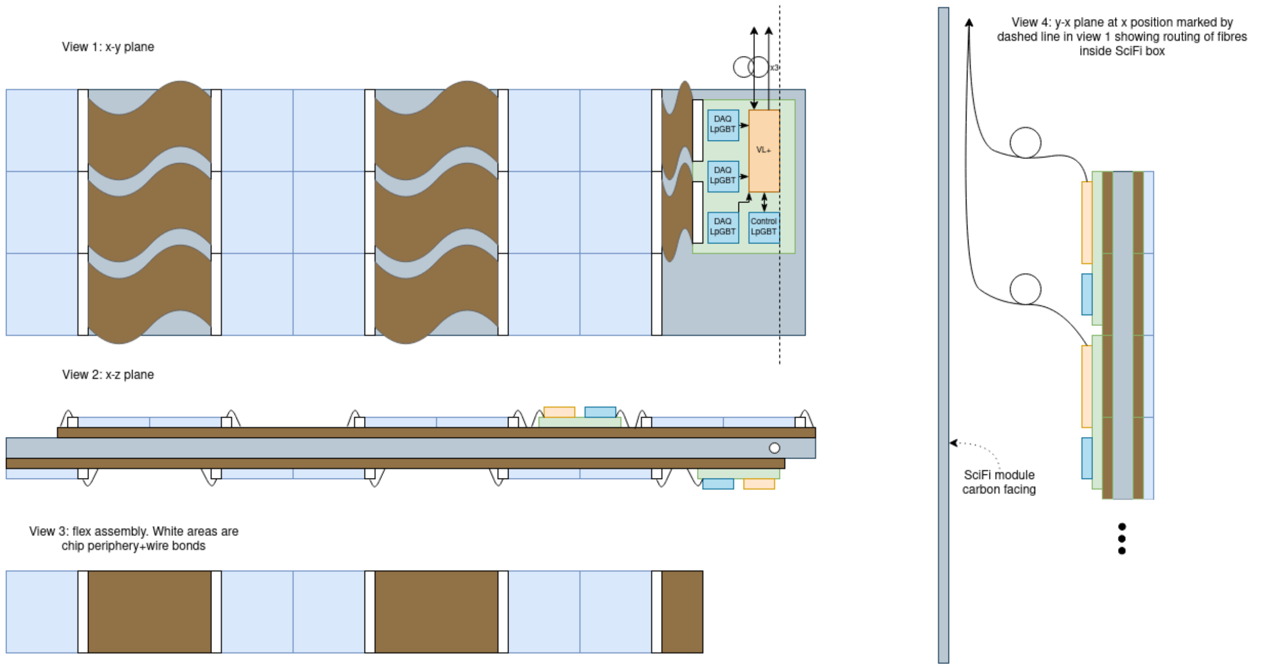
- Challenge to provide services for silicon with limited space
- Careful integrated design is needed
- Upgrade 1b timescale (TDR/build) means this work needs to start soon

CMOS Module layout

Alex Bitadze, Donal Murray (Manchester)
Tim Jones (Liverpool) and others…

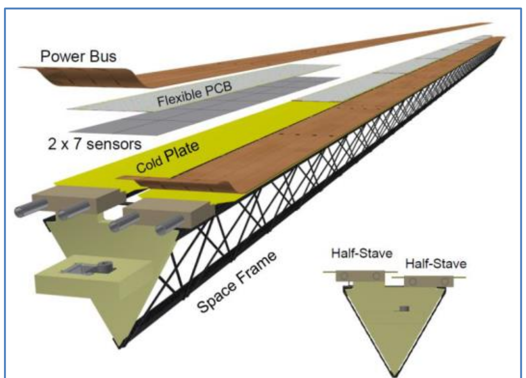
Example module concept

- Si / CF sandwich
  - Embedded pipes
- Si both sides
  - dead-area free module
- Readout runs along module
  - Transition to optical on stave

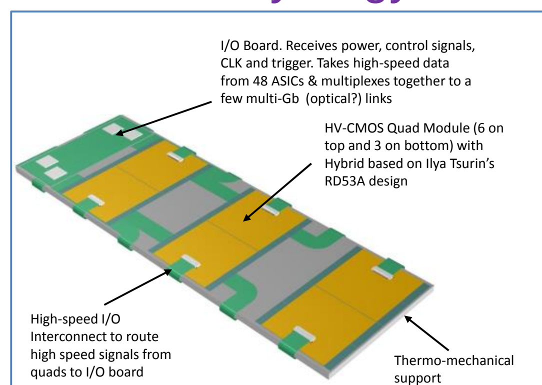


- **Mechanical, Thermal, Services Integration with SciFi Critical**
- Services fit in z-space critical
- Cooling options Include air cooling, heatpipes

- ALICE ITS closest existing system
- ALICE, ATLAS inspiration

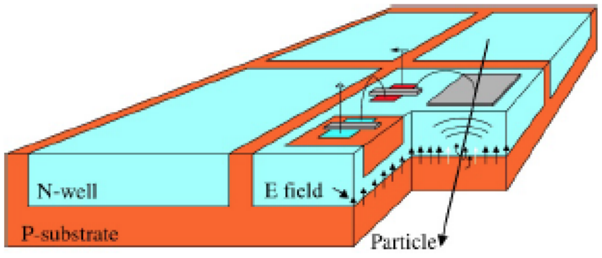


- CEPC Synergy



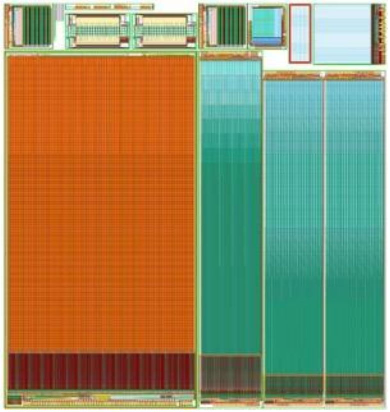
HV-CMOS MAPS

Ivan Peric (KIT), Andre Schoening (Heidelberg)
Eva Villela (Liverpool) and others…



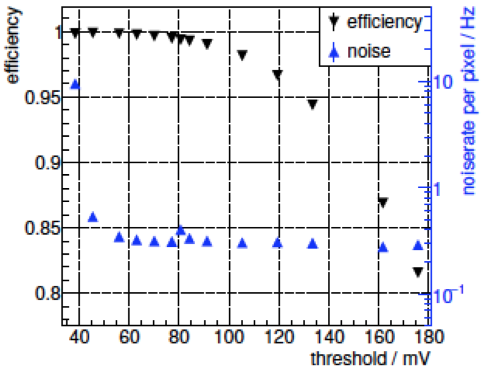
- Monolithic Active Pixel Sensor (MAPS)
- Integrated pixel sensor & chip

on **single** piece of silicon
  - Low-cost commercial process
  - e.g. used for mobile phone cameras
- First radiation hard CMOS tracker at LHC



- Chip based on existing MuPix/ATLASPix
- https://arxiv.org/abs/2002.07253
  - "MightyPix" Specification document in preparation

Parameter	Depleted CMOS Sensors for LHCb
Chip Size	$\sim 2\,\mathrm{cm} \times 2\,\mathrm{cm}$
Sensor Thickness (µm)	200 (ATLASPix3)
Pixel Size (µm)	100×300 (with smaller sizes to be explored)
Time Resolution (ns)	Must be within 25 ns window
Inactive area	$< 5\%$
Power Consumption (W/ cm^2)	0.15
Data transmission (Gbps)	4 links of 1.28 Gb/s each, multiplexed to 2 and 1 links
NIEL (TBC)	3×10^{14} (6×10^{14} with safety factor)



HV-CMOS Chip Timeline (pre- covid-19)

Period	Tasks
Q1 2020	Specifications document
	Design work for **MPW1** to prototype matrices with a few pixel sizes
Q2 2020	Submission of **MPW1**
Q3 2020	Reception and evaluation of **MPW1**
	Design work for **MPW2** to prototype a matrix with one pixel size and LHCb compatible readout electronics
Q1 2021	Submission of **MPW2**
Q2 2021	Reception and evaluation of **MPW2**
	Design work for **ENG1** to demonstrate a full reticle size detector
Q1 2022	Submission of **ENG1**
Q2 2022	Reception and evaluation of **ENG1**
	Design work for **ENG2** (production chip)
Q3 2022	Evaluation of detector module based on **ENG1**
Q1 2023	Submission of **ENG2**
Q2 2023	Evaluation in full detector system of **ENG2**
Q4 2023	Production readiness based on **ENG2**

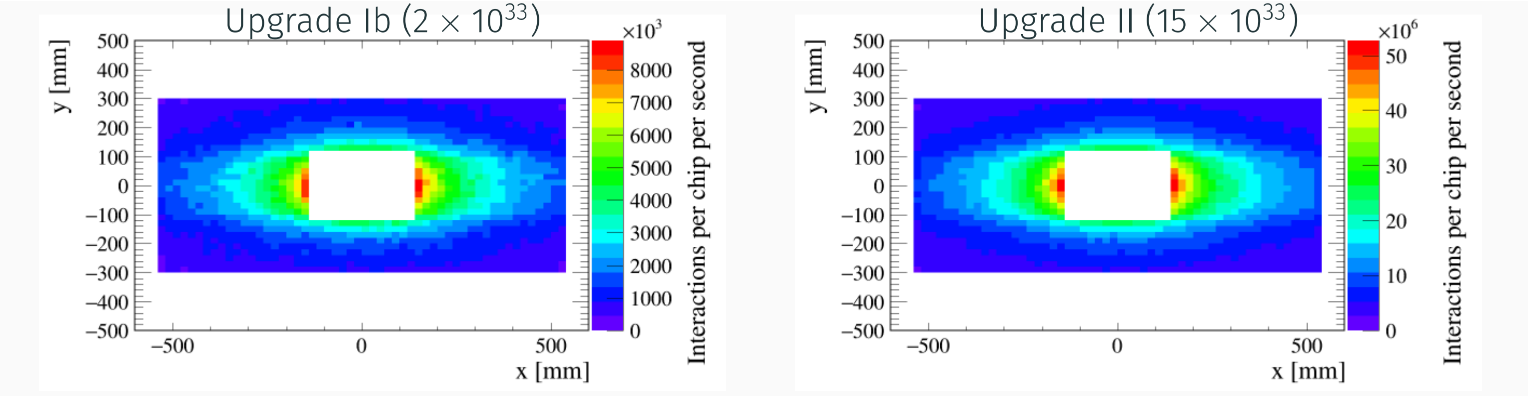
- Initial submission to explore alternative pixel sizes
- Time-walk is likely most challenging specification
- Compatibility with LHCb readout scheme in specification (thanks to Ken Wylie)
- Multiple sites setting up / planning to undertake chip testing

Electronics: CMOS Data rates

Important input to RTA and to project costing.
First numbers on rates/link requirements

>25 bits will be required per hit, one hit per interaction

- 9 bits are needed to timestamp the pixel (same as in VELOPix)
- 13 bits ($2^{13} = 8192$) are needed to encode the pixel address
- Parity bits will be required for error detection, here 4 bits are assumed.



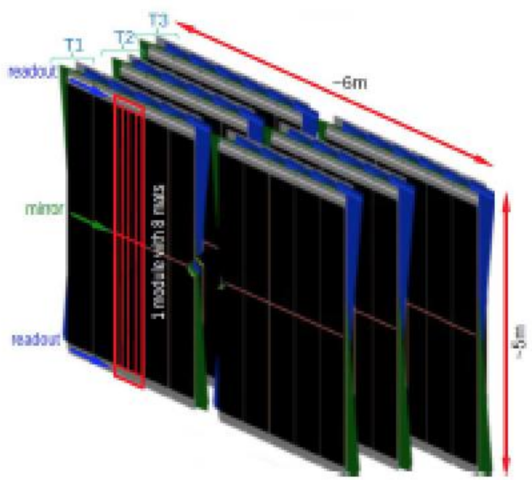
- UIb conditions: 70 Gb/s per layer
- UII conditions: 415 Gb/s per layer

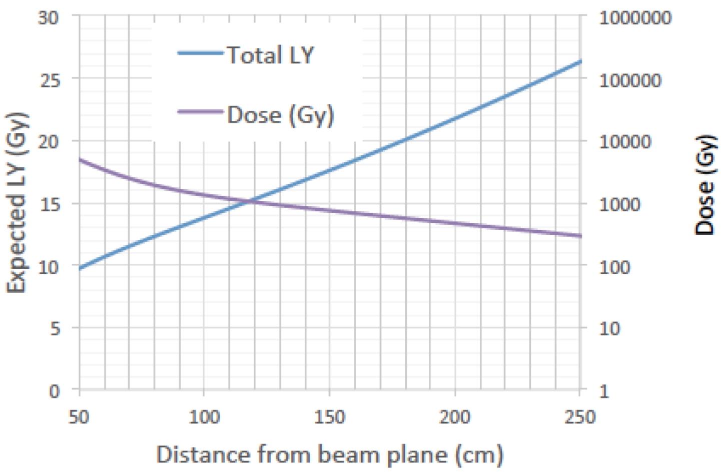
Preliminary – bits/hit underestimated, may wish to go closer than SciFi to beam
Number of LpGBTx, pcie40 also estimated

SciFi Region

See talk of Guido Haefeli

- Major challenge is radiation damage to fibres & SiPMs
  - Fibres: Ionising dose leads to loss of transparency
    - Current design assuming current fibres
    - NOL fibres – potentially faster and higher light yield
  - SiPMs: neutron fluence leads to increased dark count rate
    - Controls: cryogenic cooling, additional shielding, shaper time-constant





Summary

- Integrated SciFi and CMOS technologies in **single project**
- Initial stage Upgrade Ib
  - 2 SciFi modules/layer, 4m^2 CMOS
- Full Upgrade II modification
  - New SciFi and 18m^2 CMOS
- First rad. hard large scale CMOS tracker in HEP
- Neutron fluence major challenge for SciFi SiPMs

- Interested ?
  - Email list: LHCb-mighty-tracker@cern.ch
  - Meetings: Wednesday at 10:00 CET, bi-weekly
  - Wiki: https://twiki.cern.ch/twiki/bin/viewauth/LHCb/U2Tracking

Backup