First Thoughts on UT for Upgrade II

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Introduction

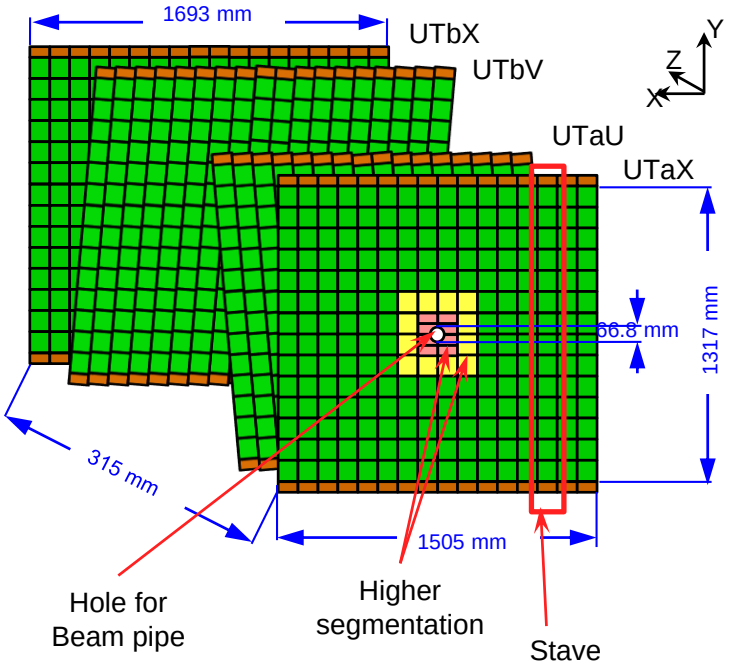
- The UT detector was designed for nominal L = 2×10^{33} $cm^{-2}s^{-1}$, can run up to L~3×10^{33} $cm^{-2}s^{-1}$. At even higher luminosity some ASICs do not have sufficient bandwidth for event data.
- The channel occupancy is kept < 1% at the nominal luminosity.
- The silicon sensors and SALT ASICs will still be efficient after 50 fb^{-1} equivalent radiation damage.

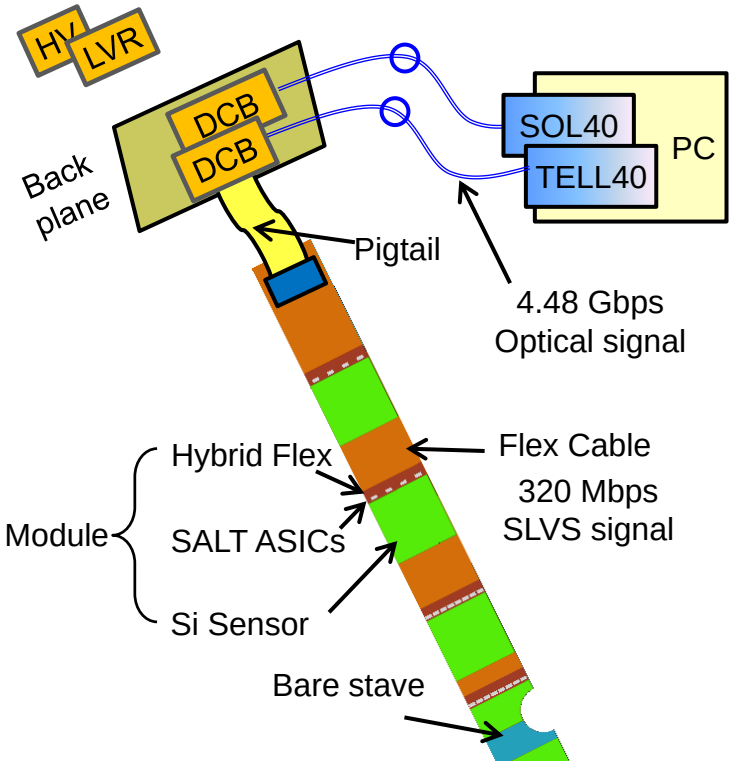
- LHCb will operate at L = 1.5×10^{34} $cm^{-2}s^{-1}$ in Upgrade II, a $\times7.5$ increase, and collect ~250 fb^{-1} data.
- We want to check the occupancy and data rate of the UT system at U2 luminosity, see how it works and whether any part may be kept.
- We also try simple designs and compare a few possibilities: a UT-like detector in the outer area + a CMOS pixel detector at the center, or a full CMOS pixel detector.

UT Detector In Upgrade I

Sensor	A	B	C	D
Pitch (μm)	187.5	93.5	93.5	93.5
Length (mm)	~100	~100	~50	~50
Strips/sensor	512	1024	1024	1024
Numbers	888	48	16	16

- Four different segmentations: A, B, C & D.
- Stave structure, modules on two sides of staves for overlapping, readout at 2 ends of each stave.
- In total 68 staves, 968 sensors, 4192 ASICs.





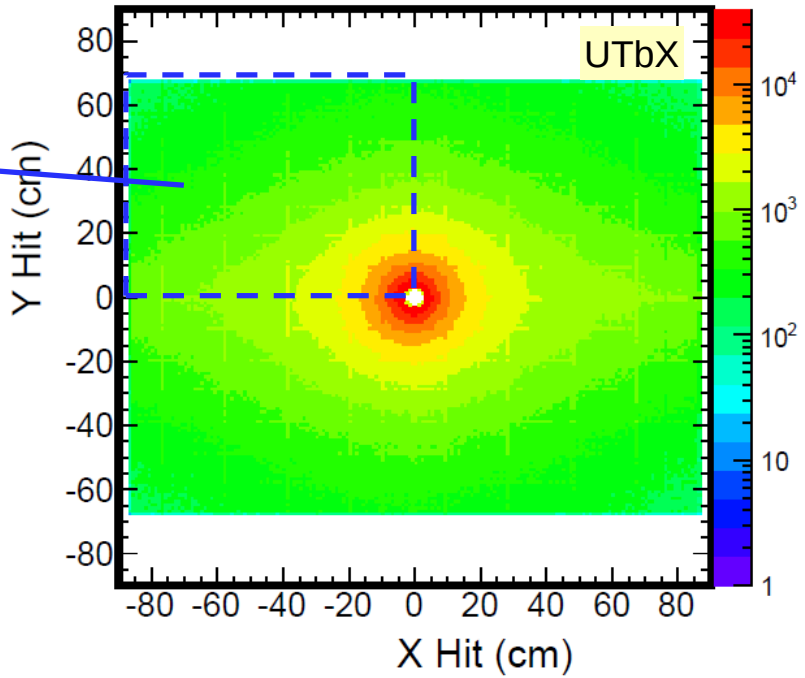
Hit Map and Channel Occupancy

Channel occupancy rate [%]

0.18	0.19	0.19	0.20	0.20	0.21	0.21	0.22	0.22
0.19	0.20	0.20	0.21	0.21	0.22	0.23	0.24	0.24
0.20	0.21	0.22	0.23	0.24	0.25	0.27	0.29	0.30
0.22	0.23	0.24	0.26	0.28	0.30	0.33	0.37	0.40
0.25	0.26	0.28	0.31	0.33	0.38	0.43	0.52	0.59
0.28	0.30	0.33	0.36	0.41	0.47	0.57	0.57	0.74
0.33	0.36	0.38	0.43	0.47	0.56	0.71	0.83	0.75 0.94

From MiniBias events
$L=2\times10^{33}$ $cm^{-2}s^{-1}$

Particle Hit Map [arb unit]

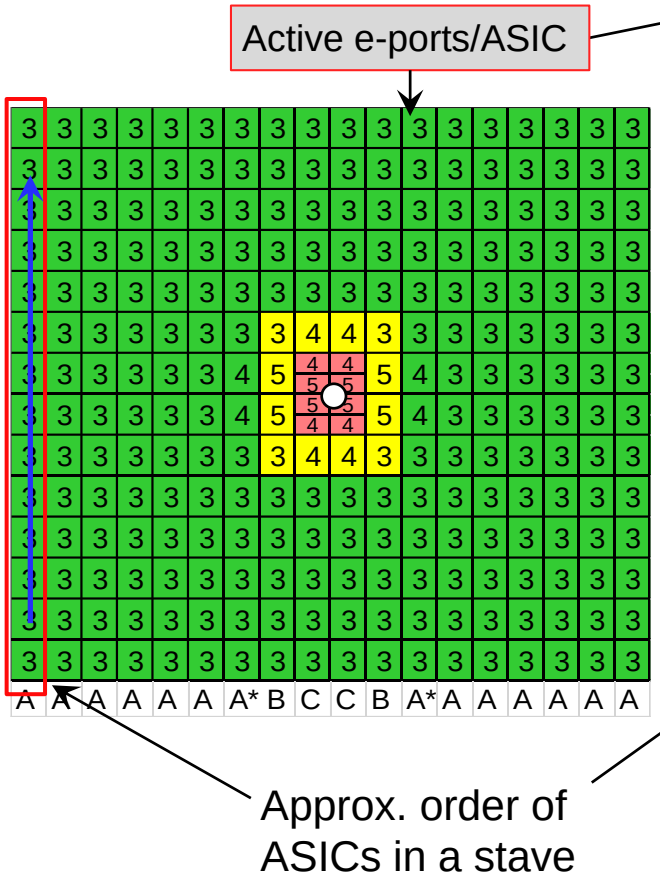


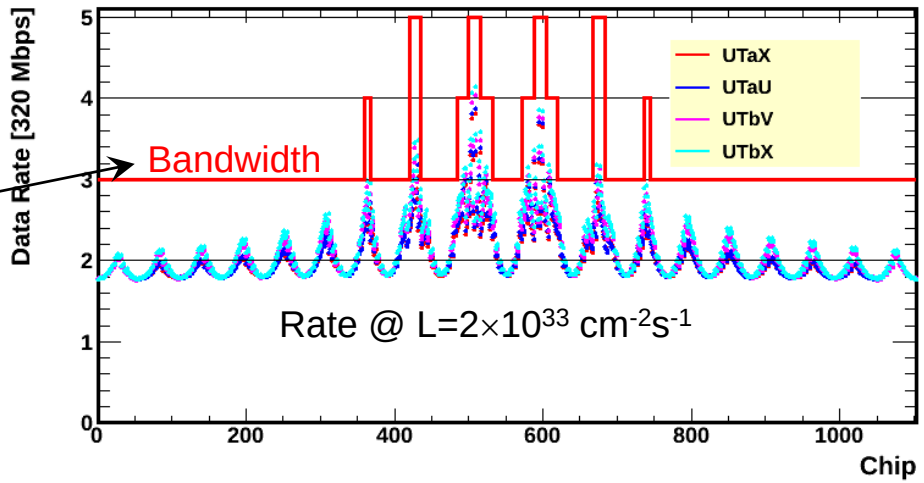
- Noise, spill-overs, and the bunch structure are taken into account.
- With this design, the channel occupancy rate of the inner-most module is ~0.94%. The highest ASIC is ~1.4%.
- The simulation was done in year 2015. The SALT performance was not fully modelled.

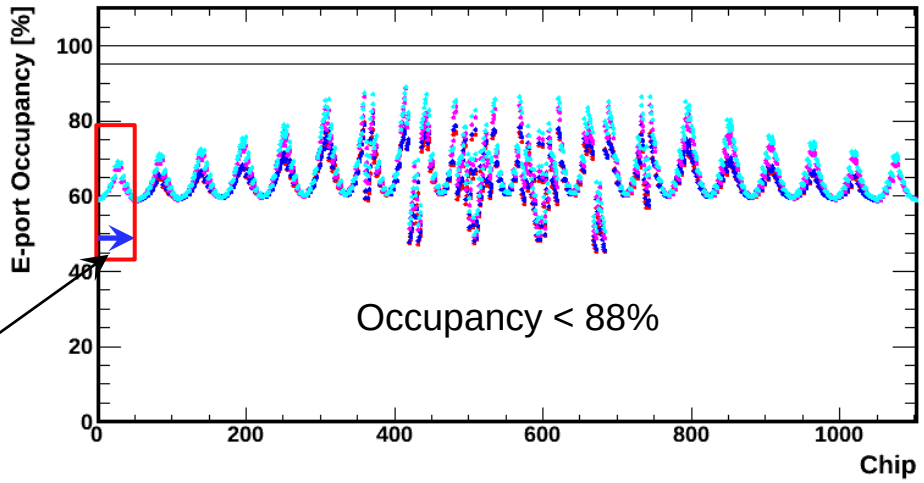
Data Rate and Active E-ports

Work up to L~3×10^{33} $cm^{-2}s^{-1}$

e-port @ 320 Mbps or 8 bits/BX.





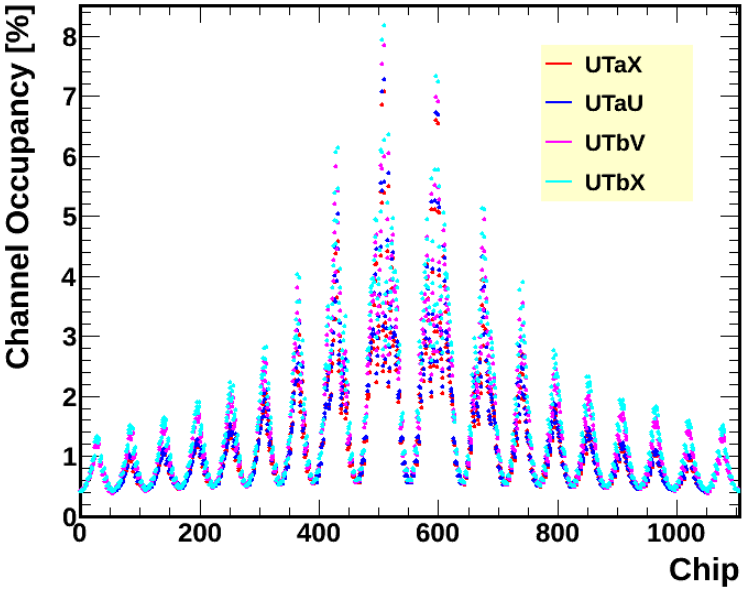


UT @ Upgrade II Luminosity

- We check UT at U2 luminosity L=1.5×10^{34} $cm^{-2}s^{-1}$, basing on the old simulation. New simulation is not ready yet.
- Luminosity increases ×7.5, cluster size 1.45 ⇒ 1.1 & 1.2 for modules of pitch = 187.5 & 93.5 μm respectively.
- Taking into account noise, spill-overs and bunch structure, the occupancy of the inner-most module is ~5.1%. The highest ASIC is ~8.2%.

Channel occupancy [%]

0.42	0.45	0.47	0.49	0.52	0.54	0.57	0.60	0.60
0.46	0.49	0.52	0.56	0.59	0.63	0.68	0.74	0.77
0.53	0.58	0.62	0.68	0.73	0.83	0.89	1.00	1.06
0.64	0.70	0.77	0.86	0.96	1.10	1.26	1.48	1.63
0.78	0.88	0.97	1.13	1.27	1.54	1.81	2.34	2.72
0.96	1.10	1.23	1.45	1.68	2.05	2.63	2.84	3.87
1.28	1.45	1.54	1.81	2.04	2.57	3.42	4.48	3.95 5.13



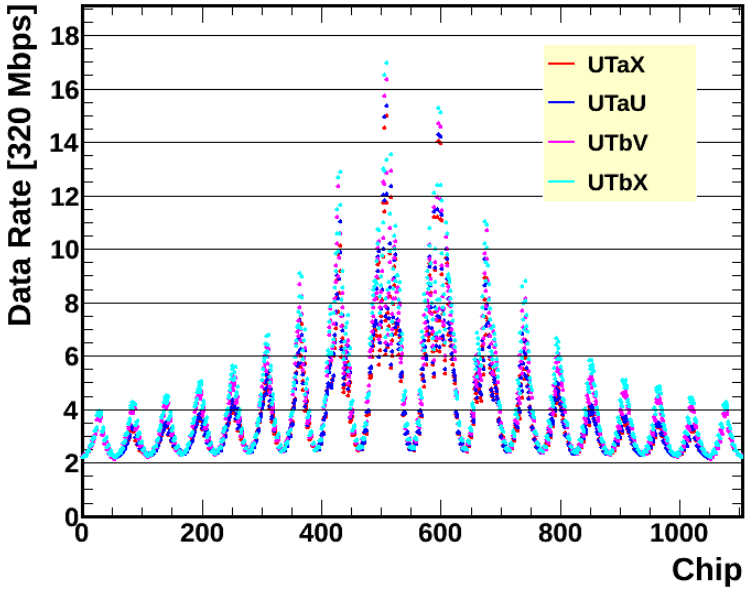
UT Fails To Transfer Data In U2

- Data rate = (12 + 12 <nHits>) × 40 MHz, i.e 1.5 e-ports for header, and 1.5 per hit.
- An ASIC can have up to 6 active e-ports, thus can handle up to <nHits> = 2.8, or 2.2% channel occupancy rate, for e-ports to be < 95% busy.
- Due to constraints of the flex cable, not all e-ports were connected. Each UT stave would have some modules fail this data rate. None of them can be kept in U2.

Number of e-ports needed (<95% busy)

3	3	3	3	3	3	3	3	3
3	3	3	3	3	3	3	4	4
3	3	3	3	3	4	4	4	4
3	3	4	4	4	4	5	5	5
4	4	4	4	5	5	6	7	8
4	4	5	5	6	6	8	8	10
5	5	5	6	6	8	10	14	12 / 18

Not sufficient active e-ports



Scenario I: Type-A Strip + CMOS Pixel

- An outer UT-like strip detector + an inner CMOS pixel detector. Benefit from both the UT and the Mighty Tracker activities.
- We can try a similar stave design to provide mechanical support and cooling.
- By the time of U2, the speed of e-link may be doubled or faster. So are GBTx and PCIe40s. In this exercise we assume that UT electronics can still be used.
- Following is a 1st attempt. The outer detector uses 712 type-A sensors (187.5 μm pitch), which was validated up to ~2×10^{14} n_{eq} cm^{-2} particle fluence.

0.42	0.45	0.47	0.49	0.52	0.54	0.57	0.60	0.60
0.46	0.49	0.52	0.56	0.59	0.63	0.68	0.74	0.77
0.53	0.58	0.62	0.68	0.73	0.83	0.89	1.00	1.06
0.64	0.70	0.77	0.86	0.96	1.10	1.26	1.48	1.63
0.78	0.88	0.97	1.13	1.27	1.54	1.81	2.34	2.72
0.96	1.10	1.23	1.45	1.68	2.05	2.63	2.84	3.87
1.28	1.45	1.54	1.81	2.04	2.57	3.42	4.48	3.95 5.

Type-A strip detector

$\Phi(250\ fb^{-1}) \sim 3\times10^{13}\ n_{eq}\ cm^{-2}$

CMOS pixel detector

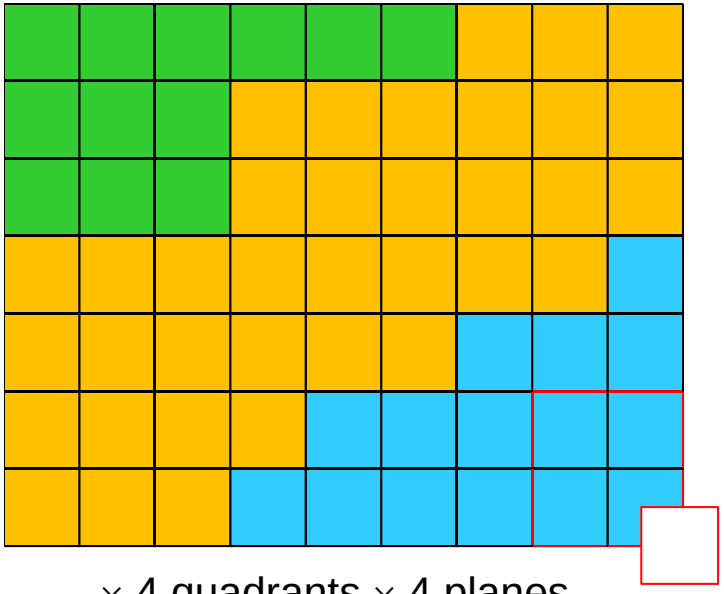
$\Phi(250\ fb^{-1}) \sim (1\text{-}2)\times10^{15}\ n_{eq}\ cm^{-2}$

× 4 quadrants × 4 planes

Possibility ±5 × ±5 cm

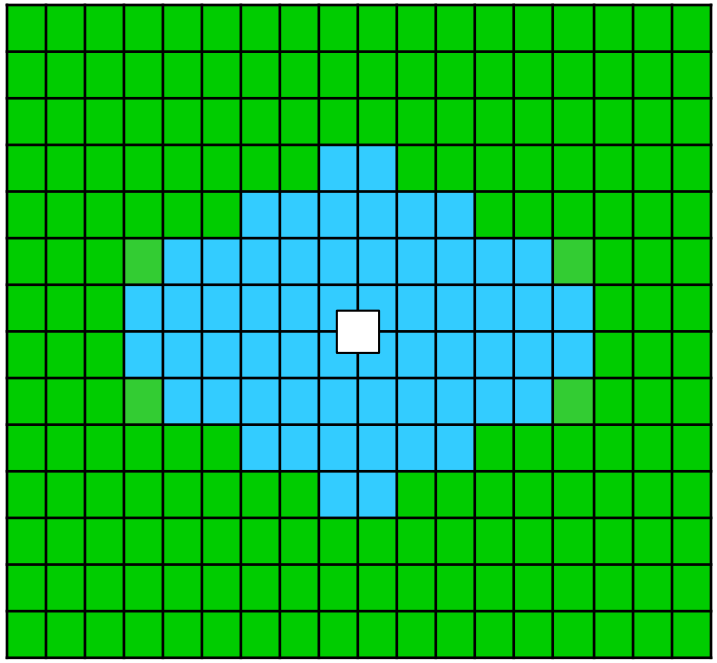
Scenario I: Outer Silicon Strip Detector

- 712 new UT modules (sensor, hybrid, stiffener, SALT). To simplify designs of flex cable, pigtail and backplane, the modules are 4 × 3 e-ports or 4 × 5 e-ports, 168 & 544 modules respectively.
- 68 new bare staves with cooling tubes etc.
- 272 new flex cables, 272 new pigtail cables, 24 new backplanes.
- Readout needs 224 DCBs and 110 TELL40s, all of them can be from UT.
- LV/HV, electronics in SBCs, etc can also be reused.



× 4 quadrants × 4 planes

Scenario I: Inner Detector



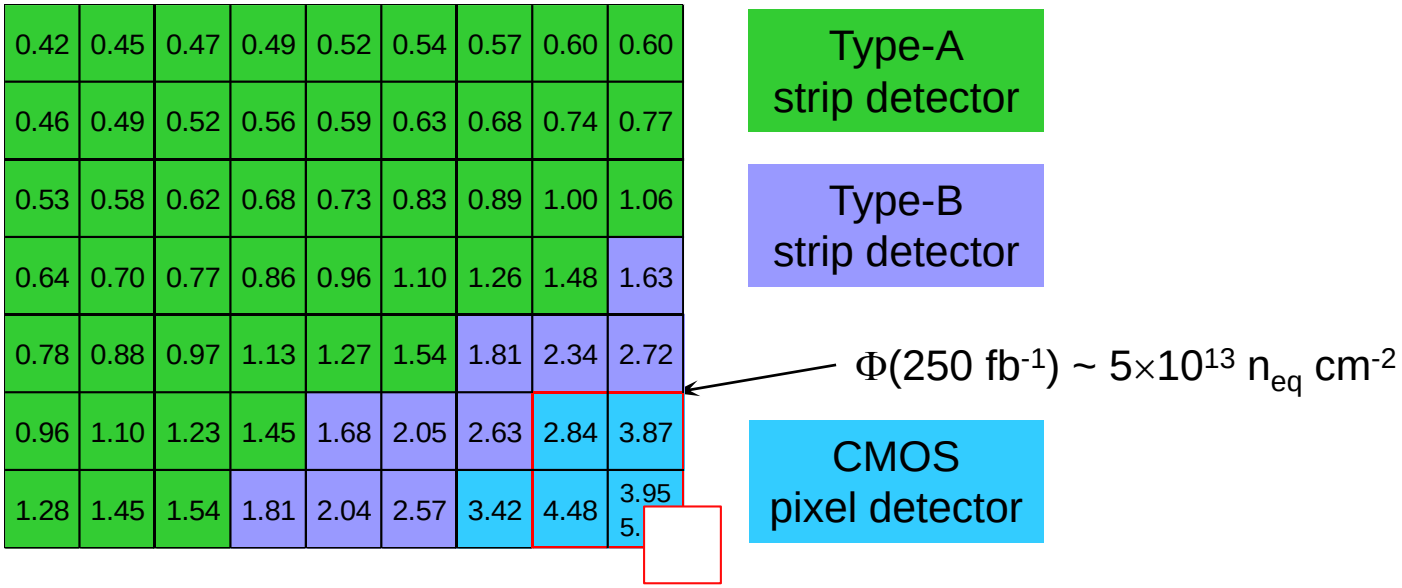
Outer: silicon strip detector

Inner: CMOS silicon pixel detector

- The inner detector is CMOS pixel sensor based. Shape and size of the beam pipe hole are to be evaluated.
- Area ~ $4 \times 60 \times (10 \times 10\ \mathrm{cm}^2) = 2.4\ \mathrm{m}^2$.
- It can share the stave with the outer detector, for both mechanical and cooling.
- The LV / HV and communication also need to be integrated.
- The stave-end electronic chassis will be modified to support two sub-systems.

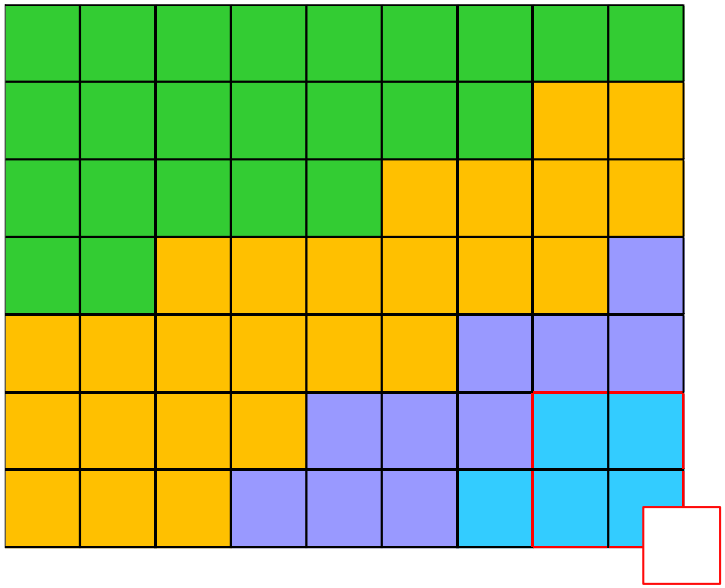
Scenario II: Type-A + Type-B + CMOS

- Use the same stave structure as the UT.
- The outer detector has 712 type-A sensors (pitch = 187.5 μm), 160 type-B sensors (pitch = 93.5 μm). Sensor radiation hardness was validated.
- The inner detector use CMOS pixel sensor, covers ~ 80 × (10×10) cm^2 area.



Scenario II: Continue

- 872 new modules of 4 × 3 e-ports and 4 × 5 e-ports for type-A, 8 × 5 e-ports for type-B, 334, 376 & 160 modules respectively.
- Readout needs 304 DCBs and 144 TELL40s. The current UT can provides at least 240 and 108 respectively.
- Area for the CMOS pixel detector: ~0.8 m^2.



× 4 quadrants × 4 planes

Scenario III

- We can use full CMOS pixel detector option.
- The overall area is about 8.5 m^2. With overlaps it will be ~10% larger. Thus we can use 9.4 m^2 estimation.

Summary

- At U2 luminosity all UT staves, which were designed for U1, have insufficient bandwidth for event data. No stave can be reused. If we include the UT style modules, the current supporting electronics, HV/LV etc can be reused.
- We compared 3 scenarios:
  - Scenario I: An outer silicon strip detector of UT type-A strip sensor + SALT, and an inner CMOS pixel detector.
  - Scenario II: Similar as scenario I, but use UT type-B strip sensors to replace the low intensity outer rim of the CMOS detector.
  - Scenario III: A full CMOS silicon pixel detector.
- Scenario II is favored in budget, but more complicated to build.
- We are working on a more realistic simulation to re-evaluate different scenarios, and plan to have a full U2 detector simulation to validate and optimize the design.
- Other high segmentation detector may also be considered. The CMOS option benefits from the Mighty Tracker activities, and the R&D project at IHEP.