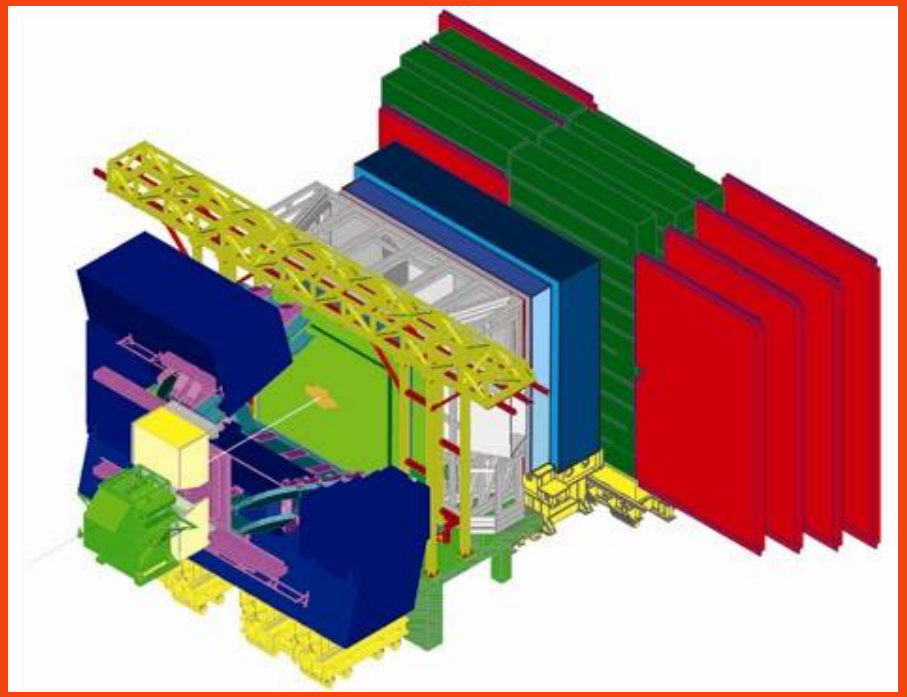


LHCb Muon Detector Upgrade

R-WELL Readout based on VFAT3 and lpGBTx

&

A scheme to reduce uncorrelated events in MWPC – N. Bondar ; Oleg Maev

R-WELL Readout based on VFAT3 and lpGBTx

VFAT3 – Front End

Front-End side main parameters:

- Gain
- Parasitic
- Input (max) rate

Detector Cap. range	9-88 pF
Peaking Times (Tp)	25, 50, 75, 100, ns
Programmable gain	1.25 – 50 (mV/fC)
Noise	~1100e (Tp=100ns, Cd=30pF)

Rate: VFAT3 has been tested up to 1 MHz

	chamber/region	max rate/pad [kHz]	C/2gap[pF]	Nch/2gap
M2R1	12	689	28	1920
M2R2	24	130	56	1904
M3R1	12	463	32	1896
M3R2	24	111	65	1911
M4R1	12	187	37	1944
M4R2	24	51	75	1917
M5R1	12	183	43	1897
M5R2	24	37	84	1922

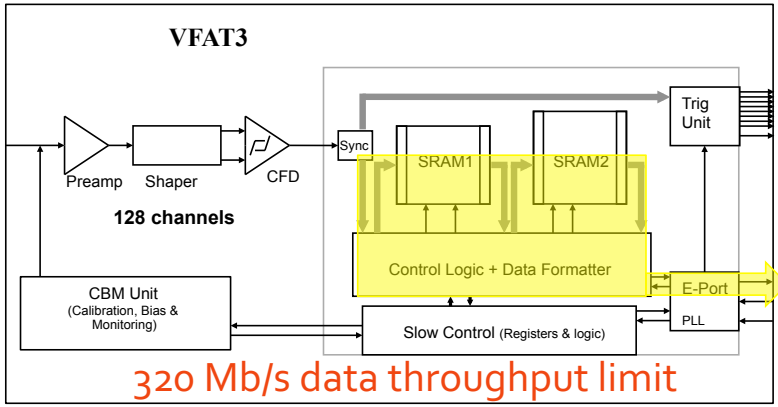
single channel rate and parasitic looks compatible with VFAT input stage

VTAT3 – Back End

Back-End side main parameters:

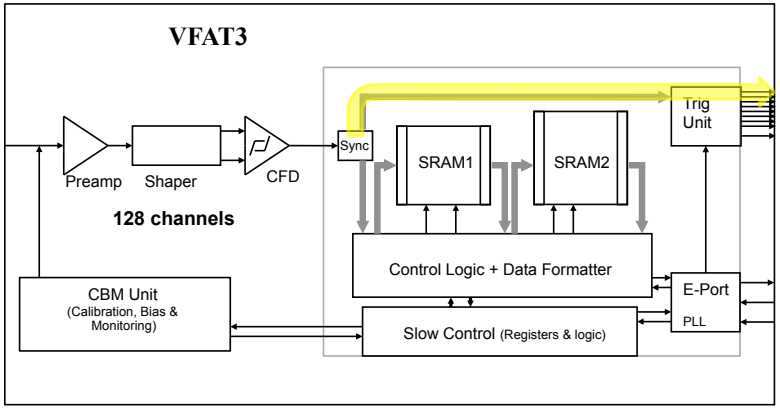
- Bandwidth
- Number of "Concentrator/DAQ" boards
- Number of links

VARIABLE LATENCY PATH



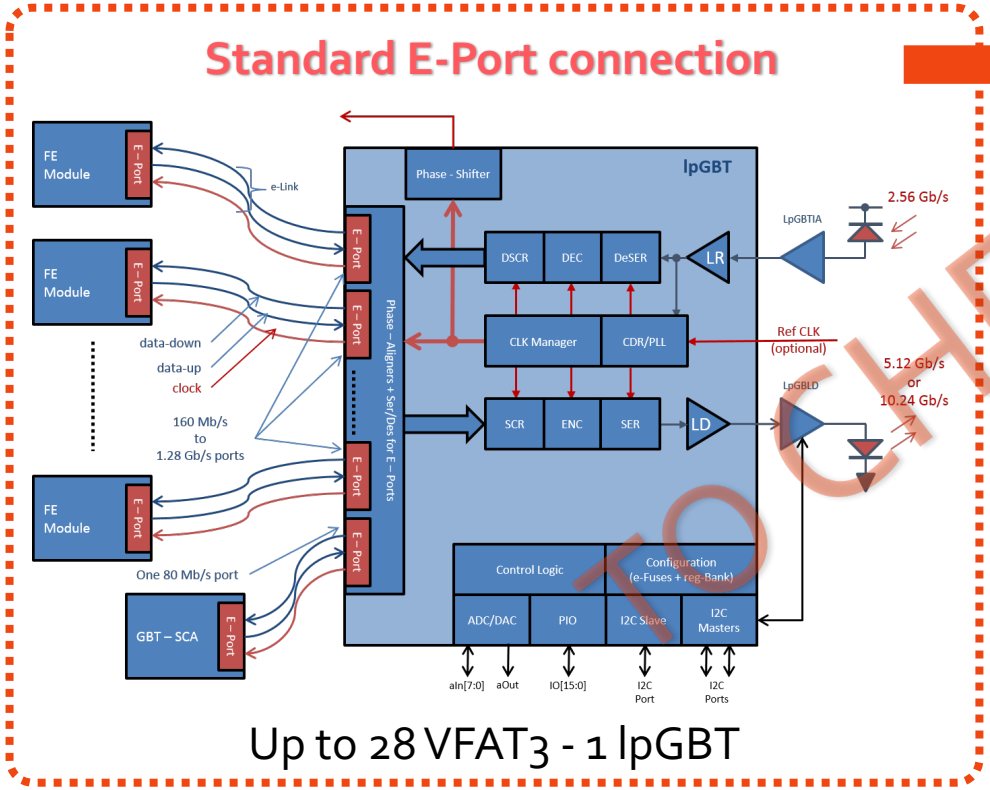
320 Mb/s data throughput limit

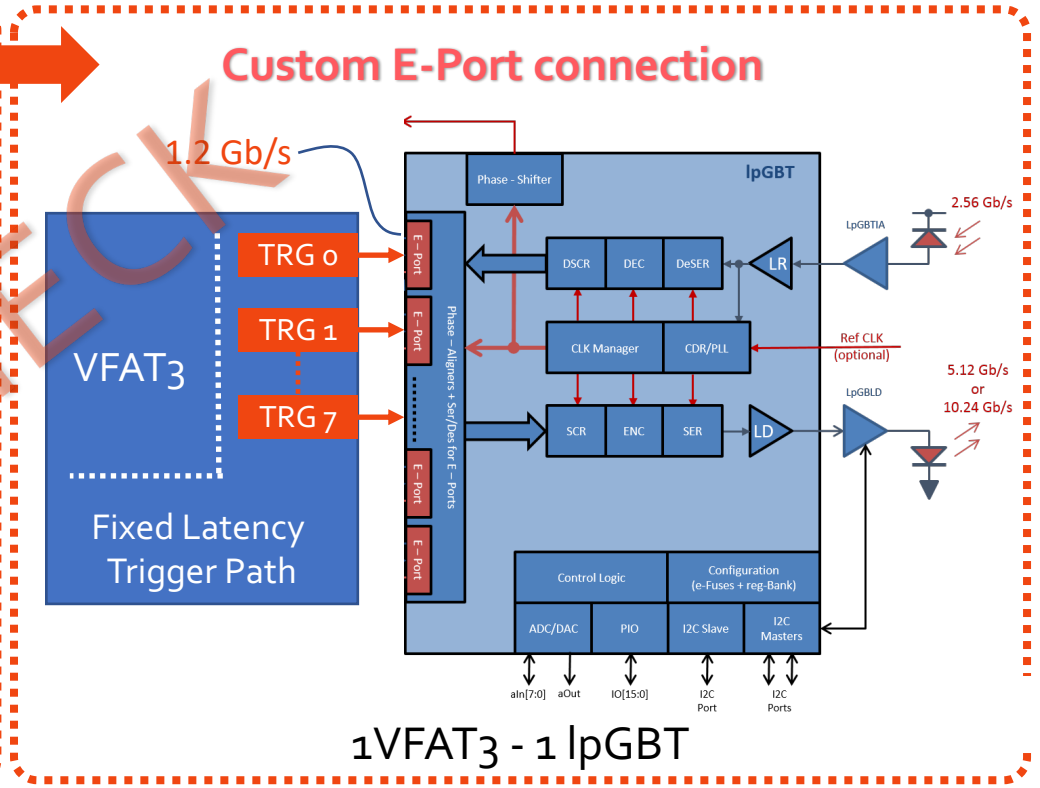
FIXED LATENCY TRIGGER PATH



Trigger Path granularity	Fast OR of 2 channels 320Mbps	*8 slvs output*
	Full granularity, DDR 640Mbps	*Trigger-less operation with full granularity readout*

VFAT3-lpGBT connection





lpGBT inputs configuration

10.24					
FEC5			FEC12		
320	640	1280	320	640	1280
28	14	7	24	12	6

Overall Bandwidth

5 or 12 consecutive errors correction

BW/Input combination

VFAT3/lpGBT vs Region/Station (R1/R2)

	chamber/region	Nch/2gap	VFAT/2gap	lpGBT/2gap	VFAT/region	lpGBT/region
M2R1	12	1920	15	15	180	180
M2R2	24	1904	15	15	360	360
M3R1	12	1896	15	15	180	180
M3R2	24	1911	15	15	360	360
M4R1	12	1944	16	16	192	192
M4R2	24	1917	15	15	360	360
M5R1	12	1897	15	15	180	180
M5R2	24	1922	16	16	384	384
				ASIC (TOTAL)	2196	2196

VFAT3 PD ≈ 320 mW
lpGBT PD ≈ 750 mW (max)

e.g. M1R1 PD ≈ 4.8 W + 11,25 W ≈ 16,05 W/chamber

VFAT3 Pros and Cons

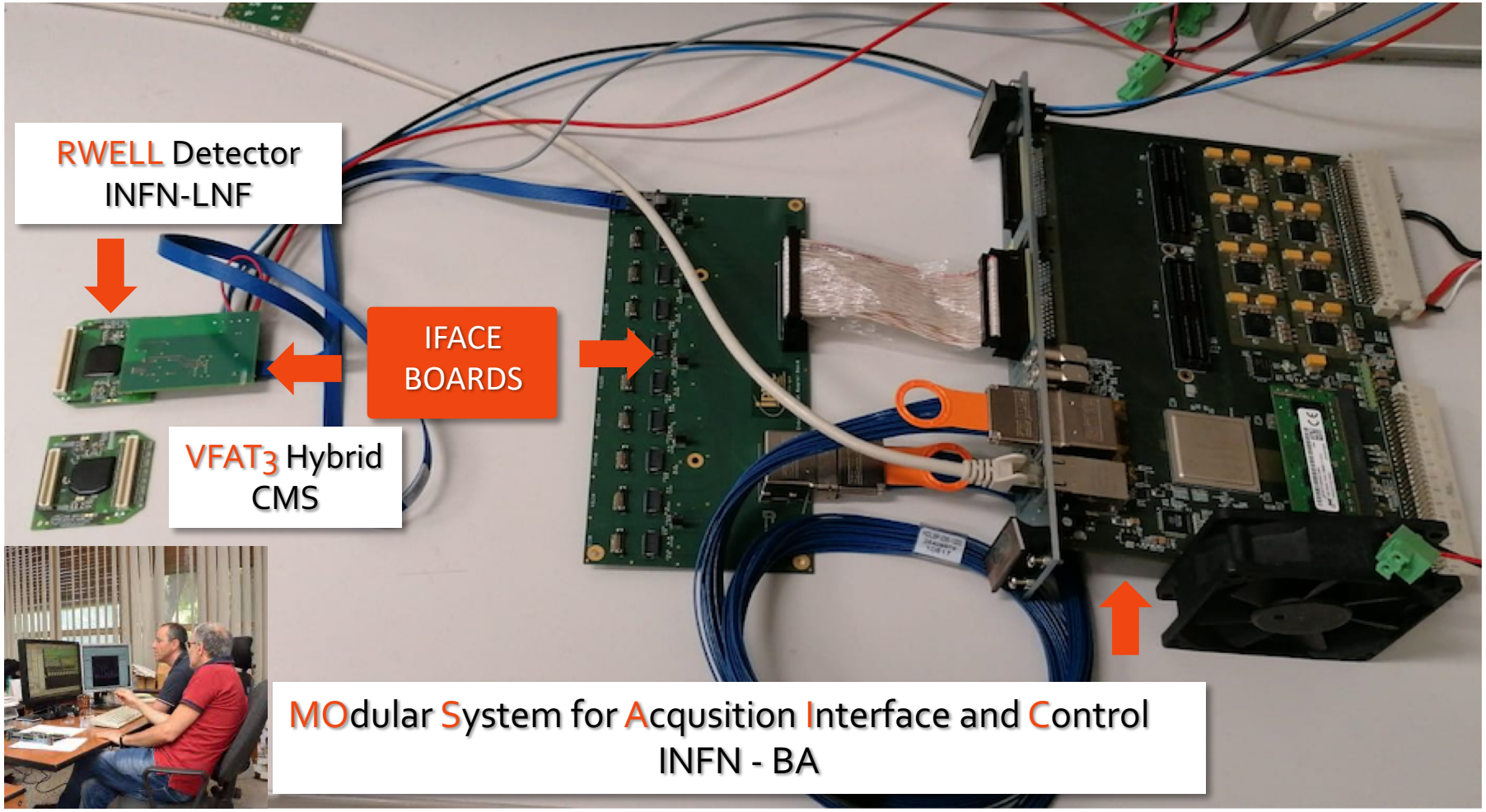
- VFAT3 pros:
  - High modularity
  - Front-End side looks compatible with R1/R2 parasitic (to be verified)
  - Back-End stage : there is a possibility to use VFAT3 trigger output and lpGBT chip (to be verified)

- VFAT3 cons:
  - High PD (a lpGBT must be used for each VFAT3)
  - Cost (number of lpGBT and OL)
  - Time alignment
    - Modularity ≈ 128 channels
    - No time measurement
    - Time step ≈ 3.2 ns

SYNC chip:
- TDC (single channel): 1.6 ns
- Time set (single channel): 32 step - 1.6 ns

Plans: Test the front-end vs input parasitic

CMS colleagues kindly provided us someVFAT3 hybrids



Data Throughput Estimation

GBT & MAP & TIME & ∽ 280 kchs

1 GBT: 48 bits channel map + 48 bits time info (5 bits x first 8 chs + 8 bits err det)

⬇

can assume 2bits/ch for data throughput calculation

⬇

2 bits/ch x ∽280 kchs x 40 MHz ∽ **23 Tb/s (!!!)**

GBT & MAP (NO TIME) & ∽ 280 kchs ∽ 11,5 Tb/s (!!!)

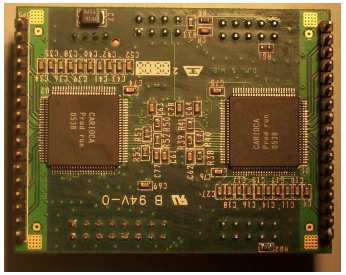
HUGE AMOUNT OF DATA

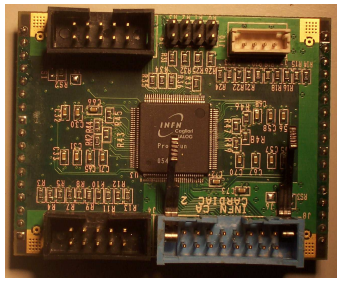
- zero suppression ? (now empty hit map removed)
- track finding ? (hardware routing + redundancy required)

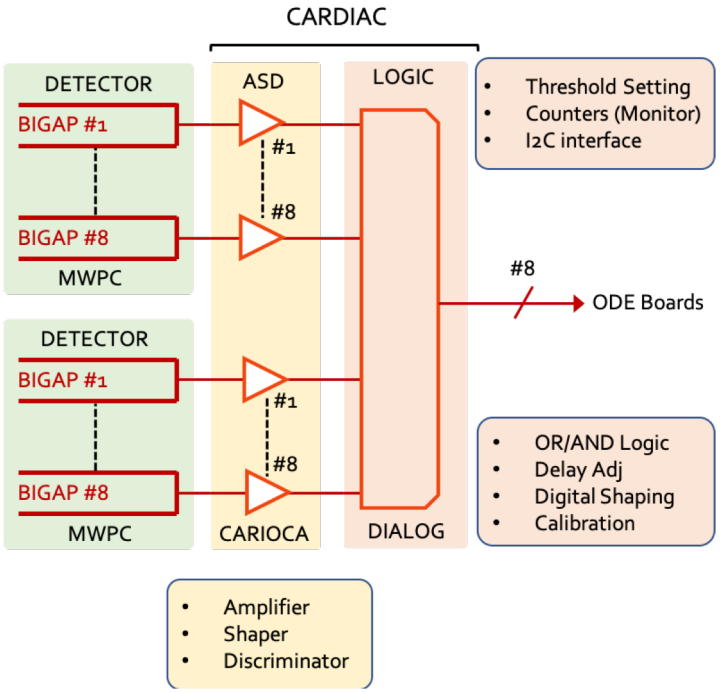
A scheme to reduce uncorrelated events in MWPC
N.Bondar – Oleg Maev

BIGAP & SINGLE GAP READOUT

→ CARIOCA channel connected to a bi-gap ←







THE READOUT OF THE SINGLE GAP ALLOWS A BETTER CONTROL OVER THE FRONT-END OUTPUT

NICOLAI

BIGAP

PROS:
- larger signal
- arrival time (first gap out of 4)

CONS:
- higher rate
- larger noise ($\sigma_n = \sqrt{\sigma_{ng1} + \sigma_{ng2}}$)
- wider dead time (15 ns ?)
- tracks uncorrelated signals

SINGLE GAP

PROS:
- ∽ rate dropped in half
- reduce dead time
- reduce input noise
- reduce the number of fake events (see next)

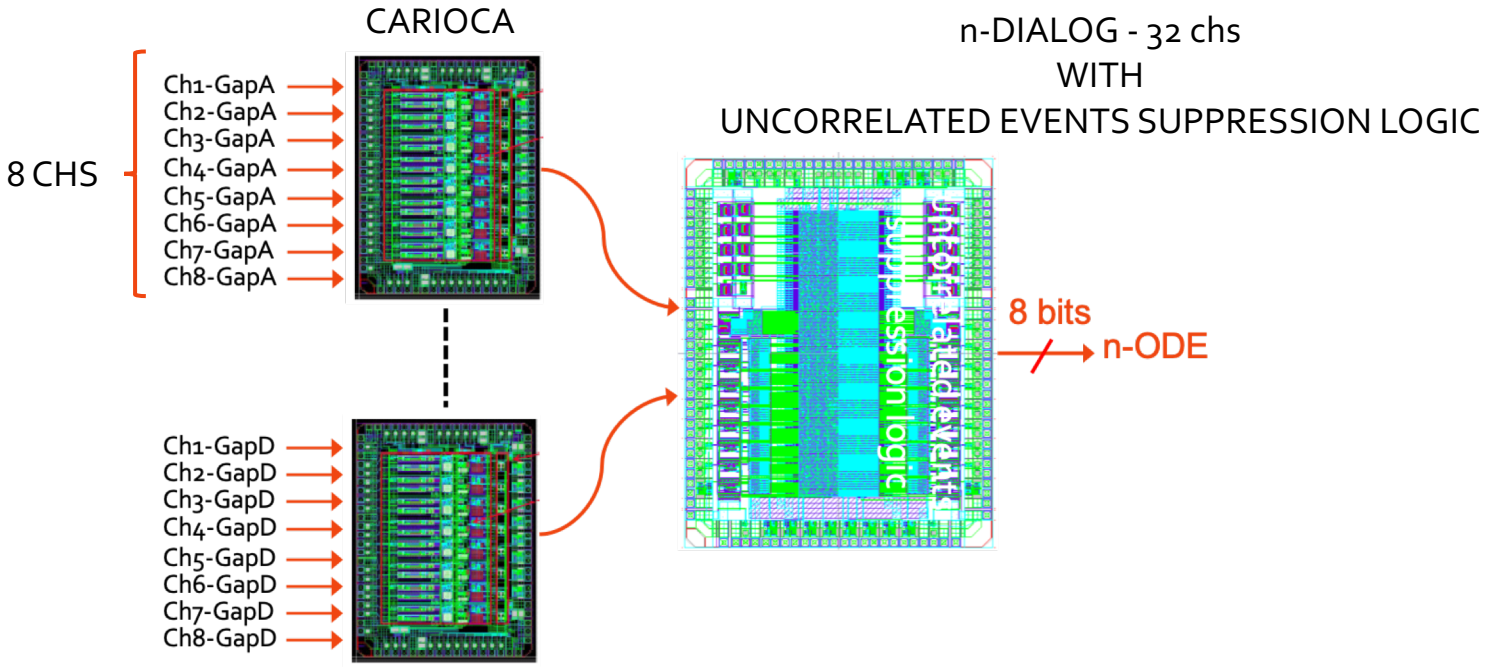
CONS:
- New DIALOG @ 32 chaneles
- New CARIOCA ?!

MWPC GOOD & BAD (UNCORRELATED) EVENTS

GOOD EVENT: hits in 4 (or 3 or 2) gaps within 30 ns

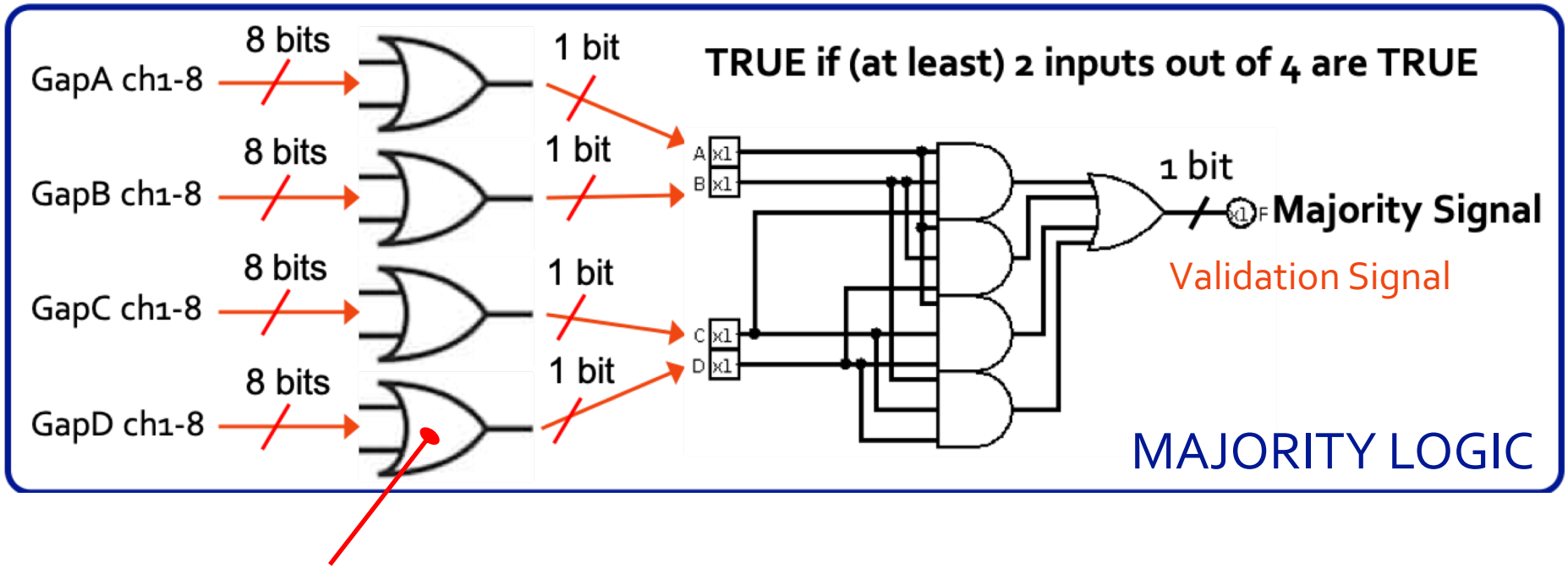
BAD EVENT: hits in only 1 gap

REMOVE UNCORRELATED EVENTS WILL REDUCE FEE OTPUT RATE AT LEAST BY A FACTOR 3-4



Identify the Good Events

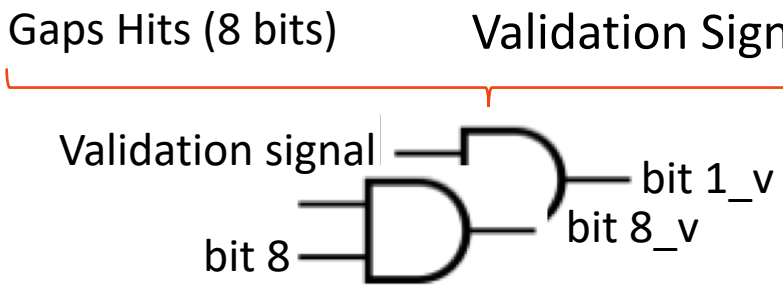
EVENTS WITH HITS IN (AT LEAST) 2 GAPS IN A 25 ns TIME WINDOW



Single gap OR: 8 bits to 1 bit reduction

Majority logic is used, for example, in error correction scheme together with logic redundancy

Propagates Hits ONLY if they Belong to a Good Event



only events with at least one hit in two GAPs (25 ns time window)

GOOD EVENT SELECTION

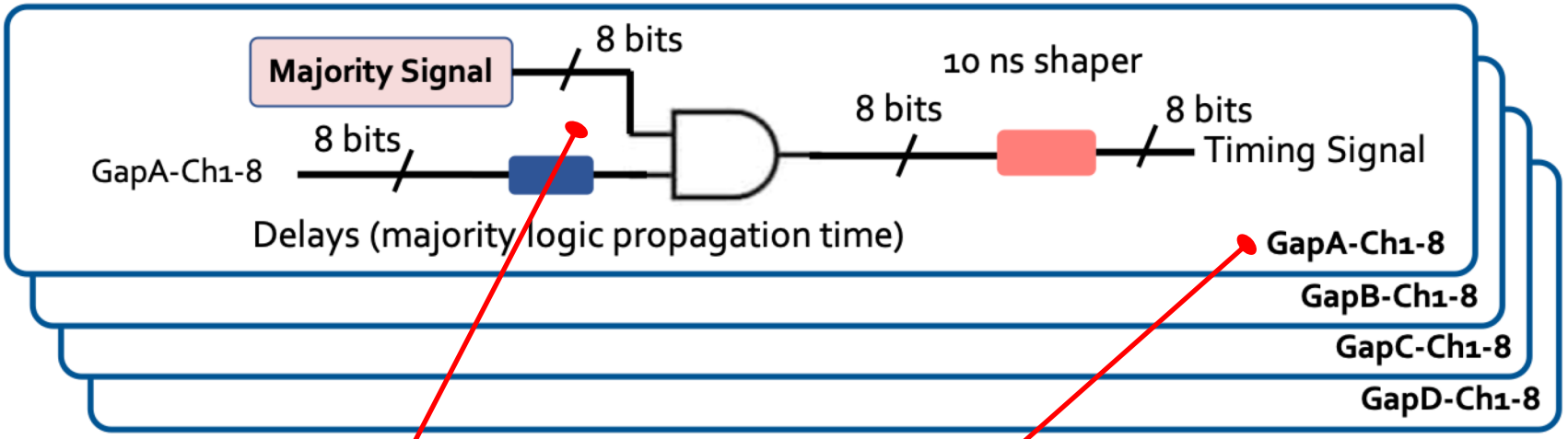
But

SPOILED TIME RESOLUTION

(because the AND in the selection logic; for example we are requiring that signals from GapA and Signal from GapB or GapC or GapD are present to generate a validation signal)

WE NEED A SCHEME TO DECOUPLE THE EVENT SELECTION FROM EVENT TIME INFORMATION

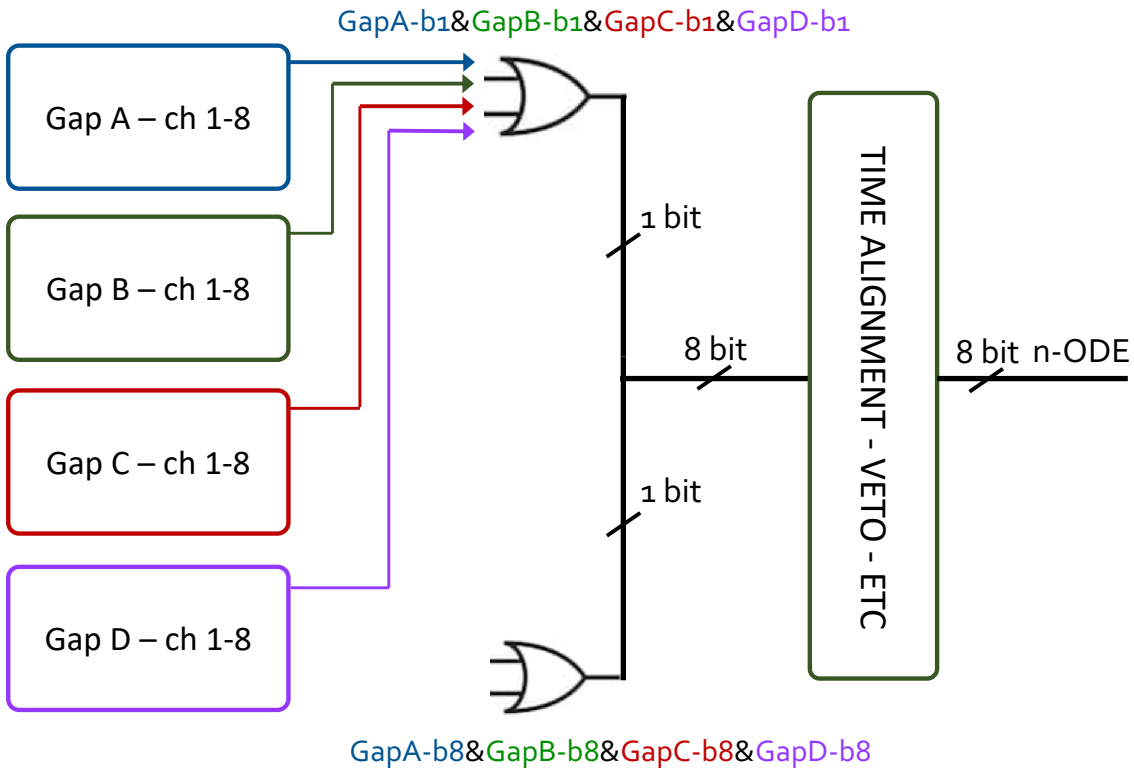
Save the Hits Time Information



- Single hits are delayed (delay = majority logic propagation time)
- The fixed delay do not downgrade the time features of the signal (appreciably)
- The AND logic propagates only hits belonging to a good event without spoiling their time resolution

- 4 bytes
  - Validation TRUE: signals are a delayed replica of the GAP signals
  - Validation = FALSE : no signal is propagated

Reconstruct the Byte for the n-ODE



PROS

- only events with hits in 2 (or more) gaps in a 25 ns time window are transferred
- hit time information preserved
- no change in current DAQ required

CONS

- new front-end design required (porting to a new technology; no fully redesign)

Conclusions

R-WELL readout using VFAT3 ASIC looks feasible but there are a couple of points to investigate: the scheme to transfer data to DAQ and the lack of time measurement

Rejecting uncorrelated events in MWPC FE would reduce the FE output rate at least by a factor 3-4. A scheme to reject these events has been presented. The scheme, based on a validation signal, allows to preserve the hits time information and can reuse current Off Detector Electronics.

THANK YOU