Sensors and Electronics for 4D Vertex Locating

Kazu with input from Martin, Adriano, Edgar, Karol, Jan, Paula and many others!

What do we want?

- Precise vertexing, primary and secondary.
  - Hit resolution
  - Low material
- Radiation hardness
  - Non Uniformity is an additional challenge.
- Time-stamping
  - Fast rise rise time – Sensor & ASIC.
  - High frequency TDC
- Constraints:
  - Power
  - Cost

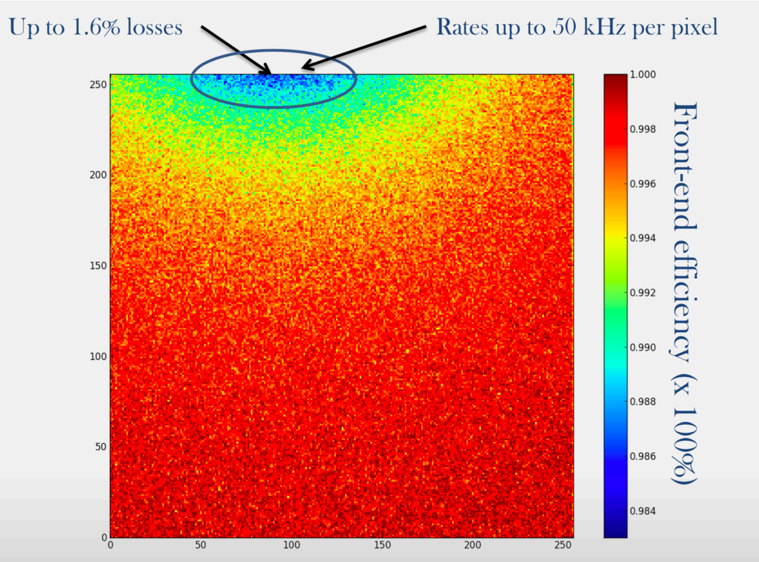
Let's check what has been achieved by others but bear in mind: We have some time to develop new solutions.

In practical terms

- Achieve 20 ps on a track.
  - Per hit time resolution of 50 ps or less
- Pixel size < 55 µm
  - Binary resolution leads to hit resolution of $\frac{55}{\sqrt{12}} = 16\ \mu m.$
  - This translates to the very best IP resolution we can have.
  - There could be other ways to achieve better spatial resolution.
- Operation up to a fluence of $5{\times}10^{16}\ neq$ for the whole U2 lifetime @ $r = 5mm$.
  - Non uniformity of the irradiation poses another challenge.
- Keep under 4 to10% X_0 per track or 1% X_0 per layer
- A future thinner foil would make this even more important.

Tougher environment

- In U1, a 50 kHz hit rate motivates the discharge of the integrator in 200 ns for a 1.6% pile up chance.
- A 7 to 10 times larger instantaneous luminosity increases the rate each pixel gets hit.
- Front end speed makes a charge measurement challenging, and probably also the power consumption.



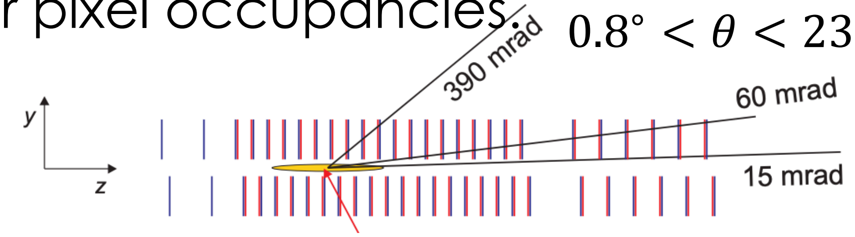
So why not smaller pixels?

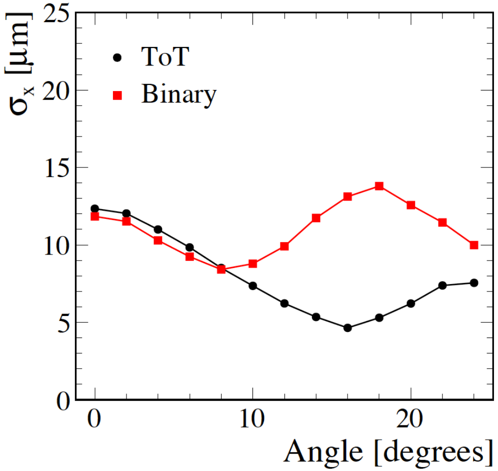
- Smaller pixels give naïvely a better spatial resolution
  - Naïvely, because the thickness needs to be matched. An equally thick sensor (200 μm) would just give 4 to 16 hit clusters instead of 2 for a single track…
- Smaller pixels will require more addressing bits, and therefore, more data.
  - Though this would be a small effect if the gain in resolution is achieved.
- They will consume more power per cm^2…
- It's difficult to fit the whole **analogue** front-end, and save space for the digital **processing**…

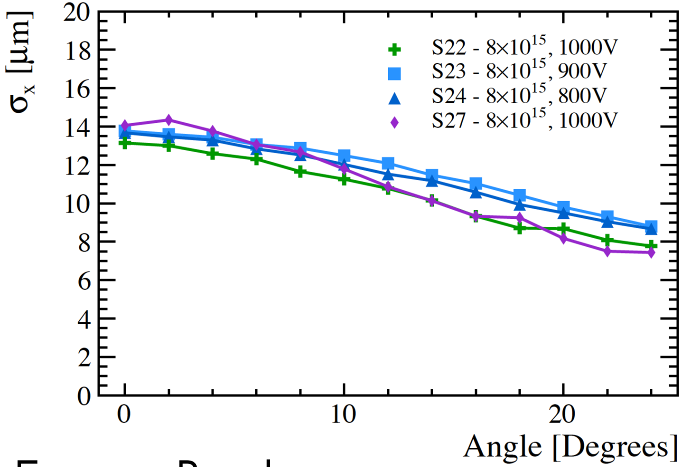
Spatial Resolution

- The easiest way to solve the problem is to segment.
- smaller pixels would also lead to lower pixel occupancies
- We know how to achieve better resolutions without segmentation. Even after irradiation
- However, this comes at a price: even 4 bits can be challenging at the Upgrade data rates

$0.8° < \theta < 23°$







PhD Thesis Emma Buchanan

Time Resolution

- We trust time to solve many of our issues.
- However, 10 years ago Silicon was not the first thought in temporal measurements.
- A lot has changed in the field since then.

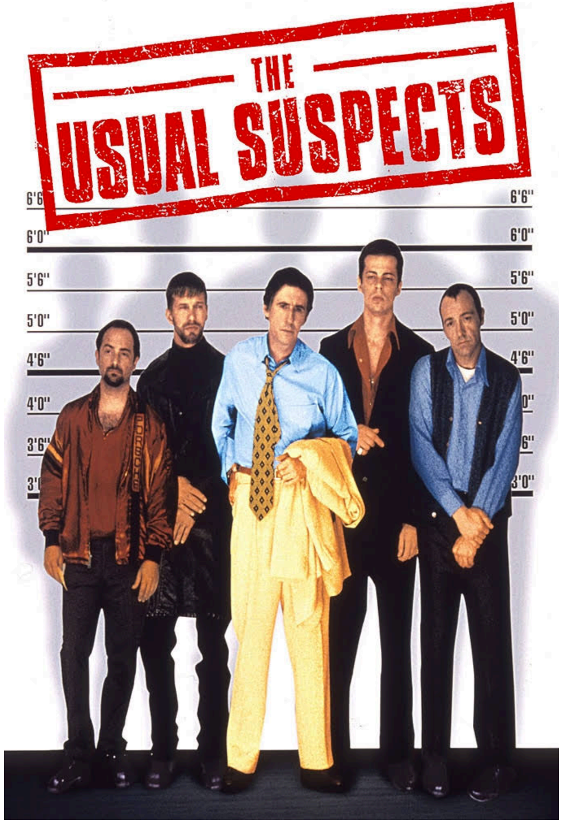
$$\sigma_t^2 = \sigma_{landau}^2 + \sigma_{timewalk}^2 + \sigma_{Distortion}^2 + \sigma_{jitter}^2 + \sigma_{TDC}^2$$

- Whatever solution we might find that will need to be a compromise:
- In general, **segmentation and radiation tolerance** are **not** a synonym to to **fast timing**.
- Power consumption is limited.

Candidate sensor technologies

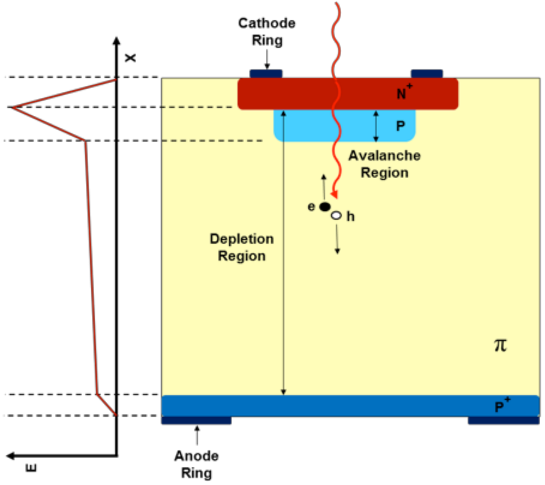
- We have several sensor technologies already in hand but no clear candidate off the shelf.
- The technology has to slowly reveal itself:
- **LGADs**, and their variants are used in ATLAS and CMS.
- **3D concepts** have shown good radiation resistance, and fast timing capabilities.
- **MAPS** have intrinsically low material and integrated processing
- Could the good old **Planar** silicon be revamped?

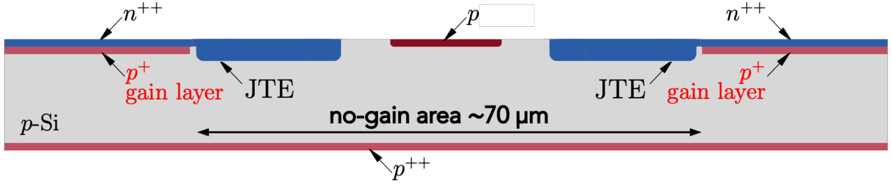
- Who is going to be our Keyser Söze?



Low Gain Avalanche Detectors

- Proposed in 2010 at CNM
- High/Controlled electric Field is used to provide charge multiplication.
- Try to make the sensor response faster with gain.
- Segmentation is challenging, due to the detector implementation.





Junction termination extension necessary At the implant edge to prevent breakdown Due to high field region – numbers vary but general problem is the loss if hit efficiency

Gain and time

CMS has approved the construction of 15 m2 of LGAD

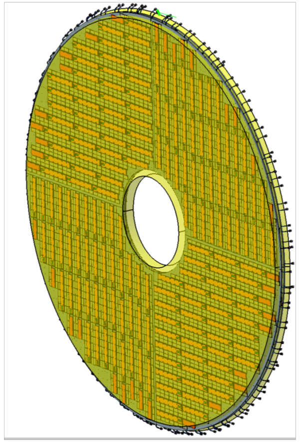
- Each sensor is made of 16x32 pads
- Each pad is 1.3 x 1.3 mm2 (same as ATLAS)
- The CMS timing layer has two disks

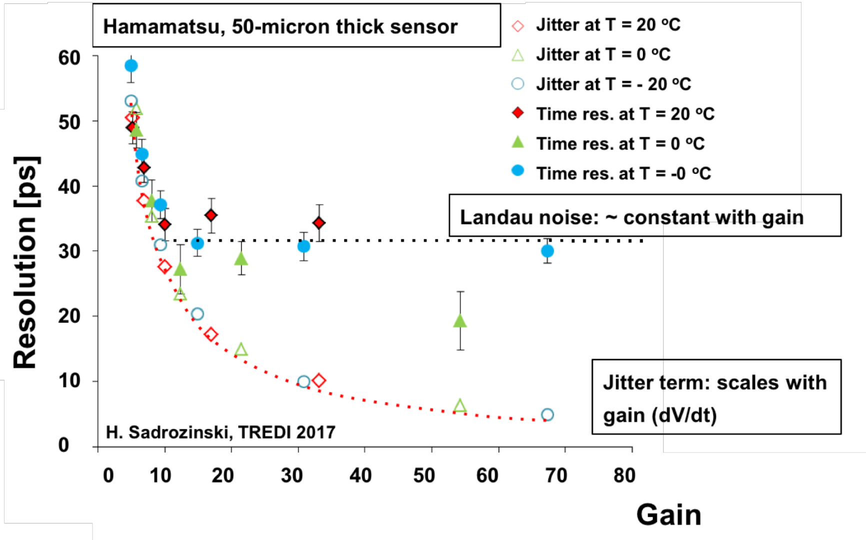
The time resolution per hit is assumed to be 45 ps:

1. 30 ps due to the sensor intrinsic time resolution
2. 30 ps due to the read-out,

Assuming minimum charge: 8 fC/50ke (gain ~ 15)
Worse resolution at lower input charge

CMS MTD



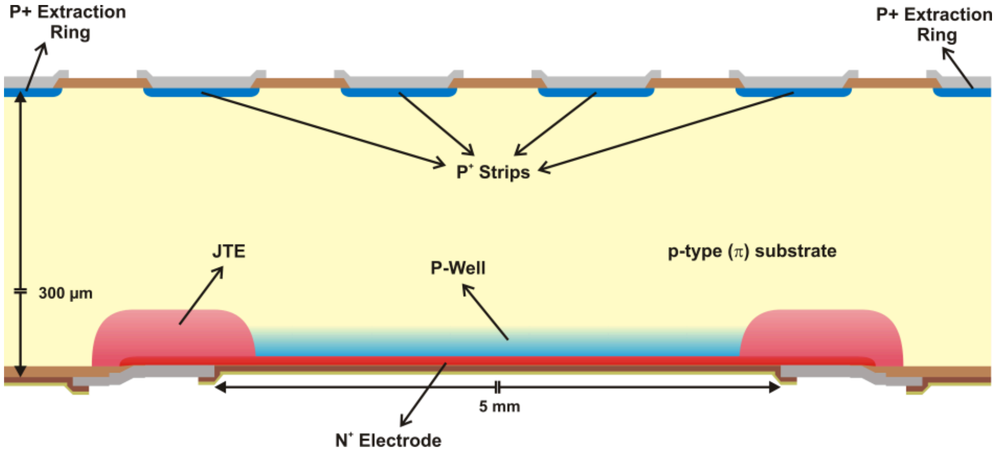


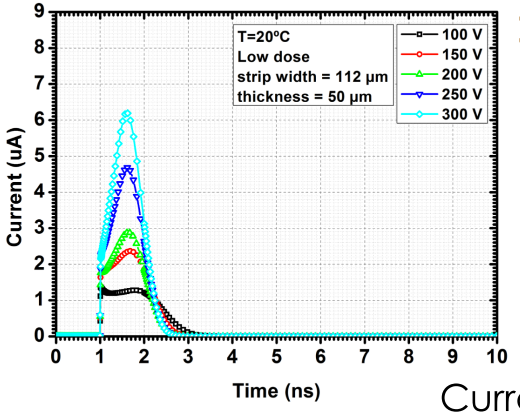
N. Cartiglia RD50/2019

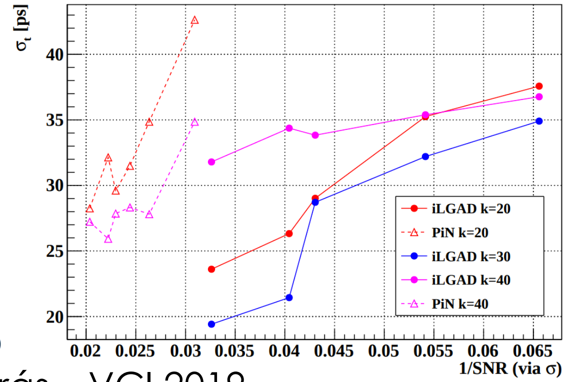
i-LGADs

10.1016/j.nima.2016.05.066
G. Pellegrini et al., 2015.

- Make 1 multiplication layer.
- Segment the opposite side of the sensor.
- High signal immdiately induces a response at the collecting pads.
- Drawback - Double sided processing





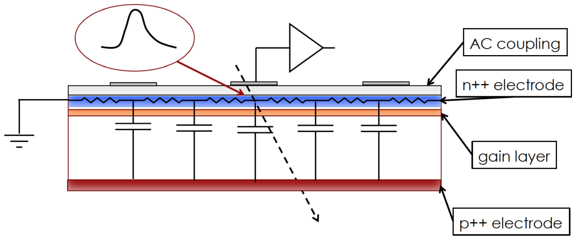


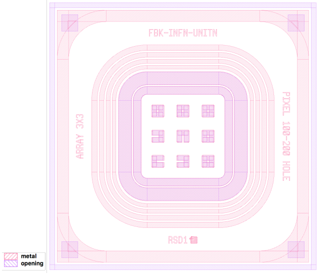
Currás – VCI 2019

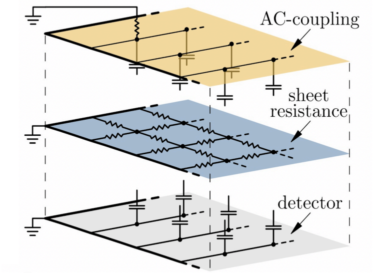
AC-LGADs

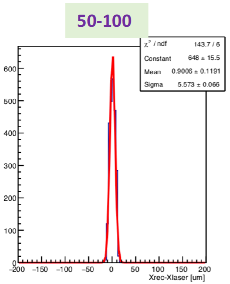
- Promising results from the first production using first resistive AC-LGAD.
  1. The signal is immediately AC-coupled to the metal pad above (if there is one), with a shape "identical" to a equivalent DC LGAD
  2. Large signal (gain 10-20): 5 - 10 fC, fast collection.
  3. Resistive layer acts as a voltage divider.
  4. Signal gets smaller and delayed with distance
- Signals tend to form big clusters, this can help spatial resolution but harm in data rates?
- How do we pre-amp this signal?

R. Arcidiacono – Hiroshima 2019

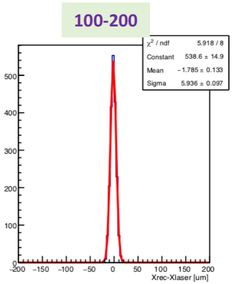








σ_x ~ 6 µm



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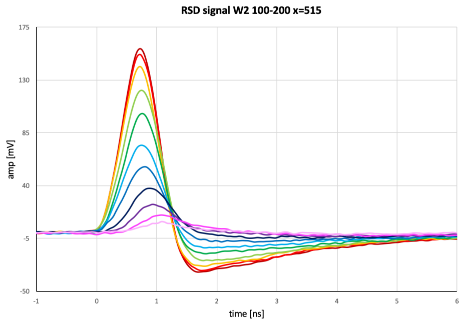
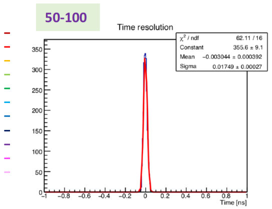
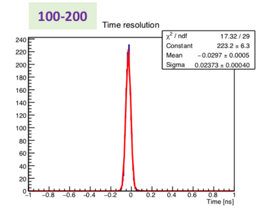




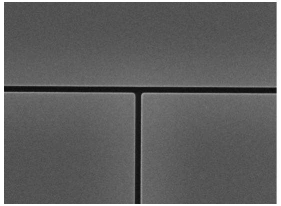
$\sigma = 17\ ps$

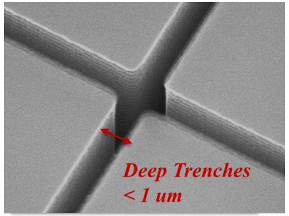


$\sigma = 24\ ps$

TI-LGADs

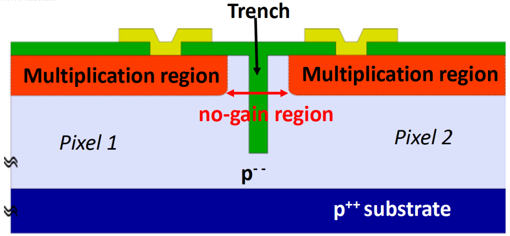
- New **LGAD** technology proposed by FBK:
- **JTE and p-stops are replaced by trenches.**
- Trenches act as a drift/diffusion barrier for electrons and isolate the pixels.
- The trenches area few microns deep and < 1µm wide.
  - Filled with Silicon Oxide
  - The fabrication process of trenches is compatible with the standard LGAD process flow.



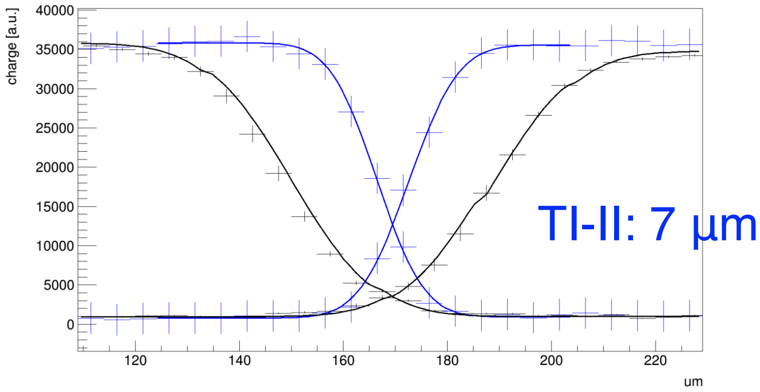


FONDAZIONE BRUNO KESSLER

RD50 Nov/19



Layout	Nominal no-gain	Effective gain-loss
1 Trench	~ 4 um	~6 um
2 Trenches	~ 6 um	~3 um

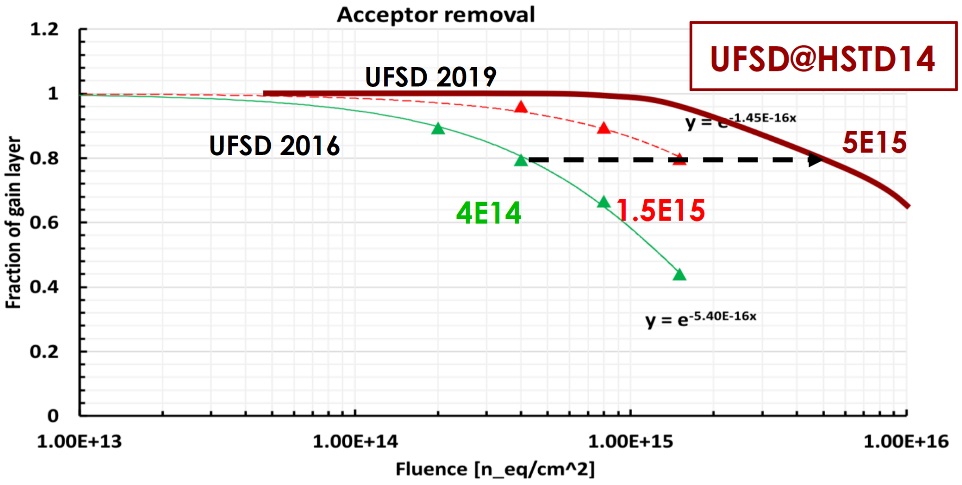


LGADs: Radiation Resistance.

- Irradiation decreases the gain layer doping (acceptor removal)
- Strong R&D in finding the solution to this problem

- VELO has a very non-uniform fluence, can we run with one bias voltage per sensor?
- is it possible to define multiple bias regions?

Prediction for end 2023



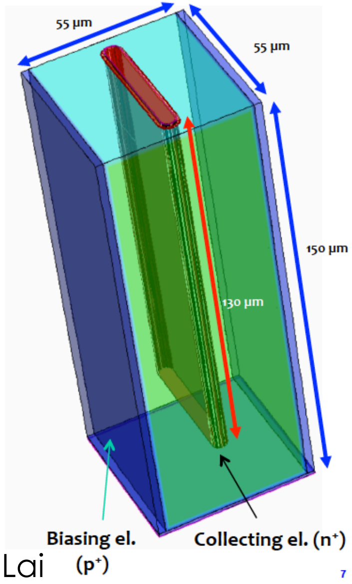
N. Cartiglia, HSTD12/2019

➔Not unreasonable to imagine an extension of good timing performances by a factor of 2-3

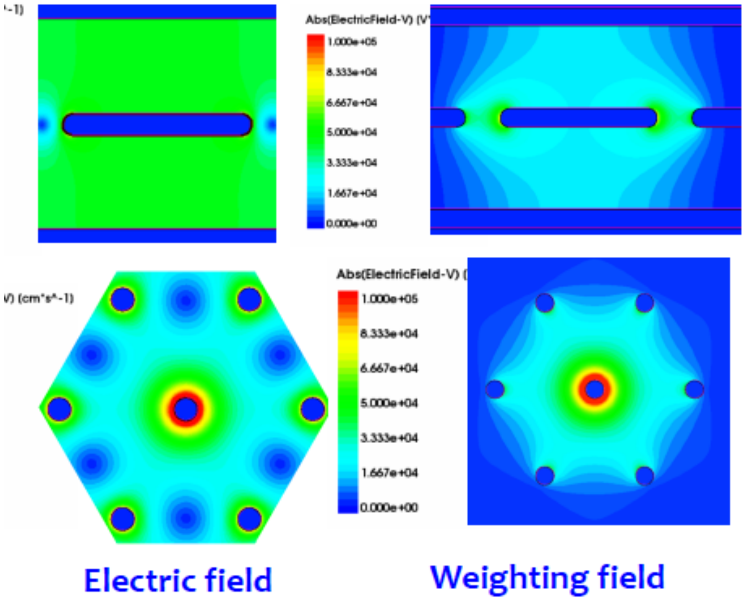
➔Goal: 30 ps at 5E15 neq/cm2

3D and Timespot

- Long implants are always close to the liberated charge.
- Optimisation of the 3D structures is one of the work packages in the TIMESPOT project.
- Use trenches (‘plates’) instead of pillars → more uniform drift and weighting field
- But also more capacitance, and thus noise for the same power budget



Courtesy of A. Lai for the Timespot



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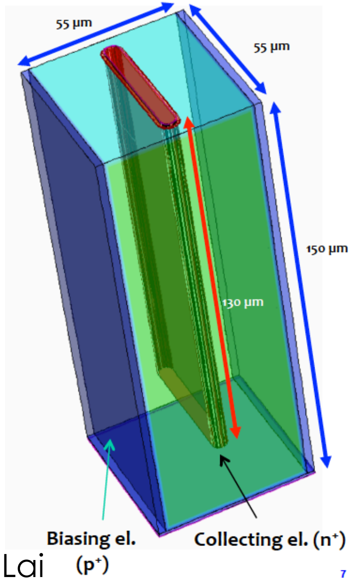

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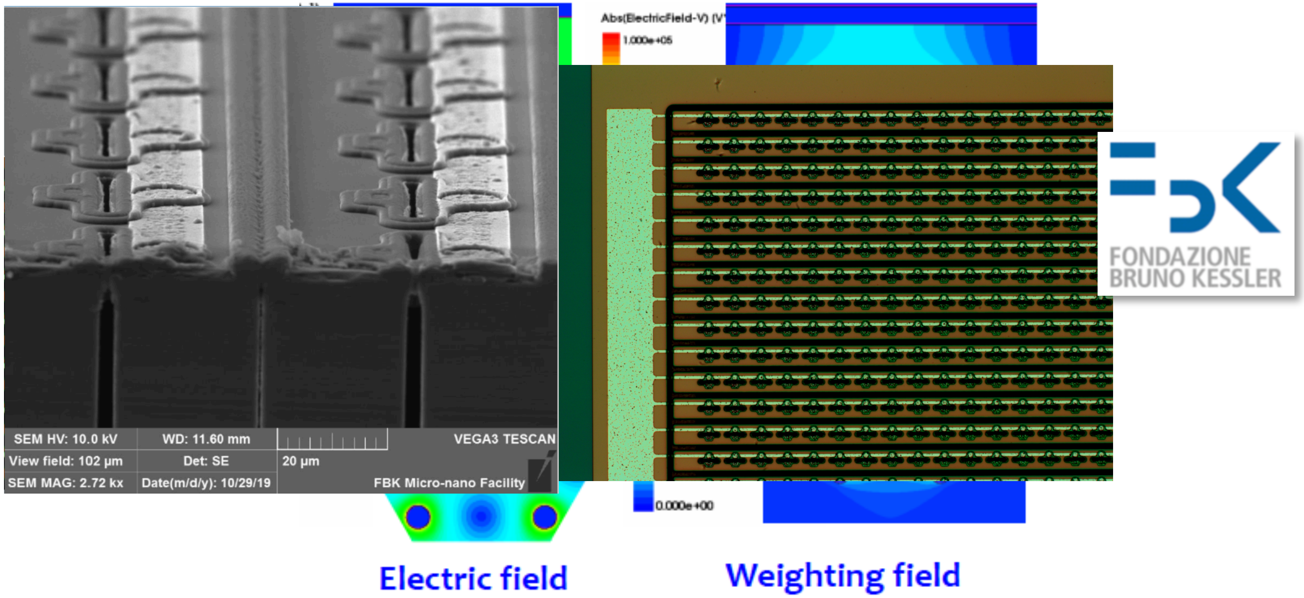
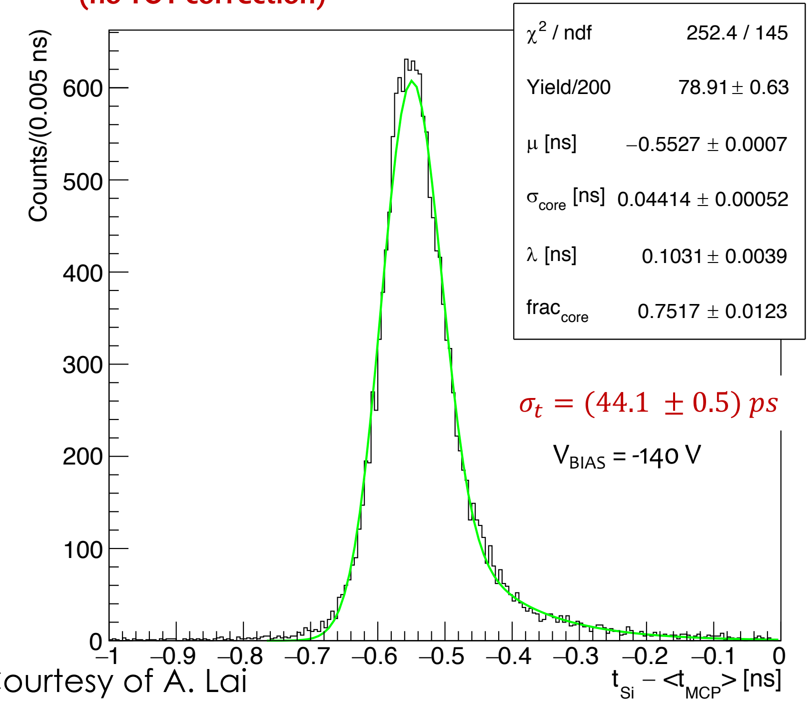


Timespot time resolution

ToA: numerical **leading edge** discriminator with a fixed threshold Th=5mV

(no TOT correction)



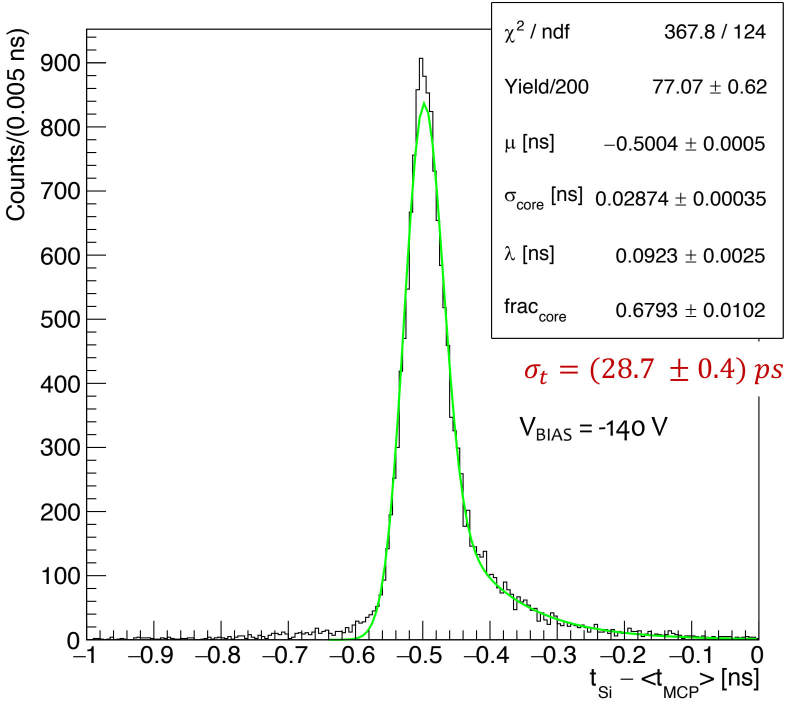
$\sigma_t = (44.1 \pm 0.5)\ ps$

V_{BIAS} = -140 V

Courtesy of A. Lai for the Timespot

Numerical filters to reduce high frequency noise applied

ToA: Numerical **CFD** with a 35% threshold



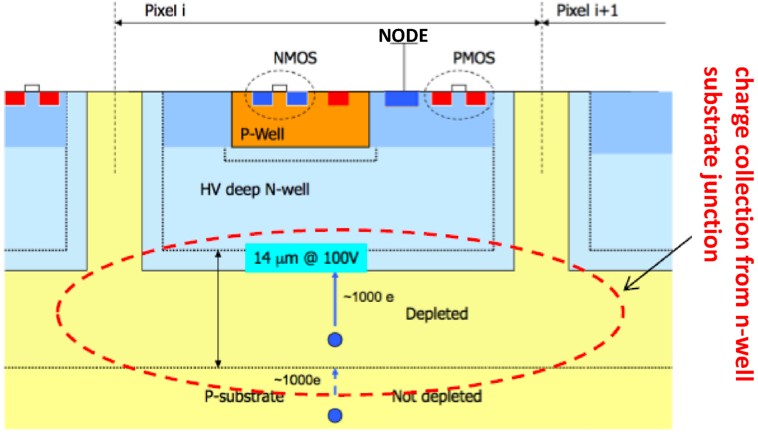
$\sigma_t = (28.7 \pm 0.4)\ ps$

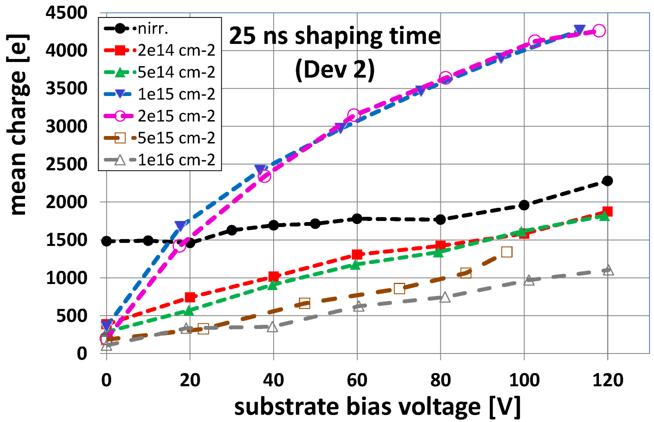
V_{BIAS} = -140 V

MAPS

- Monolithic sensors have shown low material possibilities, and lately radiation tolerance.
- But the combination with temporal resolution seems difficult.
- Different approaches such as SPADs suffer from very low fill-factors and no radiation hardnes…

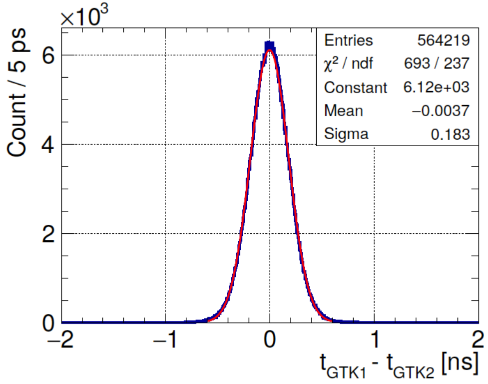
- The desired processing functionality for the VELO will demand the combination with an ASIC (as the CLIC CCPD, reducing the advantage of the low material

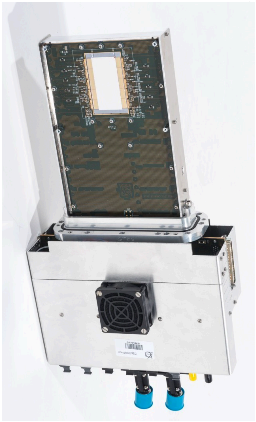


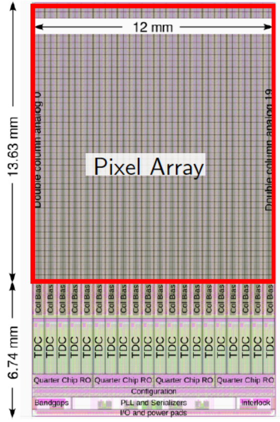


Planar – The GTK

- The NA62 GTK achieved:
- 0.5% X0
- TDC of 97 ps bin size
- TOT for timewalk correction
- Particle rate of 2 MHz/mm2
- Overall per plane resolution of 130 ps.
- Radiation hardness up to 10^16 neq is not outrageou
- At some level charge multplication kicks in.

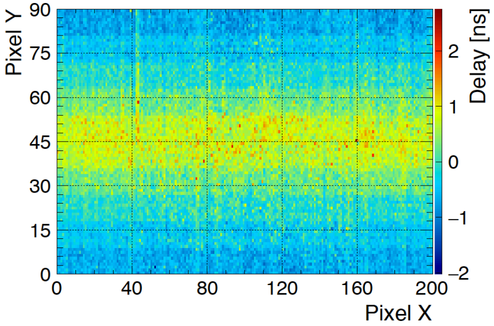


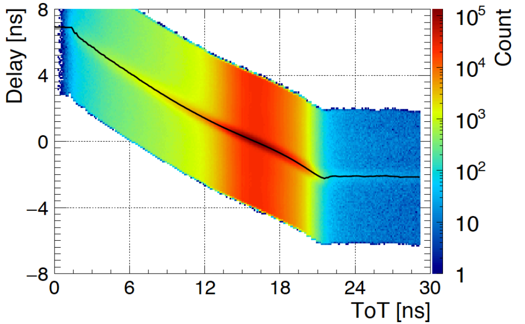




σ [ps]		Resolution [ps]	
GTK1-3	181.3	GTK1	132.0
GTK1-2	183.3	GTK2	127.1
GTK2-3	184.7	GTK3	129.2

arXiv:1904.12837, M. Perrin-Terrin et al.





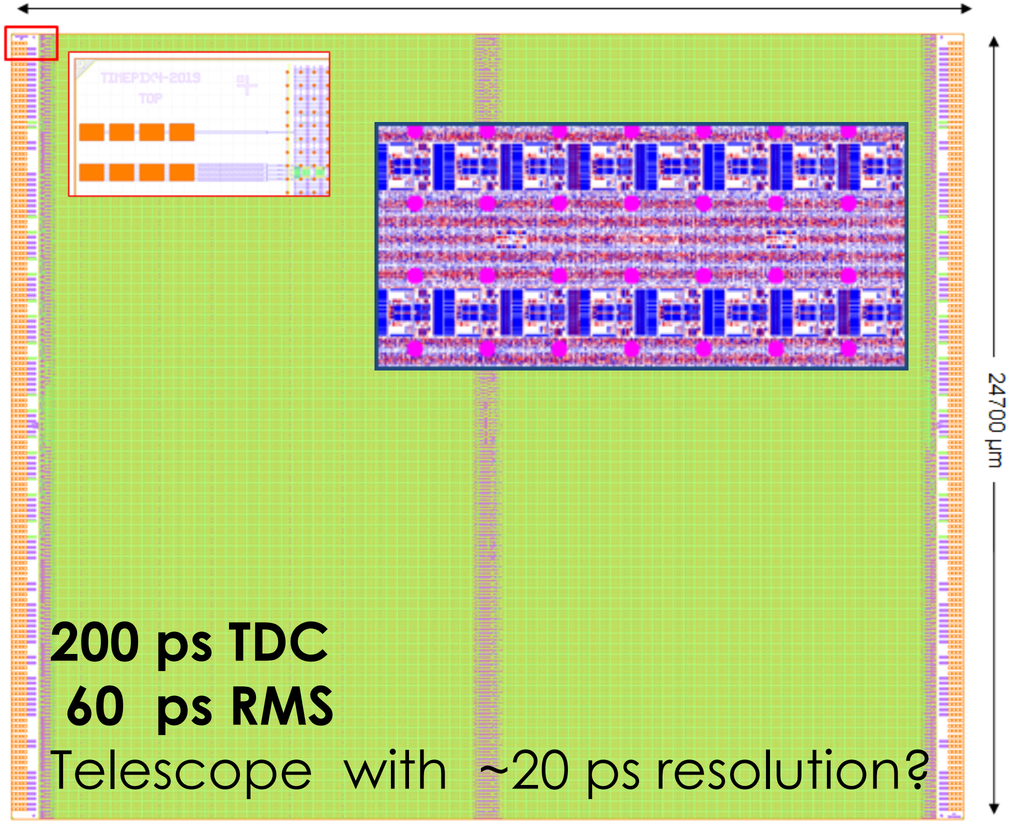
Future ASIC challenges

- Cope with increase in Radiation damage
  - 28 nm seems rad hard to 1 Grad (1e16 neq)
  - Can host 16 times more digital functionality
- Analog front-end does not scale much
  - about the same size as VeloPix/Timepix4 (~30% of pixel)
  - reducing pixel size is more 'expensive' than adding functionality
- Cope with hit pile up:
  - @Upgrade I, MIP discharge time ~200 ns for 1% max pileup.
  - Upgrade II would need 10 times faster rate.
- Per pixel TDC with time resolution < 50 ps.

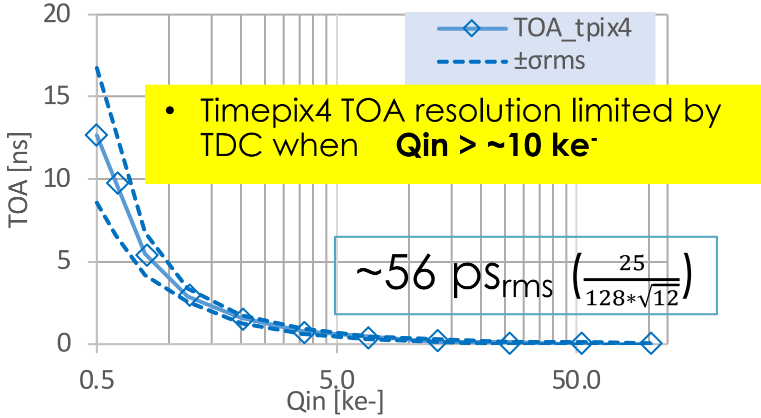
	VeloPix (2016)	Timepix4 (2019)	Velopix2 (202?)
technology	130 nm	65 nm	**28 nm**
Pixel size	55x55 μm^2	55x55 μm^2	**55x55 μm^2**
Sensitive area	2 cm^2	7 cm^2	**2 cm^2?**
Packet size	24 bit	64 bit	**64 bit?**
Max rate	400 Mhits/cm^2/s	180 Mhits/cm^2/s	**4000 Mhits/cm^2/s**
Time resolution	25 ns	200 ps	**20-50 ps?**
Output data rate	20 Gb/s	81 Gb/s	**500 Gb/s?**

- More information in the output at a higher hit rate
- On chip Time-walk correction? CFD?
- Clock distribution effects? On chip calibration?
- Clustering?

Timepix4 – a pathway



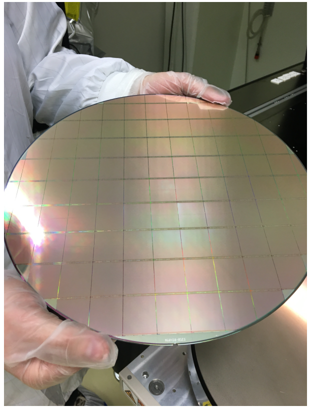
200 ps TDC
60 ps RMS
Telescope with ~20 ps resolution?



- Timepix4 TOA resolution limited by TDC when **Qin > ~10 ke$^-$**

X. Llopard, ESE Seminar

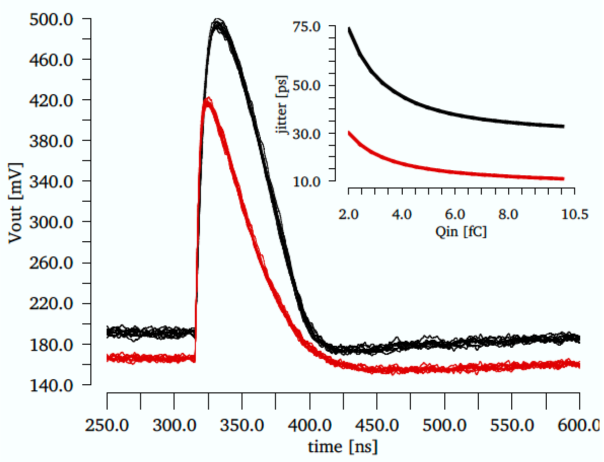
	Timepix4
Tech	65nm – 10 metal
Pixel size	55 x 55 µm
matrix	512 x 448
area	6.94 cm^2
Max rate	358 Mhits/s/cm^2
Max pixel rate	10 kHz/pixel
Time resolution	**~200ps**
Read out speed	≤163.84 Gbps



Timespot ASIC prototype 0 tests

Input Signal	Delta		Sensor	
Power [μW]	***4.1***	***7.2***	***4.1***	***7.2***
G [mV fC^{-1}]	190	168	150	124
σ_n [mV]	2.8	2.0	2.8	2.0
ENC [e]	94	77	120	103
t_{pk} [ns]	16.4	7.7	18.2	10.2
t_A [ns]	2.1	2.1	4.2	3.5
TOT [ns]	100	98	79	78
SR [mV ns^{-1}]	53	98	39	68
σ_j [ps]	54	21	74	30
σ_p [ps]	66	65	67	66
σ_{mm} [ps]	33	26	40	29

CSA performance is limited by power budget



3 TDC schemes	DCO (dithering)	Tapped delay	Time Amplifier
Size (μm^2)	23 x 22	27 x 22	23 x 21
LSB (ps)	190	50	22
RMS (ps)	47	15	37
Power Active (μW)	1200	1200	65
Power Standby (μW)	10	10	34

Courtesy of A. Lai for the Timespot

Prototype zero:
Very useful to gain confidence with 28-nm

Measured performance was **~ x2 worse than expected:** Gain drop due to under-estimated parasitic in the feedback loop (post layout simulations were not accurate enough)

Overall measured time resolution was in the range of 150 ps (LP) to 70 ps (HP) (measured @ 150 fF sensor capacitance, which is a very pessimistic case: measured 100 fF +/– 20%).

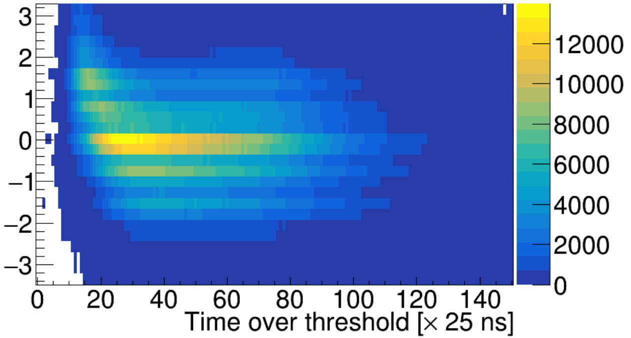
Summary

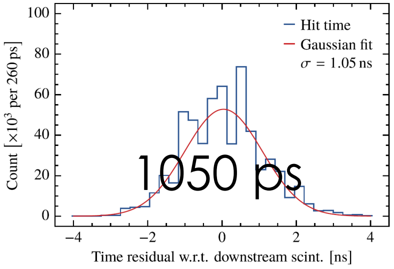
- It is early to point to the real culprit/candidate but the main suspects are identified.
  - But none is ruled out yet
- There is a lot of work ongoing in the direction of fast electronics and fast sensors.
- The radiation level and its non-uniformity is a big challenge.
- Having Space-Time high resolution is mandatory for our physics goals.

Improving the telescope

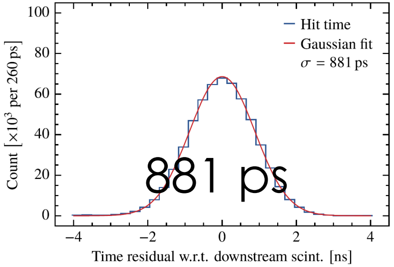
K. Heijhoff Testbeam 2018

Time walk correction

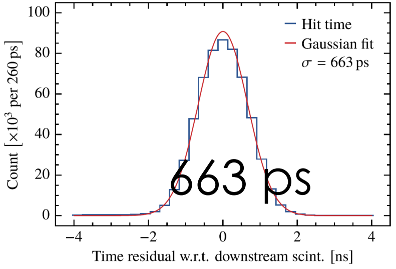




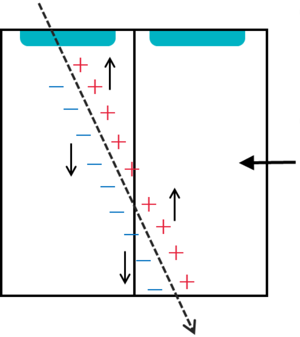
After electronics crorrection

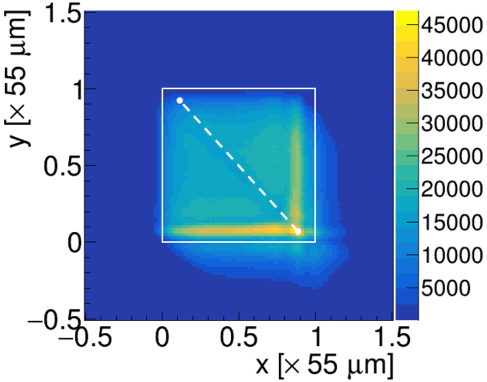


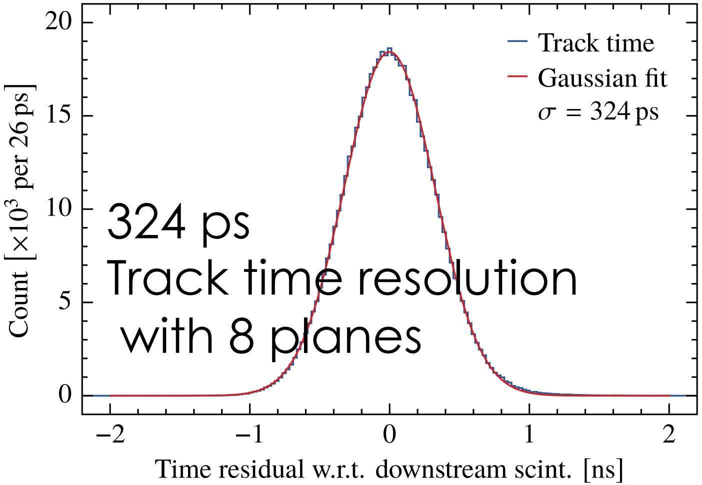
TW+drif time



Drift time correction







Gain, working points

The region for LGAD operation is quite narrow. RED points show the 30 ps performance, which depends not only in gain but also in the drift field.

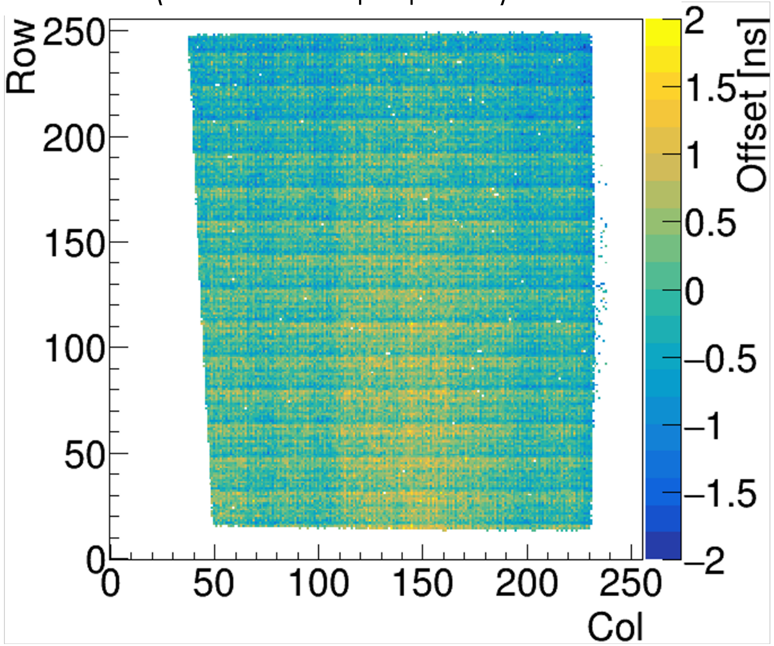
Can these detectors operate at non–uniform irradiation?

R. Arcidiacono – HSTD12 – Hiroshima 2019

System wide implementation

- Pixel matrix variations affect the resolution.
- With better resolutions, per pixel corrections become more and more important.
- Telescope is based on 300 μm thick p-on-n sensors, which are not optimized for timing.

Mean time residual per pixel (TPX3 telescope plane)

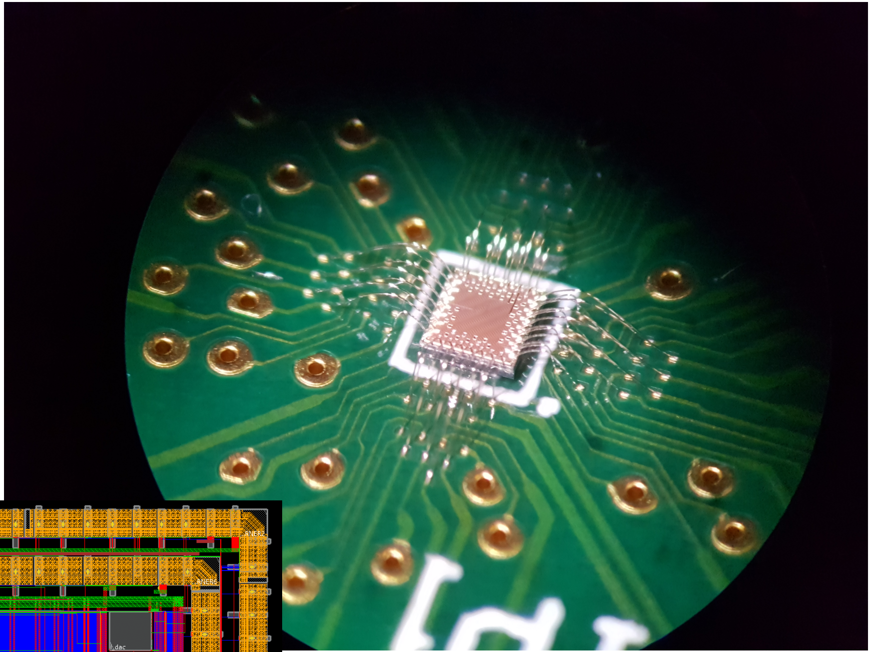


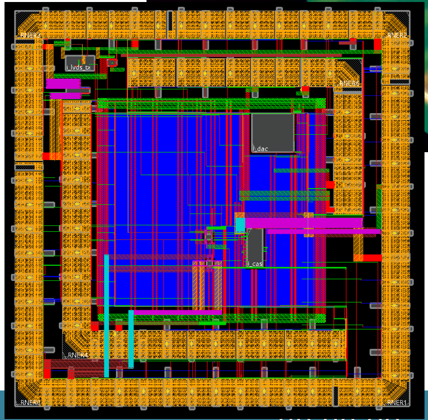
K. Heijhoff BTTB7 - 2019

1st Time spot prototype in 28-nm CMOS

- Main purpose: gain confidence on 28-nm CMOS and test technology performance.
- All cells are kept independent and directly accessible from external pins (with a few exceptions)

  → strongly pad-limited





Integrated cells:

- 3 different TDC solutions
- 6-bit DAC + SPI I/F
- 8-channels CSA+Discriminator
- Programmable power (and speed)
- General purpose OPAMP
- LVDS Tx/Rx

Total area 1.5x1.5 mm^2
mini@sic