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ESSENTIAL INSTRUMENTATION

AMPLIFIERS / REVISIONS

1 The Ideal Op Amp

2 The Inverting Configuration

3 The Non-inverting Configuration

4 Difference Amplifiers

5 Integrators and Differentiators

6 DC Imperfections

7 Effect of Finite Open Loop Gain and Bandwidth on Circuit Performance

8 Large Signal Operation of Op Amp

ESSENTIAL INSTRUMENTATION

AMPLIFIERS / REVISIONS

1. THE IDEAL AMPLIFIER

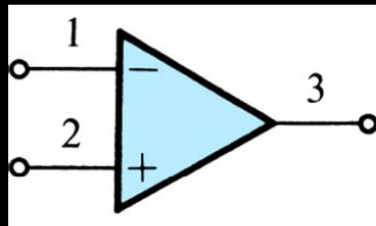
Introduction

- ❑ Their applications were initially in the area of analog computation and instrumentation
- ❑ Op amp is very popular because of its versatility
- ❑ Op amp circuits work at levels that are quite close to their predicted theoretical performance
- ❑ The op amp is treated a building block to study its terminal characteristics and its applications

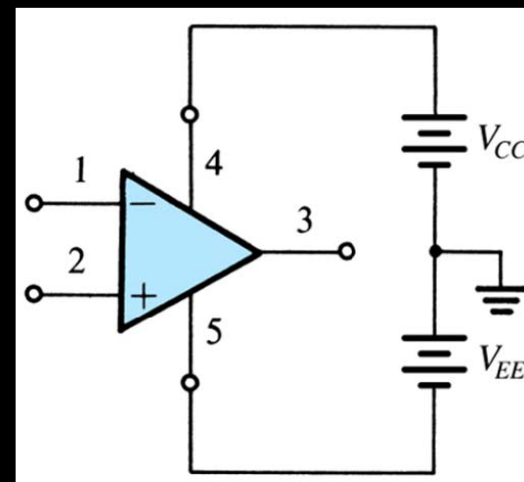
Op-amp symbol and terminals

- ❑ Two input terminals: inverting input terminal (-) and noninverting input terminal (+)
- ❑ One output terminal
- ❑ Two dc power supplies V^+ and V^-
- ❑ Other terminals for frequency compensation and offset nulling

Circuit symbol for op amp



Op amp with dc power supplies



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Ideal characteristics of op amp

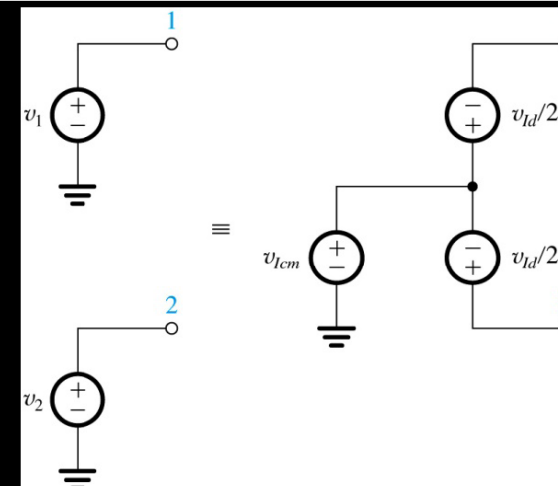
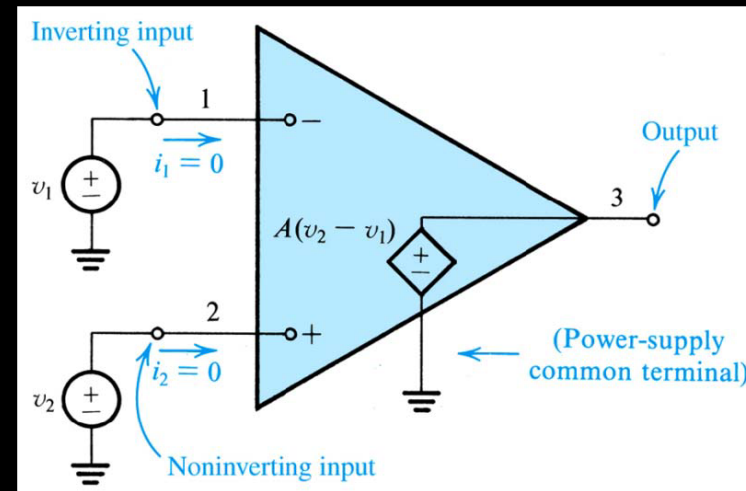
- ❑ Differential-input single-ended-output amplifier
- ❑ Infinite input impedance
 - $i_1 = i_2 = 0$ (regardless of the input voltage)
- ❑ Zero output impedance
 - $v_o = A(v_2 - v_1)$ (regardless of the load)
- ❑ Infinite open-loop differential gain
- ❑ Infinite common-mode rejection
- ❑ Infinite bandwidth

Differential and common-mode signals

- ❑ Two independent input signals: v_1 and v_2
- ❑ Differential-mode input signal (v_{Id}): $v_{Id} = (v_2 - v_1)$
- ❑ Common-mode input signal (v_{Icm}): $v_{Icm} = (v_1 + v_2)/2$
- ❑ Alternative expression of v_1 and v_2 :

$$v_1 = v_{Icm} - v_{Id}/2$$

$$v_2 = v_{Icm} + v_{Id}/2$$



2. THE INVERTING CONFIGURATION

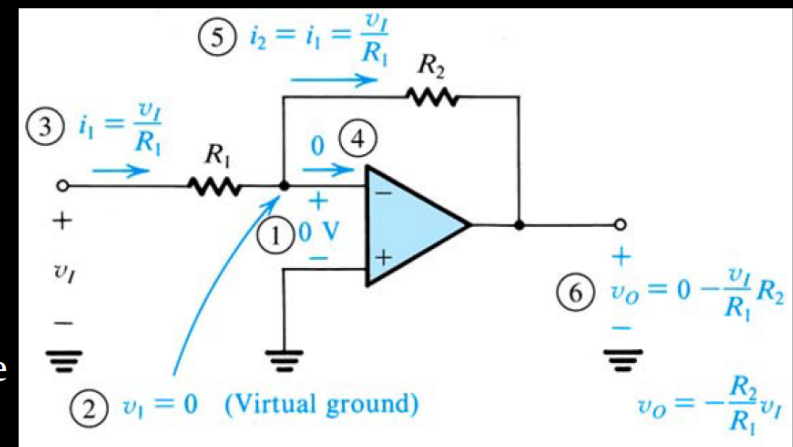
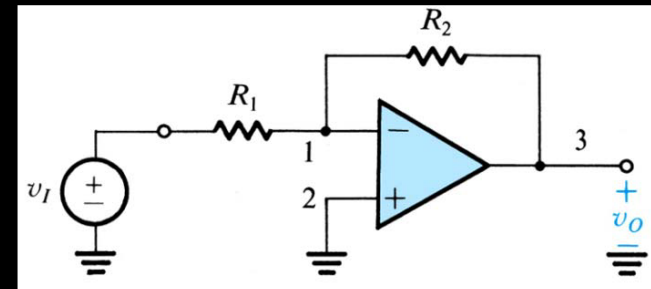
The inverting close-loop configuration

- ❑ External components R_1 and R_2 form a close loop
- ❑ Output is fed back to the inverting input terminal
- ❑ Input signal is applied from the inverting terminal

Inverting-configuration using ideal op amp

- ❑ The required conditions to apply virtual short for op-amp circuit:

- Negative feedback configuration
- Infinite open-loop gain
- ❑ Closed-loop gain: $G \equiv v_O/v_I = -R_2/R_1$
 - Infinite differential gain: $v_2 - v_1 = v_O/A = 0$
 - Infinite input impedance: $i_2 = i_1 = 0$
 - Zero output impedance: $v_O = v_1 - i_1 R_2 = -v_1 R_2/R_1$
 - Voltage gain is negative
 - ➔ Input and output signals are out of phase
 - Closed-loop gain depends entirely on external passive components (independent of op-amp gain)
 - Close-loop amplifier trades gain (high open-loop gain) for accuracy (finite but accurate closed-loop gain)

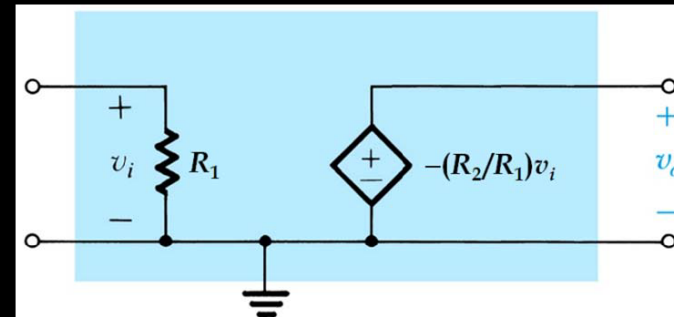
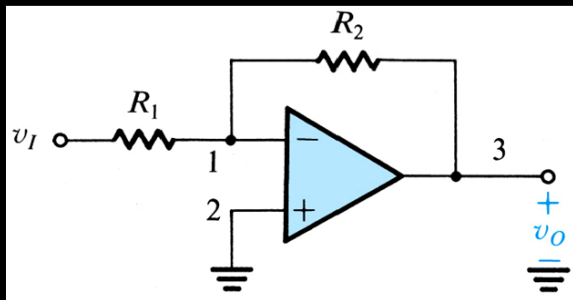


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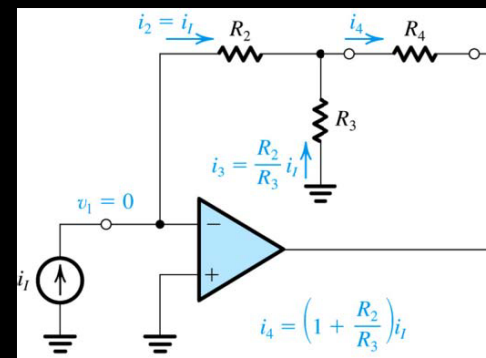
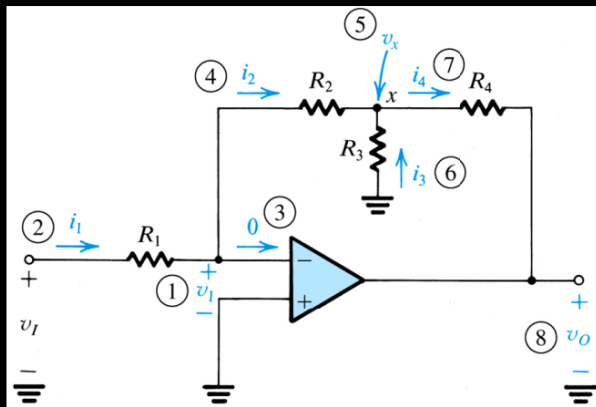
AMPLIFIERS / REVISIONS

□ Equivalent circuit model for the inverting configuration

- Input impedance: $R_i \equiv v_1/i_1 = v_1/(v_1/R_1) = R_1$
 - For high input closed-loop impedance, R_1 should be large, but is limited to provide sufficient G
 - In general, the inverting configuration suffers from a low input impedance
- Output impedance: $R_o = 0$
- Voltage gain: $A_{v_o} = -R_2/R_1$



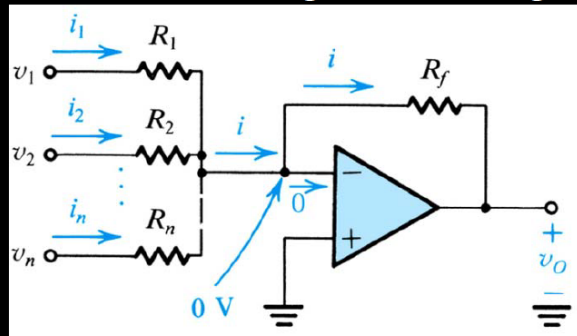
□ Other circuit example for inverting configuration



SOLVE THE FOLLOWING CIRCUITS

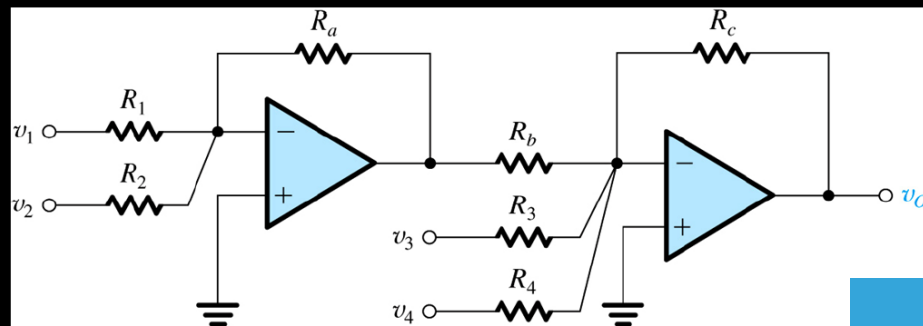
Application: the weighted summer

- A weighted summer using the inverting configuration



hided solution

- A weighted summer for coefficients of both signs



hided solution

3. THE NON-INVERTING CONFIGURATION

The noninverting close-loop configuration

- ❑ External components R_1 and R_2 form a close loop
- ❑ Output is fed back to the inverting input terminal
- ❑ Input signal is applied from the noninverting terminal

Noninverting configuration using ideal op amp

- ❑ The required conditions to apply virtual short for op-amp circuit:

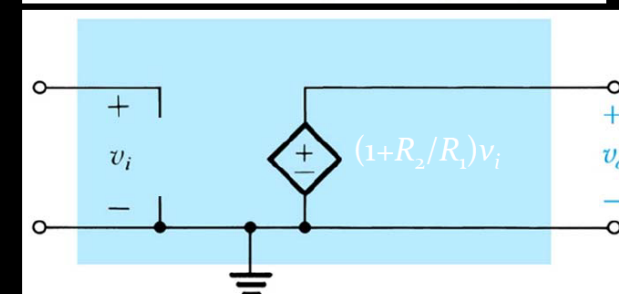
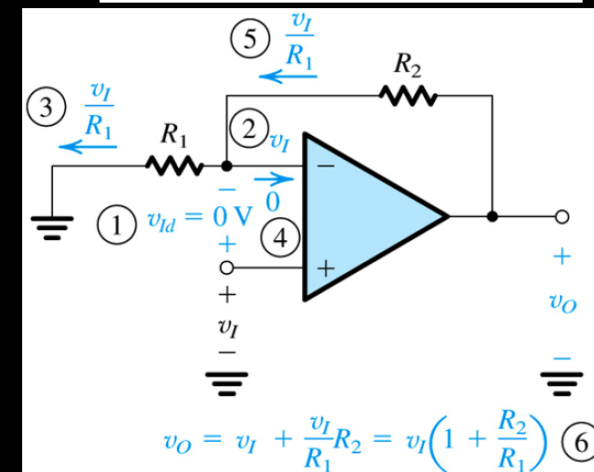
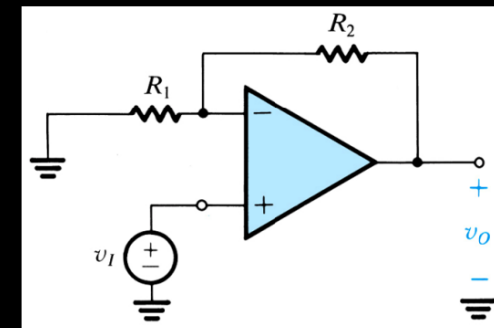
- Negative feedback configuration
- Infinite open-loop gain

- ❑ Closed-loop gain: $G \equiv v_O/v_I = 1 + R_2/R_1$

- Infinite differential gain: $v_+ - v_- = v_O/A = 0$
- Infinite input impedance: $i_2 = i_1 = v_-/R_1$
- Zero output impedance: $v_O = v_- + i_1 R_2 = v_I(1 + R_2/R_1)$
- Closed-loop gain depends entirely on external passive components (independent of op-amp gain)
- Close-loop amplifier trades gain (high open-loop gain) for accuracy (finite but accurate closed-loop gain)

- ❑ Equivalent circuit model for the noninverting configuration

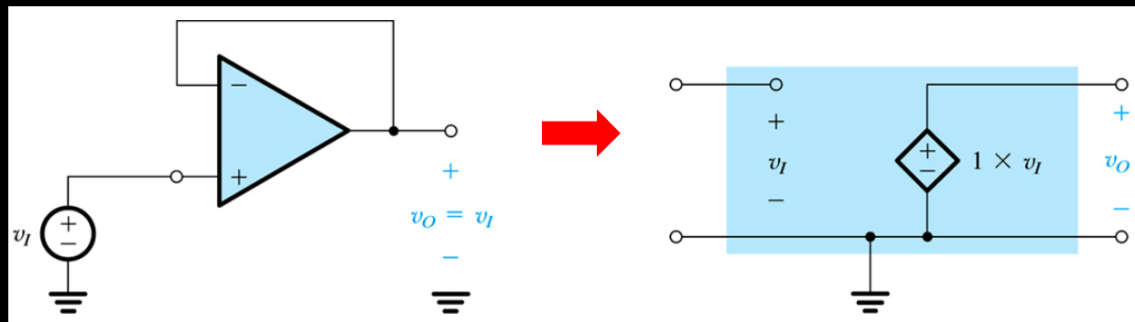
- Input impedance: $R_i = \infty$
- Output impedance: $R_o = 0$
- Voltage gain: $A_{v_o} = 1 + R_2/R_1$



THE VOLTAGE FOLLOWER

The voltage follower

- ❑ Unity-gain buffer based on noninverting configuration
- ❑ Equivalent voltage amplifier model:
 - Input resistance of the voltage follower $R_i = \infty$
 - Output resistance of the voltage follower $R_o = 0$
 - Voltage gain of the voltage follower $A_{v_o} = 1$
- ❑ The closed-loop gain is unity regardless of source and load
- ❑ It is typically used as a buffer voltage amplifier to connect a source with a high impedance to a low-impedance load

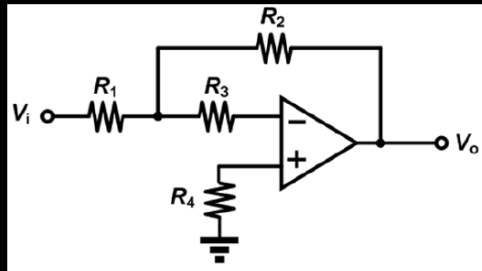


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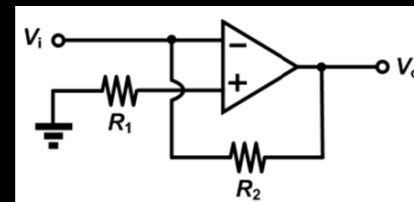
AMPLIFIERS / REVISIONS

Exercise 1: Assume the op amps are ideal, find the voltage gain (v_o/v_i) of the following circuits.

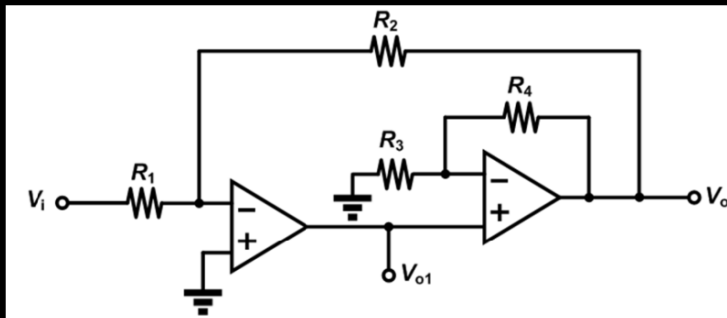
(1)



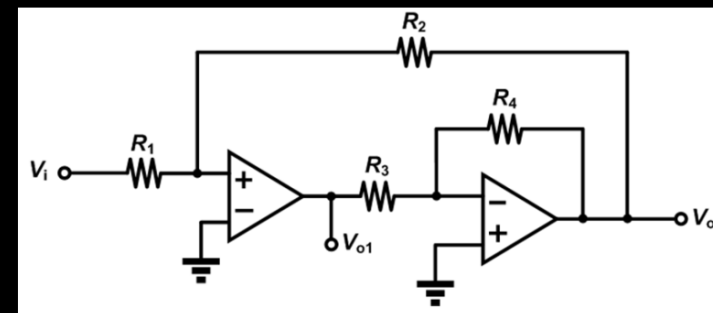
(2)



(3)



(4)

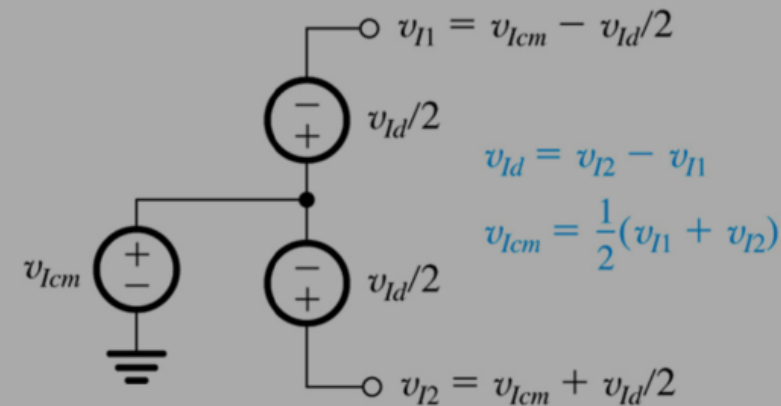
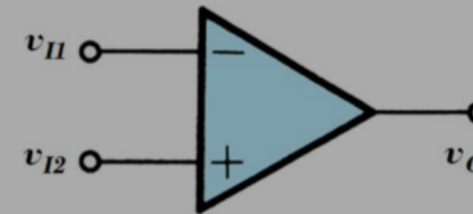


4. DIFFERENCE AMPLIFIERS

Difference amplifier

- ☑ Ideal difference amplifier:
 - Responds to differential input signal v_{Id}
 - Rejects the common-mode input signal v_{Icm}
- ☐ Practical difference amplifier:
 - $v_O = A_d v_{Id} + A_{cm} v_{Icm}$
 - A_d is the differential gain
 - A_{cm} is the common-mode gain
 - Common-mode rejection ratio (CMRR):

$$CMRR = 20 \log \frac{|A_d|}{|A_{cm}|}$$



Single op-amp difference amplifier

$$v_+ = \frac{R_4}{R_3 + R_4} v_{I2} = v_-$$

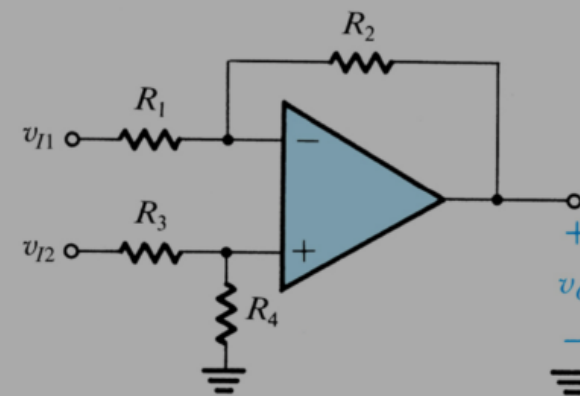
$$v_O = v_- + iR_2 = v_- + \left(\frac{v_- - v_{I1}}{R_1} \right) R_2 = -\frac{R_2}{R_1} v_{I1} + \frac{1 + R_2/R_1}{1 + R_3/R_4} v_{I2}$$

$$= -\frac{R_2}{R_1} (v_{Icm} - v_{Id}/2) + \frac{1 + R_2/R_1}{1 + R_3/R_4} (v_{Icm} + v_{Id}/2)$$

$$= \left(\frac{1 + R_2/R_1}{1 + R_3/R_4} - \frac{R_2}{R_1} \right) v_{Icm} + \frac{1}{2} \left(\frac{1 + R_2/R_1}{1 + R_3/R_4} + \frac{R_2}{R_1} \right) v_{Id}$$



$$A_d = \frac{1}{2} \left(\frac{1 + R_2/R_1}{1 + R_3/R_4} + \frac{R_2}{R_1} \right) \quad A_{cm} = \left(\frac{1 + R_2/R_1}{1 + R_3/R_4} - \frac{R_2}{R_1} \right)$$



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Superposition technique for linear time-invariant circuit

$$\text{Set } v_{I2} = 0 \rightarrow v_{O1} = -(R_2/R_1)v_{I1}$$

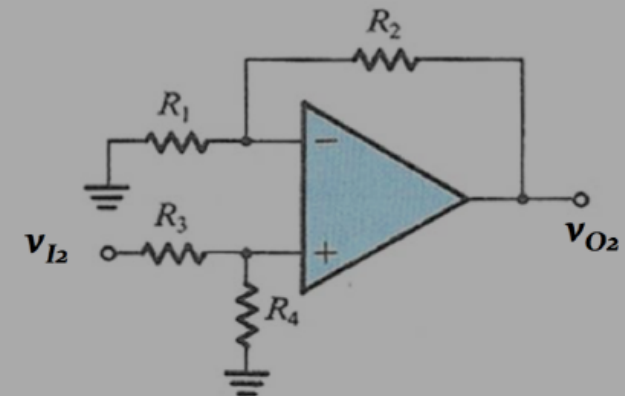
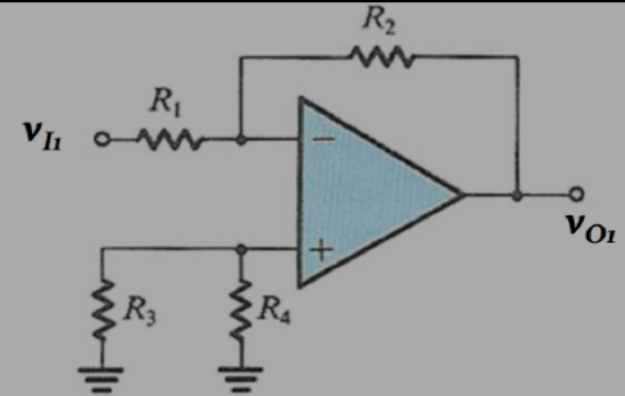
$$\text{Set } v_{I1} = 0 \rightarrow v_{O2} = \left(1 + \frac{R_2}{R_1}\right) \left(\frac{R_4}{R_3 + R_4}\right) v_{I2}$$

$$v_O = v_{O1} + v_{O2} = -\frac{R_2}{R_1}v_{I1} + \frac{1 + R_2/R_1}{1 + R_3/R_4}v_{I2}$$

$$= \left(\frac{1 + R_2/R_1}{1 + R_3/R_4} - \frac{R_2}{R_1}\right)v_{Icm} + \frac{1}{2} \left(\frac{1 + R_2/R_1}{1 + R_3/R_4} + \frac{R_2}{R_1}\right)v_{Id}$$

$$CMRR = 20 \log \left\{ \frac{1}{2} \left(\frac{1 + R_2/R_1}{1 + R_3/R_4} + \frac{R_2}{R_1}\right) / \left(\frac{1 + R_2/R_1}{1 + R_3/R_4} - \frac{R_2}{R_1}\right) \right\}$$

$$\rightarrow A_d = \frac{1}{2} \left(\frac{1 + R_2/R_1}{1 + R_3/R_4} + \frac{R_2}{R_1}\right) \quad A_{cm} = \left(\frac{1 + R_2/R_1}{1 + R_3/R_4} - \frac{R_2}{R_1}\right)$$



❑ The condition for difference amplifier operation: $R_2/R_1 = R_4/R_3 \rightarrow v_O = (R_2/R_1)(v_2 - v_1)$

❑ For simplicity, the resistances can be chosen as: $R_3 = R_1$ and $R_4 = R_2$

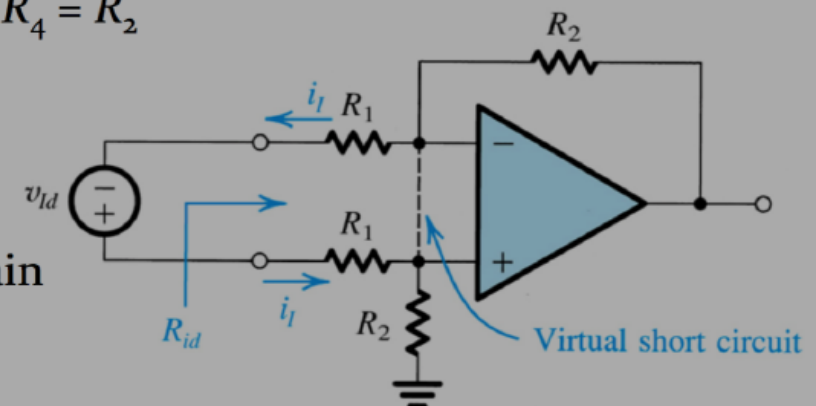
❑ Differential input resistance R_{id} :

■ Differential input resistance: $R_{id} = 2R_1$

■ Large R_1 can be used to increase R_{id}

→ R_2 becomes impractically large to maintain required gain

❑ Gain can be adjusted by changing R_1 and R_2 simultaneously

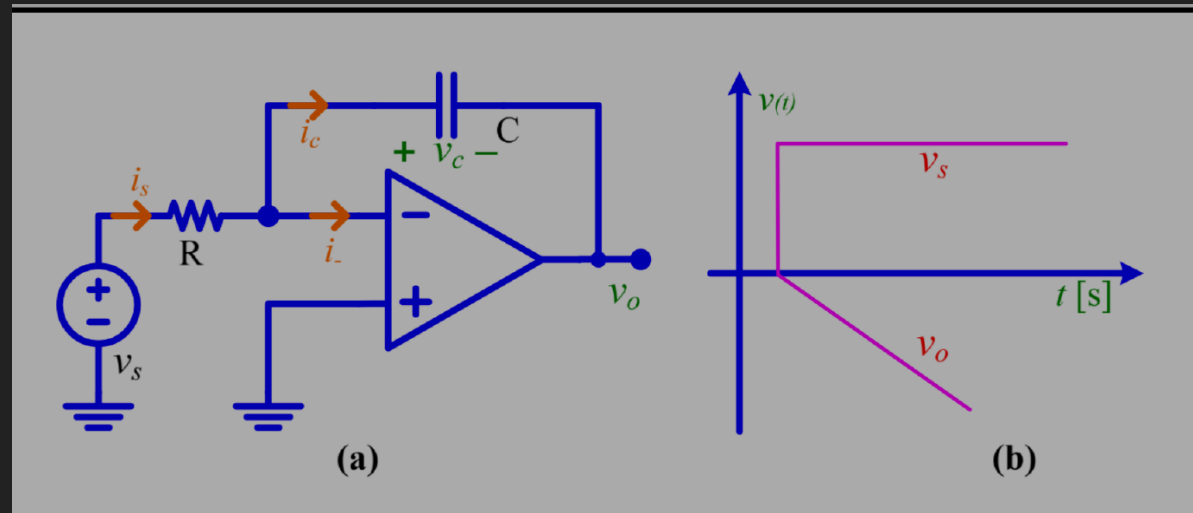


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AMPLIFIERS / REVISIONS

5. INTEGRATORS AND DIFFERENTIATORS

THE INVERTING INTEGRATOR



CURRENTS:

$$i_s = \frac{v_s}{R}$$

$$i_c = -C \frac{dv_o}{dt}$$

OUTPUT VOLTAGE CALCULATION:

Since $i_c = i_s$

$$\int dv_o = \int -\frac{1}{RC} v_s d\tau$$

$$\therefore v_o(t) = -\frac{1}{RC} \int_0^t v_s(\tau) d\tau + v_o(0)$$

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EXAMPLE: Draw the output waveform of the integrator shown in Fig. 1(a) in response to the input shown in Fig. 2. Assume $R=10\text{k}\Omega$, $C=10\text{nF}$ and $v_o(0)=0$.

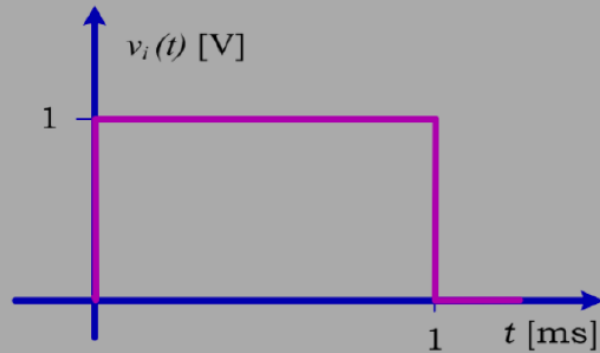


Fig. 2: Step input

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EXAMPLE: Draw the output waveform of the integrator shown in Fig. 1(a) in response to the input shown in Fig. 2. Assume $R=10\text{k}\Omega$, $C=10\text{nF}$ and $v_o(0)=0$.

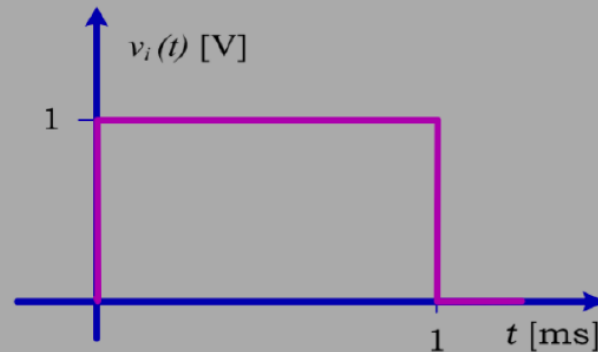
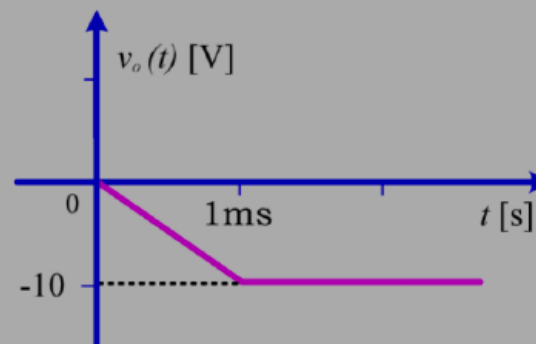


Fig. 2: Step input

Solution:

$$v_o(t) = -\frac{1}{CR} \int_0^t 1 \times d\tau = -\frac{1}{1 \times 10^{-4}} t \quad \text{for } 0 \leq t \leq 1\text{ms}$$

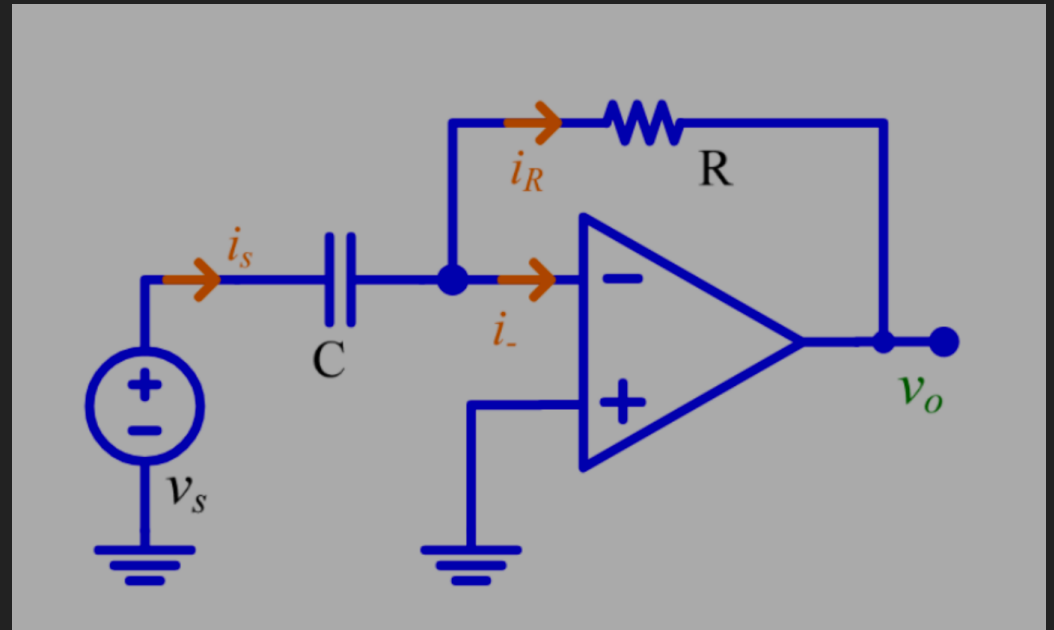
Thus, the output voltage will decrease linearly with time from 0V at $t=0$ to -10V at $t=1\text{ms}$ as shown in Fig. 3.



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THE INVERTING DIFFERENTIATOR



CURRENTS:

$$i_R = -\frac{v_o}{R}$$

$$i_s = C \frac{dv_s}{dt}$$

OUTPUT VOLTAGE CALCULATION:

Since $i_R = i_s$

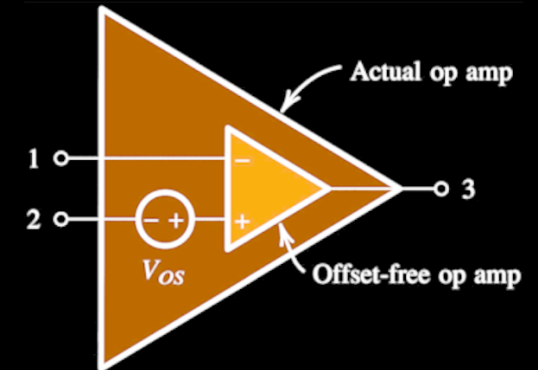
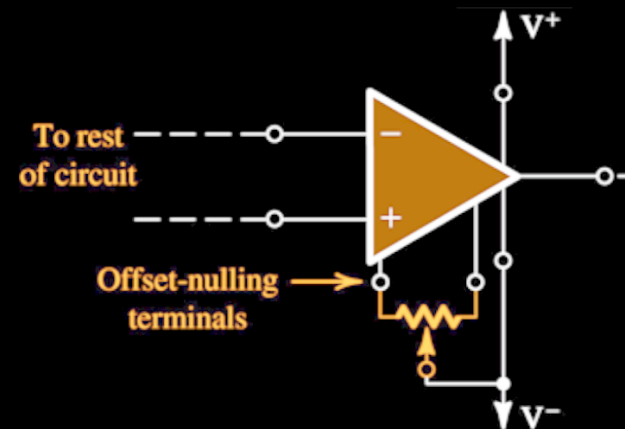
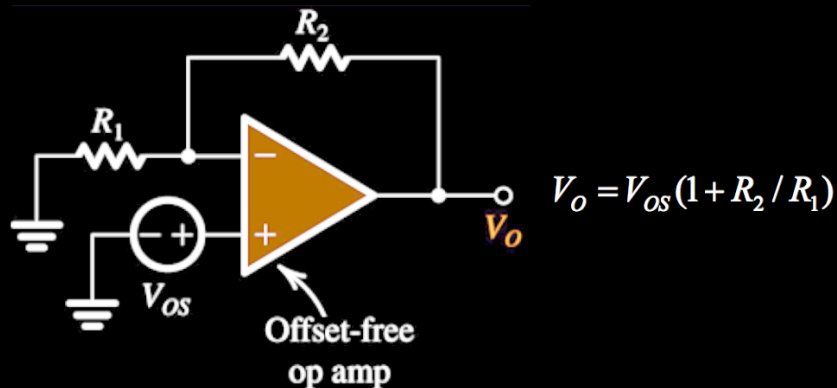
$$v_o = -RC \frac{dv_s}{dt}$$

6. DC IMPERFECTIONS

Offset voltage

- ❑ **Input offset voltage** (V_{OS}) arises as a result of the unavoidable mismatches
- ❑ The offset voltage and its polarity vary from one op-amp to another
- ❑ The analysis can be simplified by using the circuit model with an offset-free op amp and a voltage source V_{OS} at input terminal
- ❑ Typical offset voltage is a few mV

Effect of offset voltage for a closed-loop amplifier



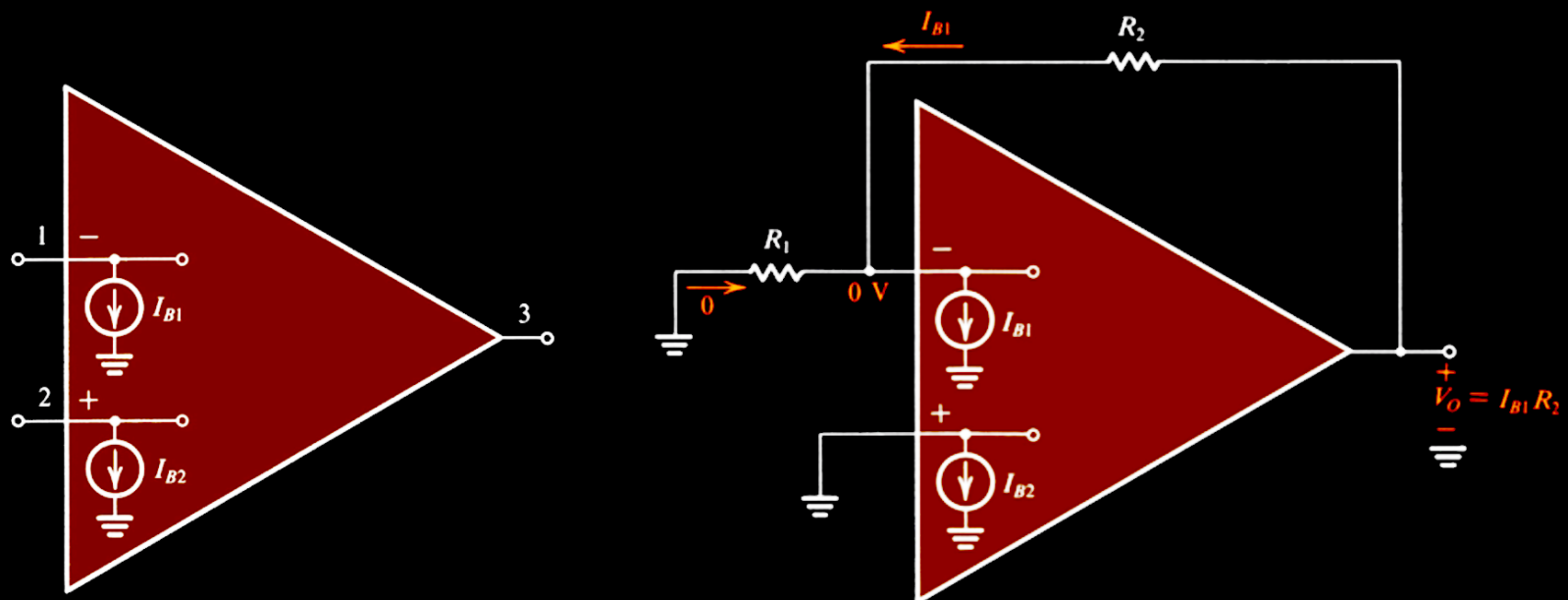
- ❑ A dc voltage $V_{OS}(1+R_2/R_1)$ exists at the output at zero input voltage
- ❑ Input offset voltage is effectively amplified by the closed-loop gain as the error voltage at output
- ❑ Some op amps are provided with two additional terminals for offset nulling

Input bias and offset current

- DC bias currents I_{B1} and I_{B2} are required for certain types of op amps
- Input bias current is defined by $I_B = (I_{B1} + I_{B2})/2$
- Input offset current is defined as $I_{OS} = |I_{B1} - I_{B2}|$
- Typical values for op amps that use bipolar transistors are $I_B = 100 \text{ nA}$ and $I_{OS} = 10 \text{ nA}$

Effect of input bias current for a closed-loop amplifiers

- Output dc voltage due to input bias current: $V_O = I_{B1}R_2 \cong I_B R_2$
- The value of R_2 and the closed-loop gain are limited.



Effect of input offset voltage on the the inverting integrator

- The output voltage is given by

$$v_o = V_{os} + \frac{1}{C} \int_0^t \frac{V_{os}}{R} dt = V_{os} + \frac{V_{os}}{RC} t$$

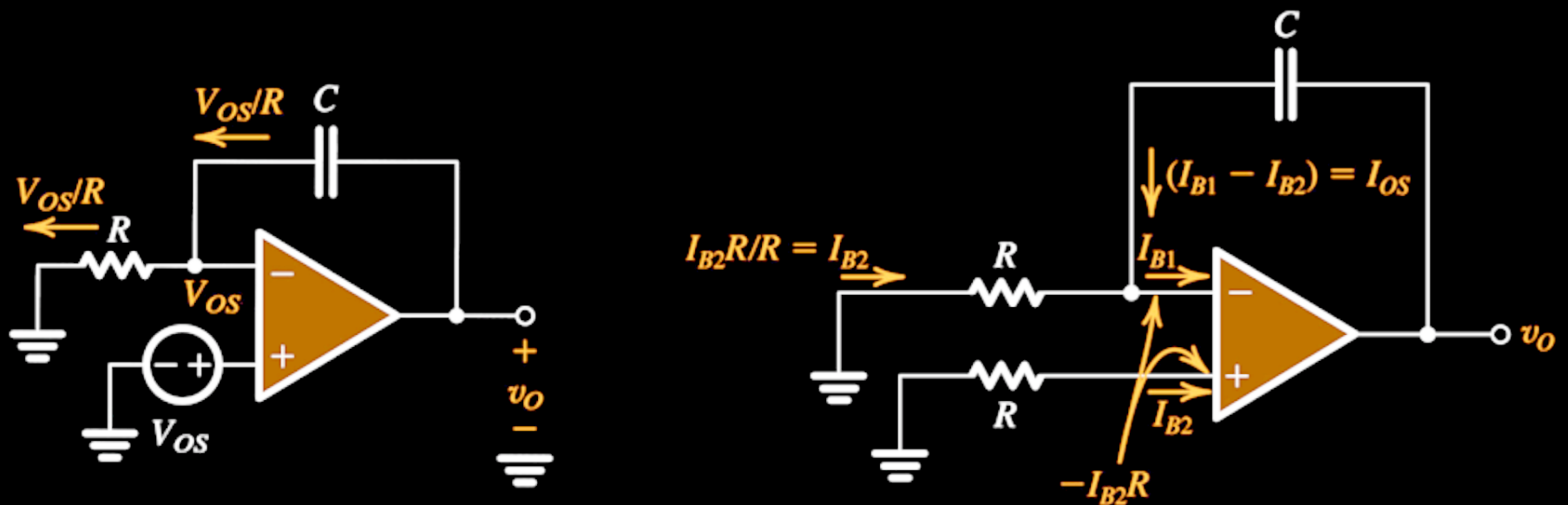
- The output voltage increases with time until the op amp saturates

Effect of input bias current on the inverting integrator

- The output voltage is given by

$$v_o = -I_{B2}R + \frac{1}{C} \int_0^t I_{os} dt = -I_{B2}R + \frac{I_{os}}{C} t$$

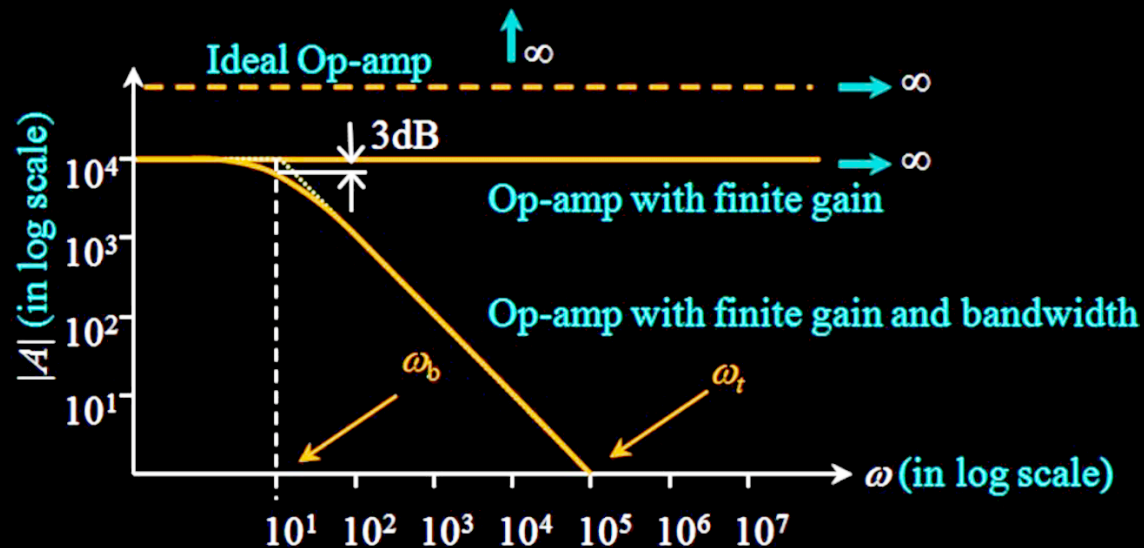
- The output voltage also increases with time until the op amp saturates



7. EFFECT OF FINITE OPEN-LOOP GAIN AND BANDWIDTH

Practical op-amp characteristics

- Op amp with finite open-loop gain: $A(j\omega) = A_o$
- Op amp with finite open-loop gain and bandwidth: $A(j\omega) = A_o/(1+j\omega/\omega_b)$
- Frequency response of op amp:



Open-loop op-amp

- The frequency response of an open-loop op amp is approximated by STC form:

$$A(j\omega) = A_o/(1+j\omega/\omega_b)$$

- At low frequencies ($\omega \ll \omega_b$), the open-loop op amp is approximated by $|A(j\omega)| \approx A_o$
- At high frequencies ($\omega \gg \omega_b$), the open-loop op amp is approximated by $|A(j\omega)| \approx \omega_b A_o/\omega$
- Unity-gain bandwidth ($f_t = \omega_t/2\pi$) is defined as the frequency at which $|A(j\omega_t)| \approx 1 \rightarrow \omega_t = A_o \omega_b$

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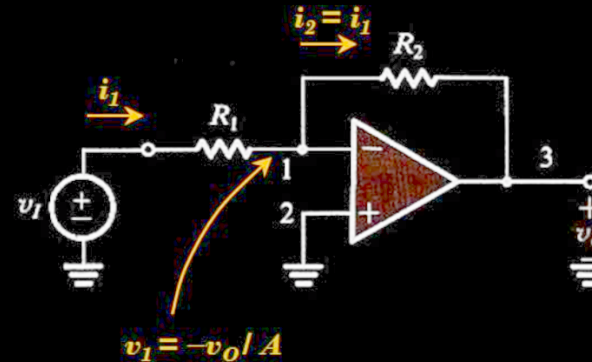
Inverting configuration using op-amp with finite open-loop gain

□ Closed-loop gain:

$$i_1 = \frac{v_I - (-v_O / A_0)}{R_1} = \frac{v_I + v_O / A_0}{R_1}$$

$$v_O = -\frac{v_O}{A_0} - i_1 R_2 = -\frac{v_O}{A_0} - \left(\frac{v_I + v_O / A_0}{R_1} \right) R_2$$

$$G \equiv \frac{v_O}{v_I} = \frac{-R_2 / R_1}{1 + (1 + R_2 / R_1) / A_0}$$



- Closed-loop gain approaches the ideal value of $-R_2/R_1$ as A_0 approaches to infinite
- To minimize the dependence of G on open-loop gain, we should have $A_0 \gg 1 + R_2/R_1$

□ Input impedance: $R_i = \frac{v_I}{i_1} = \frac{v_I}{(v_I + v_O / A_0) / R_1} = \frac{v_I}{(v_I + v_I G / A_0) / R_1} = \frac{R_1}{1 + G / A_0}$

□ Output impedance: $R_o = 0$

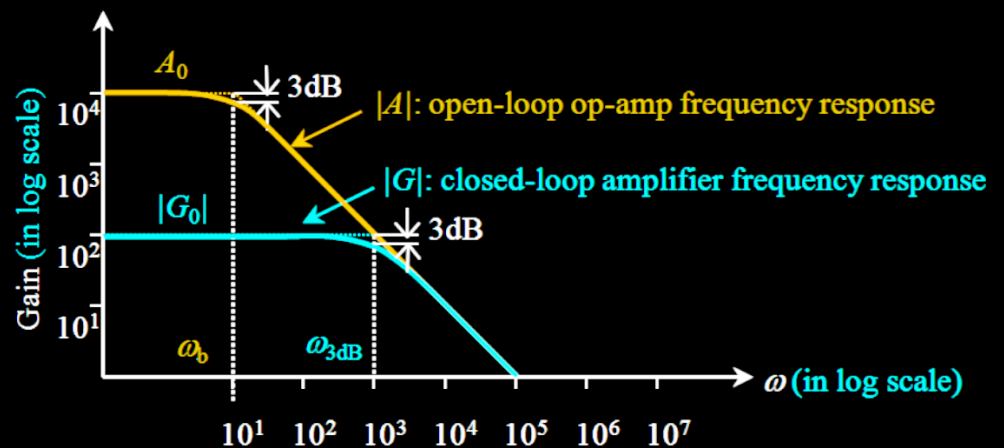
Inverting configuration using op amp with finite gain and bandwidth

$$G = \frac{-R_2 / R_1}{1 + (1 + R_2 / R_1) / A(j\omega)} = \frac{-R_2 / R_1}{1 + (1 + R_2 / R_1) [A_0 / (1 + j\omega / \omega_b)]}$$

$$= \frac{-R_2 / R_1}{[1 + (1 + R_2 / R_1) / A_0] + j[\omega(1 + R_2 / R_1) / \omega_b A_0]}$$

if $A_0 \gg 1 + R_2/R_1 \rightarrow G \approx G_0 / (1 + j\omega / \omega_{3dB})$

where $G_0 = -R_2/R_1$ and $\omega_{3dB} = A_0 \omega_b / (1 + R_2/R_1) \approx (A_0 / |G_0|) \omega_b$



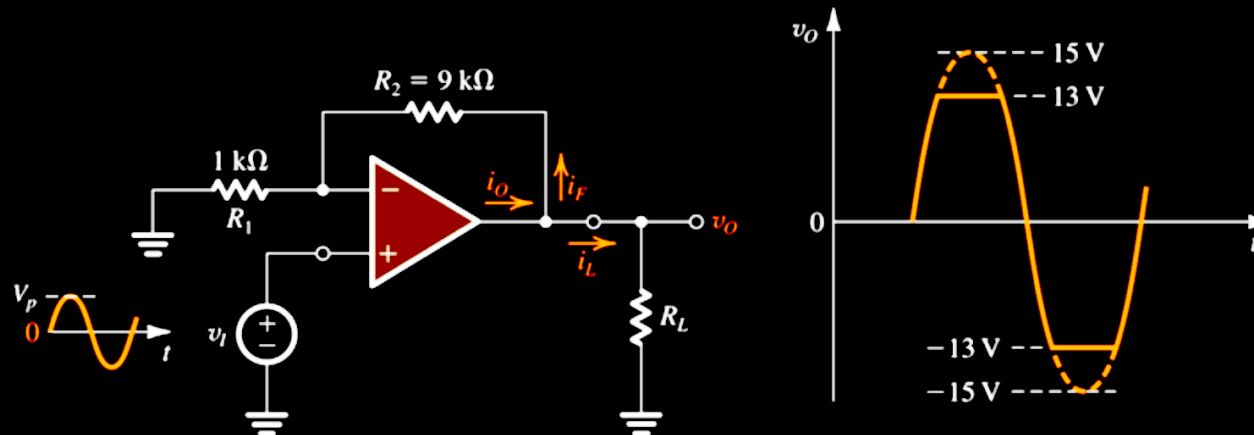
8. LARGE SIGNAL OPERATION BEHAVIOUR

Output voltage saturation

- ❑ Rated output voltage ($v_{O,max}$) specifies the maximum output voltage swing of op amp
- ❑ Linear amplifier operation (for the required $v_O < v_{O,max}$): $v_O = (1+R_2/R_1)v_I$
- ❑ Clipped output waveform (for the required $v_O > v_{O,max}$): $v_O = v_{O,max}$
- ❑ The maximum input swing allowed for output voltage limited case: $v_{I,max} = v_{O,max}/(1+R_2/R_1)$
- ❑ Output is typically limited by voltage in cases where R_L is large

Output current limits

- ❑ Maximum output current ($i_{O,max}$) specifies the output current limitation of op amp
- ❑ Linear amplifier operation (for the required $i_O < i_{O,max}$): $v_O = (1+R_2/R_1)v_I$ and $i_L = v_O/R_L$
- ❑ Clipped output waveform (for the required $i_O > i_{O,max}$): $i_L = i_{O,max} - i_F$
- ❑ The maximum input swing allowed for output current limited case:
$$v_{I,max} = i_{O,max}[R_L || (R_1+R_2)]/(1+R_2/R_1)$$
- ❑ Output is typically limited by current in cases where R_L is small

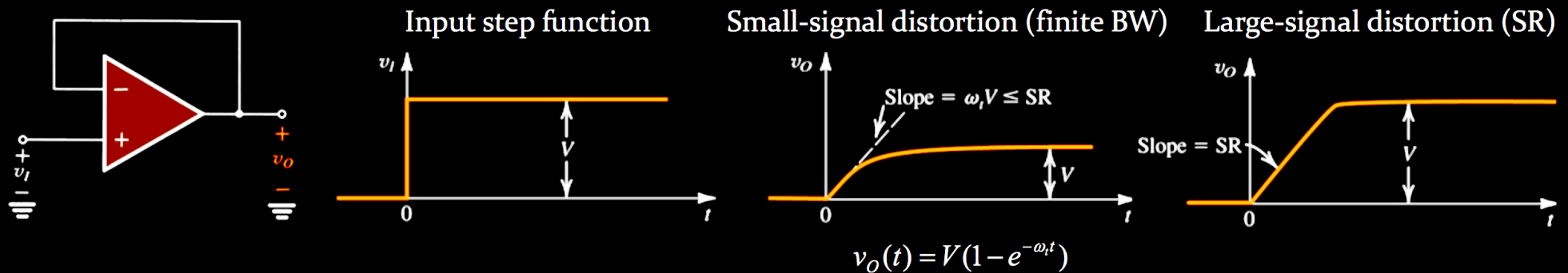


ESSENTIAL INSTRUMENTATION

AMPLIFIERS / REVISIONS

SLEW RATE

- ❑ Slew rate is the maximum rate of change possible at the output: $SR = \left. \frac{dv_o}{dt} \right|_{\max}$ (V/sec)
- ❑ Slew rate may cause non-linear distortion for large-signal operation



Full-power bandwidth

- ❑ Defined as the highest frequency allowed for a unity-gain buffer with a sinusoidal output at $v_{O,\max}$

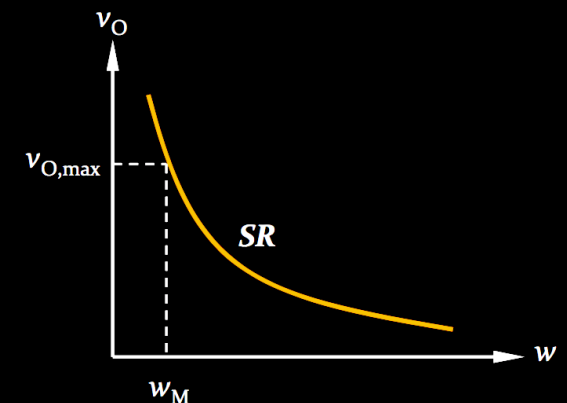
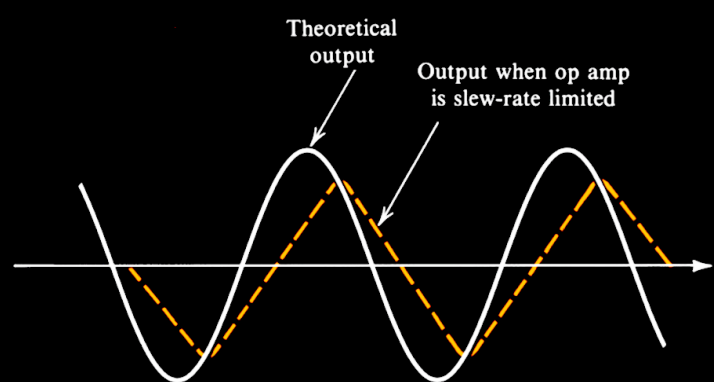
$$v_i(t) = V_o \sin \omega t \rightarrow v_o(t) = V_o \sin \omega t$$

$$\frac{dv_o(t)}{dt} = \omega V_o \cos \omega t$$

$$\left| \frac{dv_o(t)}{dt} \right|_{\max} = \omega V_o < SR \rightarrow \text{distortionless}$$

$$\left| \frac{dv_o(t)}{dt} \right|_{\max} = \omega V_o > SR \rightarrow \text{distortion}$$

$$f_M = \frac{\omega_M}{2\pi} = \frac{SR}{2\pi v_{O,\max}}$$



ESSENTIAL INSTRUMENTATION

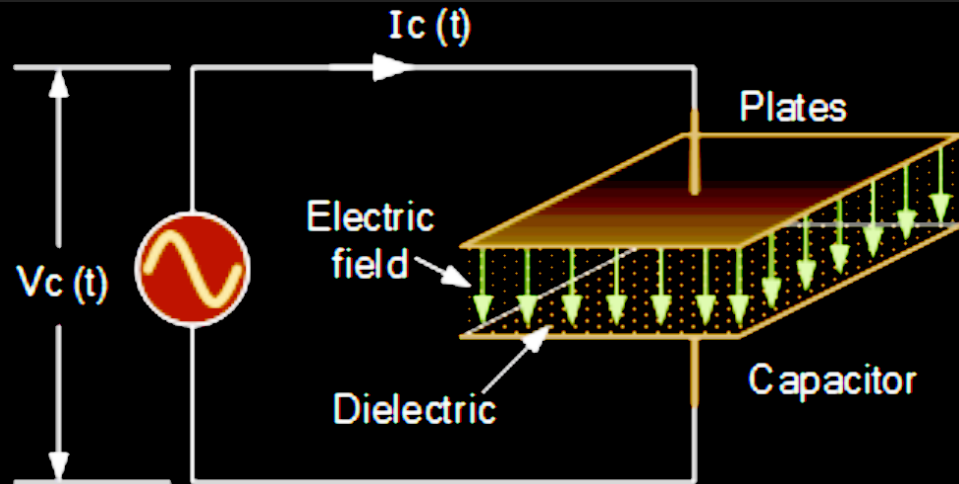
FILTERS

- 1 Capacitive Reactance
 - 2 The Passive Low Pass Filter
 - 3 The Passive High Pass Filter
 - 4 The Passive Band Pass Filter
 - 5 Active Filters
-

ESSENTIAL INSTRUMENTATION

FILTERS

1. CAPACITIVE REACTANCE



Capacitive Reactance X_c is the complex impedance of a capacitor whose value changes with respect to the applied frequency

$$X_c = \frac{1}{2\pi fC}$$

Capacitive Reactance against f

Capacitive Reactance Example No1

Calculate the capacitive reactance value of a 220nF capacitor at a frequency of 1kHz and again at a frequency of 20kHz.

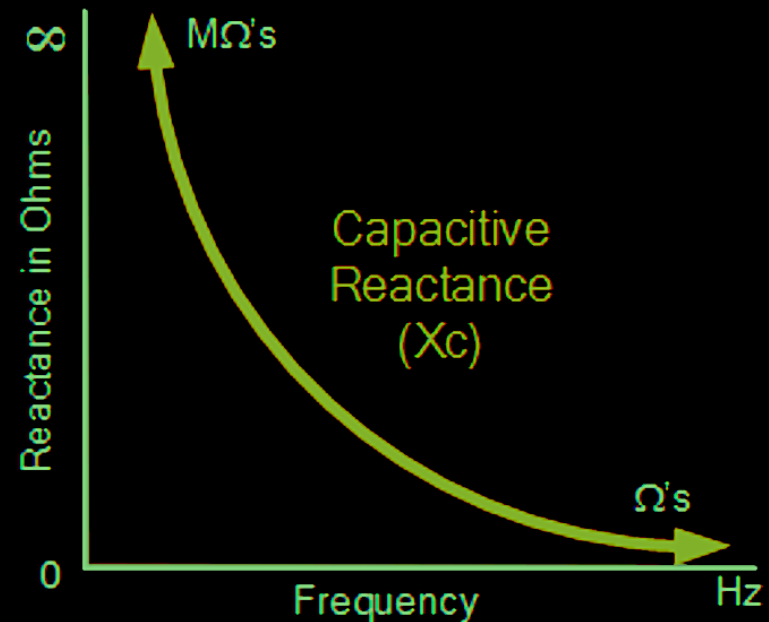
At a frequency of 1kHz:

$$X_c = \frac{1}{2\pi fC} = \frac{1}{2\pi \times 1000 \times 220 \times 10^{-9}} = 723.4\Omega$$

Again at a frequency of 20kHz:

$$X_c = \frac{1}{2\pi fC} = \frac{1}{2\pi \times 20000 \times 220 \times 10^{-9}} = 36.2\Omega$$

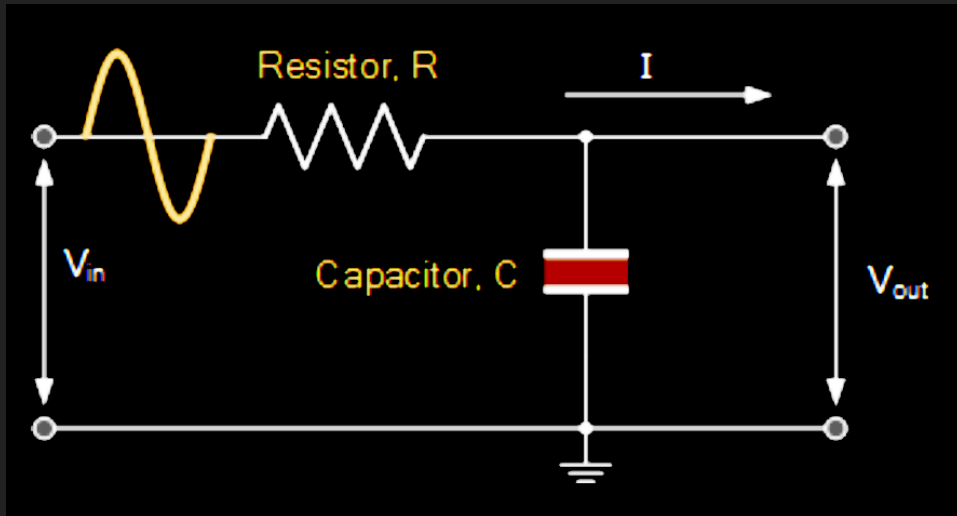
where: f = frequency in Hertz and C = capacitance in Farads



ESSENTIAL INSTRUMENTATION

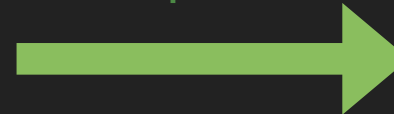
FILTERS

2. THE PASSIVE LOW PASS FILTER



A Low Pass Filter is a circuit that can be designed to modify, reshape or reject all unwanted high frequencies of an electrical signal and accept or pass only those signals wanted by the circuits designer

Z = impedance



$$V_{out} = V_{in} \times \frac{X_C}{\sqrt{R^2 + X_C^2}} = V_{in} \frac{X_C}{Z}$$

$$V_{out} = V_{in} \times \frac{R_2}{R_1 + R_2}$$

where: $R_1 + R_2 = R_T$, the total resistance of the circuit

+

$$Z = \sqrt{R^2 + X_C^2}$$

Low Pass Filter Example No1

A Low Pass Filter circuit consisting of a resistor of $4k7\Omega$ in series with a capacitor of $47nF$ is connected across a $10v$ sinusoidal supply. Calculate the output voltage (V_{OUT}) at a frequency of $100Hz$ and again at frequency of $10,000Hz$ or $10kHz$.

Voltage Output at a Frequency of 100Hz.

$$X_C = \frac{1}{2\pi f C} = \frac{1}{2\pi \times 100 \times 47 \times 10^{-9}} = 33,863\Omega$$

$$V_{OUT} = V_{IN} \times \frac{X_C}{\sqrt{R^2 + X_C^2}} = 10 \times \frac{33863}{\sqrt{4700^2 + 33863^2}} = 9.9v$$

Voltage Output at a Frequency of 10,000Hz (10kHz).

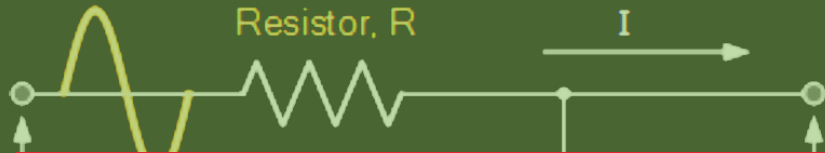
$$X_C = \frac{1}{2\pi f C} = \frac{1}{2\pi \times 10,000 \times 47 \times 10^{-9}} = 338.6\Omega$$

$$V_{OUT} = V_{IN} \times \frac{X_C}{\sqrt{R^2 + X_C^2}} = 10 \times \frac{338.6}{\sqrt{4700^2 + 338.6^2}} = 0.718v$$

ESSENTIAL INSTRUMENTATION

FILTERS

2. THE PASSIVE LOW PASS FILTER



“CUT-OFF”, “CORNER” OR “BREAKPOINT” FREQUENCY IS DEFINED AS BEING THE FREQUENCY POINT WHERE THE CAPACITIVE REACTANCE AND RESISTANCE ARE EQUAL,

Cut-off Frequency and Phase Shift

$$f_c = \frac{1}{2\pi RC}$$

$$\text{Phase Shift } \phi = -\arctan(2\pi fRC)$$

Low Pass Filter Example No1

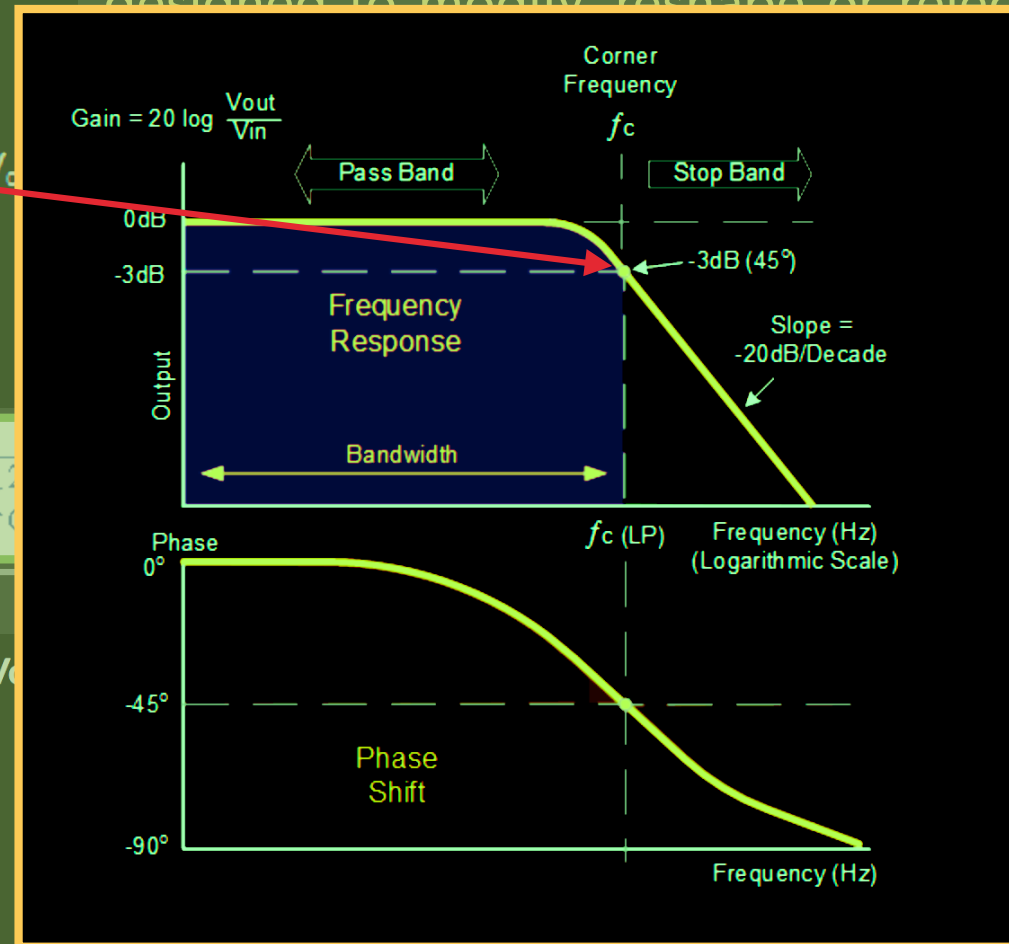
A Low Pass Filter circuit consisting of a resistor of $4k7\Omega$ in series with a capacitor of $47nF$ is connected across a $10v$ sinusoidal supply. Calculate the output voltage (V_{OUT}) at a frequency of $100Hz$ and again at frequency of $10,000Hz$ or $10kHz$.

Voltage Output at a Frequency of $100Hz$.

$$X_c = \frac{1}{2\pi f C} = \frac{1}{2\pi \times 100 \times 47 \times 10^{-9}} = 33,863\Omega$$

$$V_{OUT} = V_{IN} \times \frac{X_c}{\sqrt{R^2 + X_c^2}} = 10 \times \frac{33863}{\sqrt{4700^2 + 33863^2}} = 9.9v$$

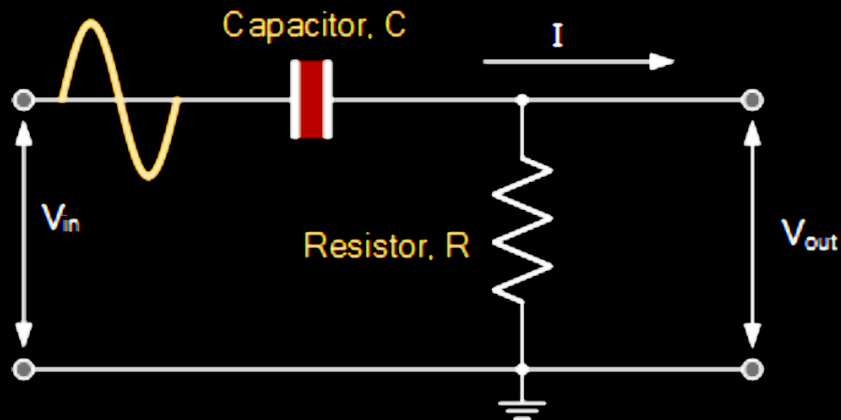
A Low Pass Filter is a circuit that can be designed to modify, reshape or reject all an only units



$$V_{OUT} = V_{IN} \times \frac{X_c}{\sqrt{R^2 + X_c^2}} = 10 \times \frac{338.0}{\sqrt{4700^2 + 338.6^2}} = 0.718v$$

FILTERS

3. THE PASSIVE HIGH PASS FILTER



A High Pass Filter is the exact opposite to the low pass filter circuit as the two components have been interchanged with the filters output signal now being taken from across the resistor

Frequency Response:

Cut-off Frequency and Phase Shift

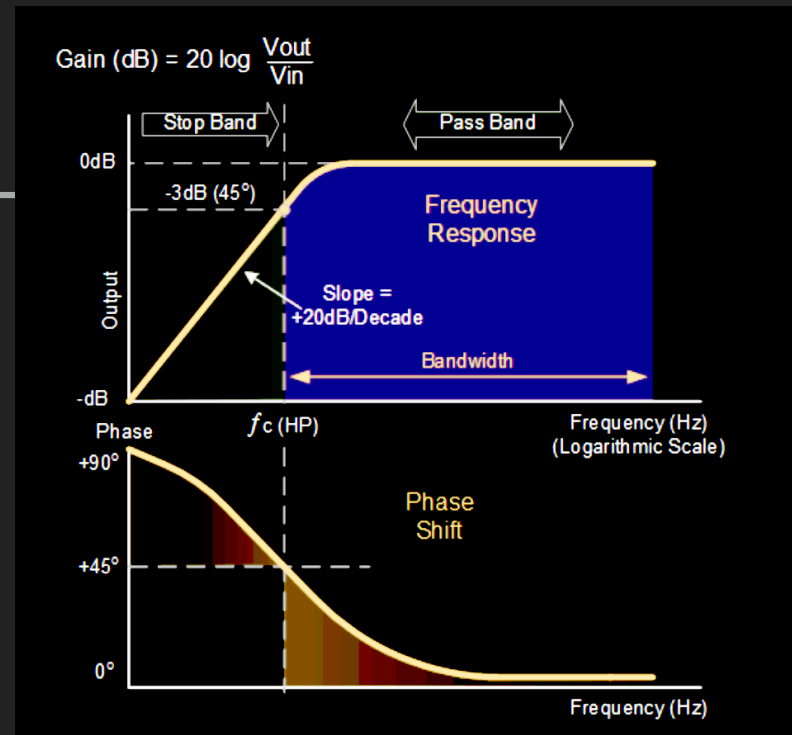
$$f_c = \frac{1}{2\pi RC}$$

$$\text{Phase Shift } \phi = \arctan \frac{1}{2\pi f RC}$$

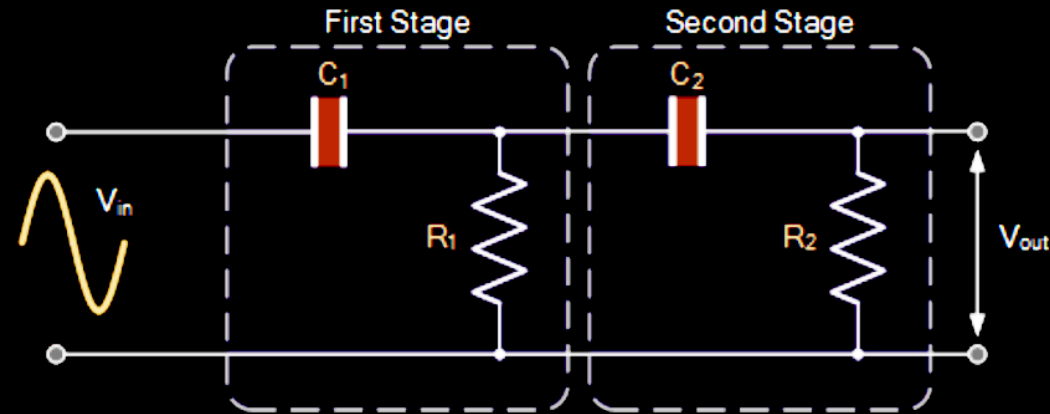
The circuit gain, A_v which is given as V_{out}/V_{in} (magnitude) and is calculated as:

$$A_v = \frac{V_{OUT}}{V_{IN}} = \frac{R}{\sqrt{R^2 + X_c^2}} = \frac{R}{Z}$$

at low f : $X_c \rightarrow \infty$, $V_{out} = 0$
 at high f : $X_c \rightarrow 0$, $V_{out} = V_{in}$



SECOND ORDER HIGH PASS FILTER



The above circuit uses two first-order filters connected or cascaded together to form a second-order or two-pole high pass network. Then a first-order filter stage can be converted into a second-order type by simply using an additional RC network, the same as for the 2nd-order low pass filter. The resulting second-order high pass filter circuit will have a slope of 40dB/decade (12dB/octave).

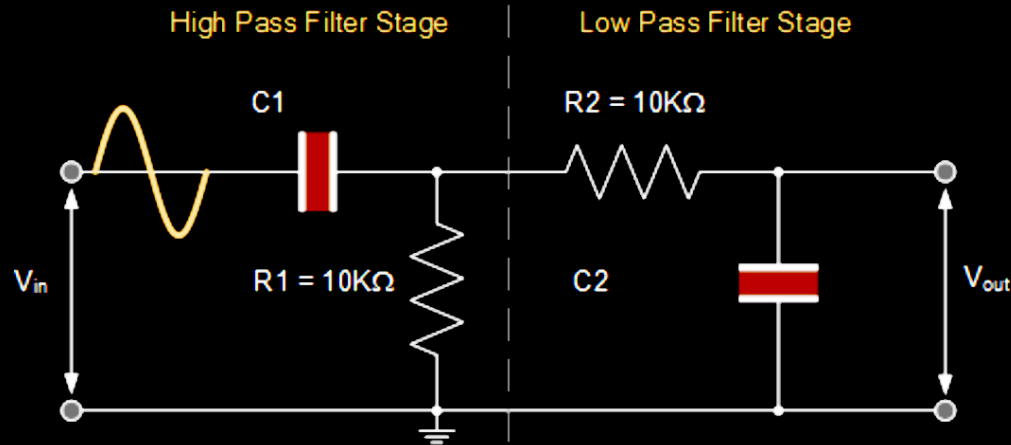
As with the low pass filter, the cut-off frequency, f_c is determined by both the resistors and capacitors as follows.

$$f_c = \frac{1}{2\pi\sqrt{R_1 C_1 R_2 C_2}} \text{ Hz}$$

ESSENTIAL INSTRUMENTATION

FILTERS

4. THE PASSIVE BAND PASS FILTER

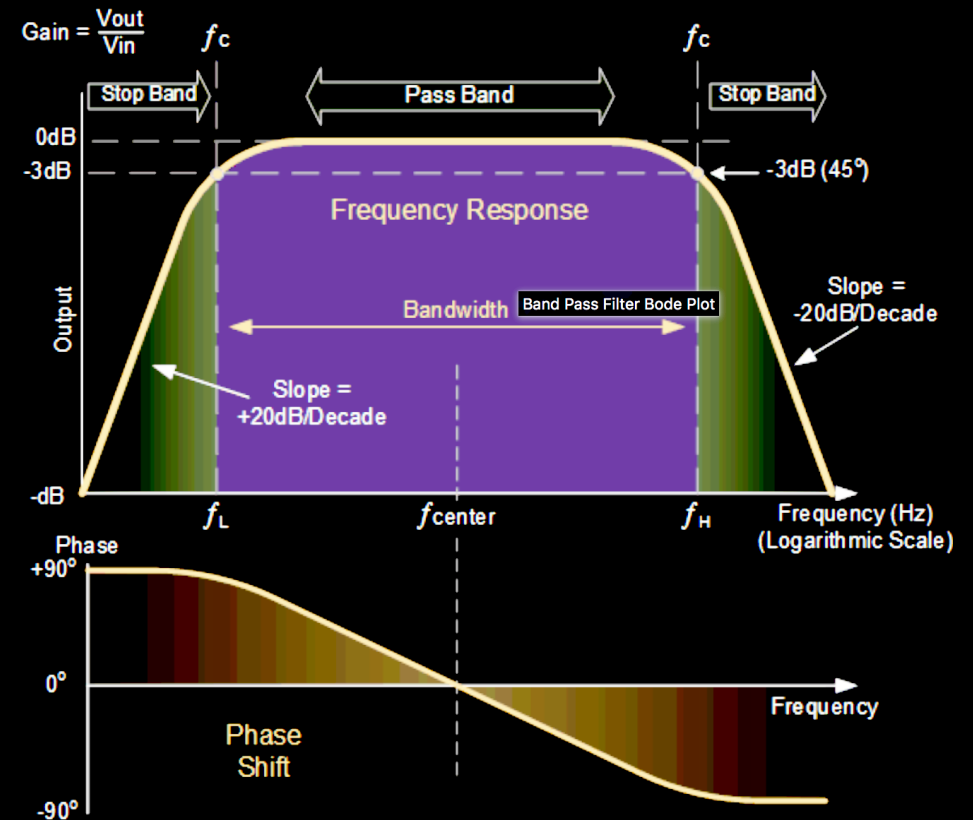


Passive Band Pass Filters can be made by connecting together a low pass filter with a high pass filter

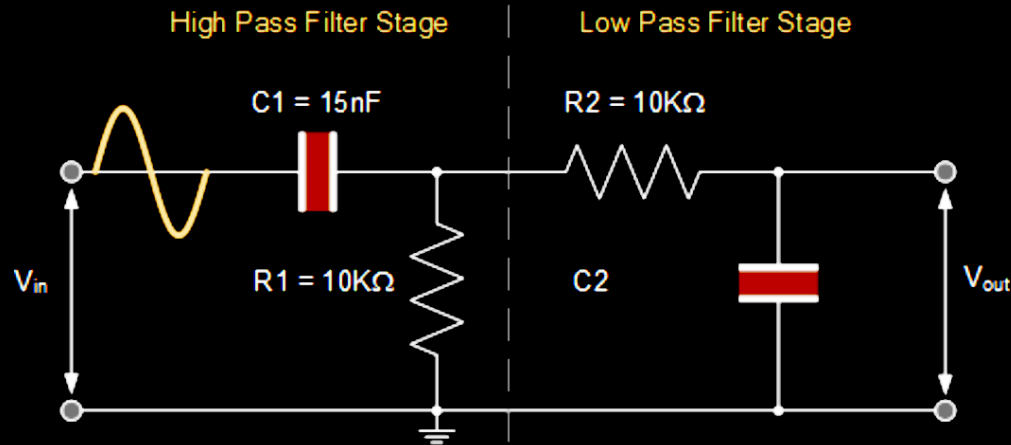
Frequency Response (2nd order):

Band Pass Filter Example No1.

A second-order band pass filter is to be constructed using RC components that will only allow a range of frequencies to pass above 1kHz (1,000Hz) and below 30kHz (30,000Hz). Assuming that both the resistors have values of $10\text{k}\Omega$, calculate the values of the two capacitors required.



4. THE PASSIVE BAND PASS FILTER



Step 1:

The High Pass Filter Stage

The value of the capacitor C_1 required to give a cut-off frequency f_L of 1kHz with a resistor value of $10\text{k}\Omega$ is calculated as:

$$C_1 = \frac{1}{2\pi f_L R} = \frac{1}{2\pi \times 1,000 \times 10,000} = 15.9\text{nF}$$

Then, the values of R_1 and C_1 required for the high pass stage to give a cut-off frequency of 1.0kHz are: $R_1 = 10\text{k}\Omega$ and to the nearest preferred value, $C_1 = 15\text{nF}$.

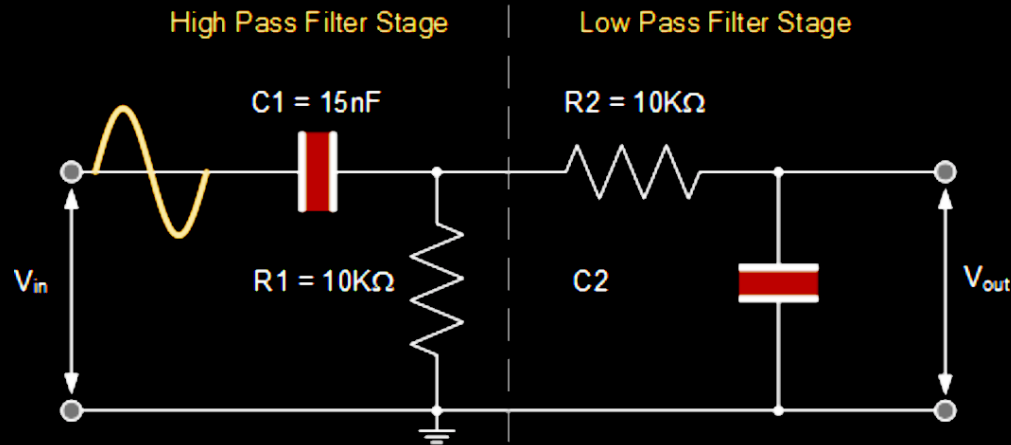
Band Pass Filter Example No1.

A second-order band pass filter is to be constructed using RC components that will only allow a range of frequencies to pass above 1kHz (1,000Hz) and below 30kHz (30,000Hz). Assuming that both the resistors have values of $10\text{k}\Omega$, calculate the values of the two capacitors required.

ESSENTIAL INSTRUMENTATION

FILTERS

4. THE PASSIVE BAND PASS FILTER



Step 1:

The High Pass Filter Stage

The value of the capacitor $C1$ required to give a cut-off frequency f_L of 1kHz with a resistor value of $10\text{k}\Omega$ is calculated as:

$$C_1 = \frac{1}{2\pi f_L R} = \frac{1}{2\pi \times 1,000 \times 10,000} = 15.9\text{nF}$$

Then, the values of $R1$ and $C1$ required for the high pass stage to give a cut-off frequency of 1.0kHz are: $R1 = 10\text{k}\Omega$ and to the nearest preferred value, $C1 = 15\text{nF}$.

Step 2:

The Low Pass Filter Stage

The value of the capacitor $C2$ required to give a cut-off frequency f_H of 30kHz with a resistor value of $10\text{k}\Omega$ is calculated as:

$$C_2 = \frac{1}{2\pi f_H R} = \frac{1}{2\pi \times 30,000 \times 10,000} = 530\text{pF}$$

Then, the values of $R2$ and $C2$ required for the low pass stage to give a cut-off frequency of 30kHz are, $R = 10\text{k}\Omega$ and $C = 530\text{pF}$. However, the nearest preferred value of the calculated capacitor value of 530pF is 560pF, so this is used instead.

With the values of both the resistances $R1$ and $R2$ given as $10\text{k}\Omega$, and the two values of the capacitors $C1$ and $C2$ found for both the high pass and low pass filters as 15nF and 560pF respectively, then the circuit for our simple passive **Band Pass Filter** is given as.

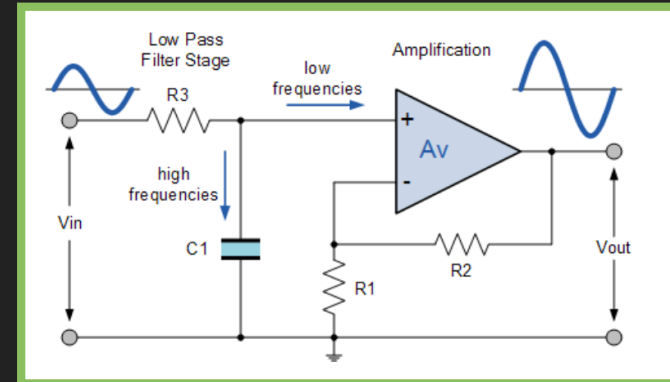
Band Pass Filter Example No1.

A second-order band pass filter is to be constructed using RC components that will only allow a range of frequencies to pass above 1kHz (1,000Hz) and below 30kHz (30,000Hz). Assuming that both the resistors have values of $10\text{k}\Omega$, calculate the values of the two capacitors required.

1-Active Low Pass Filter (1st order):

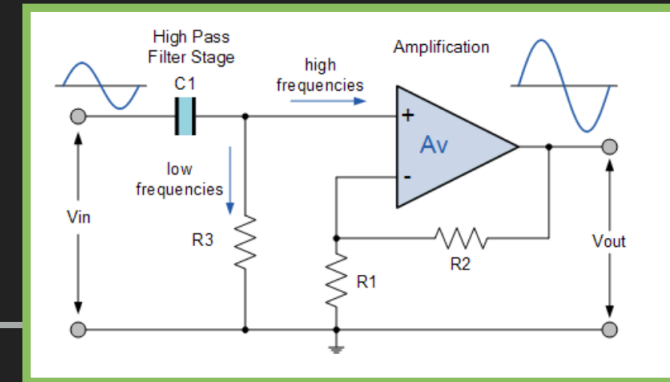
By combining a basic RC Low Pass Filter circuit with an operational amplifier we can create an Active Low Pass Filter circuit complete with amplification

- a) The frequency response of the circuit will be the same as that for the passive RC filter
- b) The DC gain will be: $(1+R_2/R_1)$



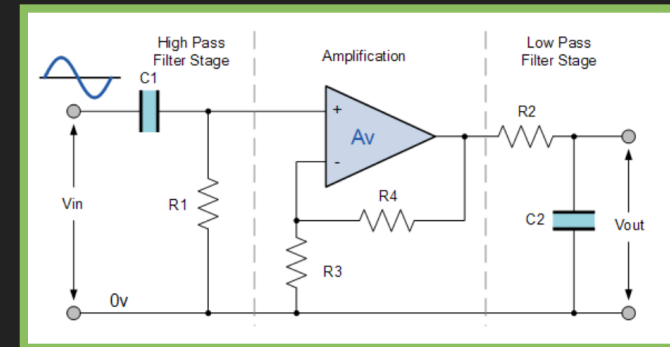
2-Active High Pass Filter (1st order):

An Active High Pass Filter can be created by combining a passive RC filter network with an operational amplifier to produce a high pass filter with amplification



3-Active Band Pass Filter (1st order):

The principal characteristic of a Band Pass Filter or any filter for that matter, is its ability to pass frequencies relatively unattenuated over a specified band or spread of frequencies called the "Pass Band".



Problem: draw for all circuits the output signal you would expect

**FOURIER
TRANSFORM
ANALYSIS**

FOURIER ANALYSIS

PARTICLE PHYSICS

Dilepton azimuthal correlations in $t\bar{t}$ production

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E-18071 Granada, Spain

Abstract

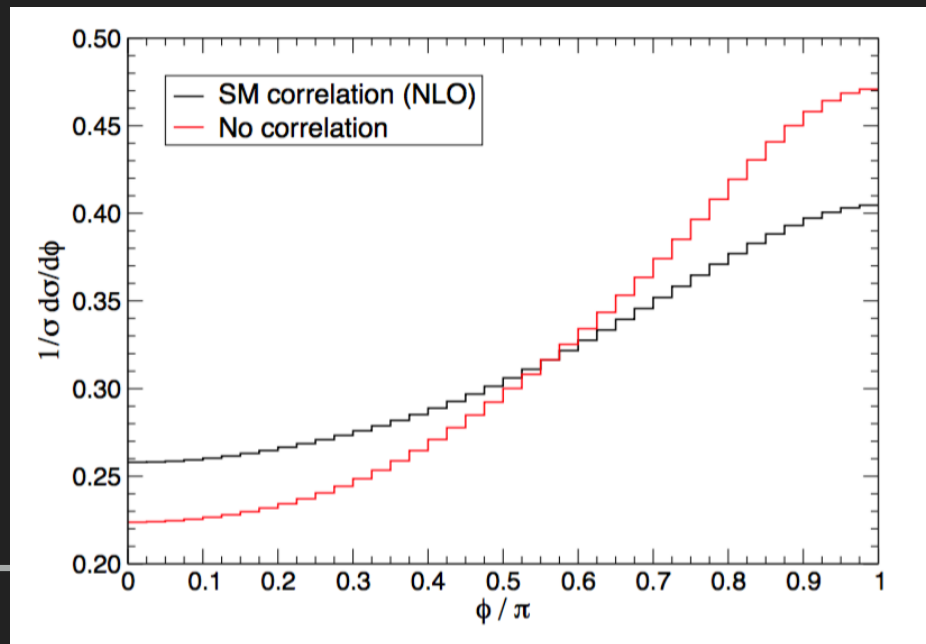
The dilepton azimuthal correlation, namely the difference ϕ between the azimuthal angles of the positive and negative charged lepton in the laboratory frame, provides a stringent test of the spin correlation in $t\bar{t}$ production at the Large Hadron Collider. We introduce a parameterisation of the differential cross section $d\sigma/d\phi$ in terms of a Fourier series and show that the third-order expansion provides a sufficiently accurate approximation. This expansion can be considered as a ‘bridge’ between theory and data, making it very simple to cast predictions in the Standard Model (SM) and beyond, and to report measurements, without the need to provide the numbers for the whole binned distribution. We show its application by giving predictions for the coefficients in the presence of (i) an anomalous top chromomagnetic dipole moment; (ii) an anomalous $t\bar{t}W$ interaction. The methods presented greatly facilitate the study of this angular distribution, which is of special interest given the $3.2(3.7)\sigma$ deviation from the SM next-to-leading order prediction found by the ATLAS Collaboration in Run 2 data.

1 Introduction

The production of $t\bar{t}$ pairs at the large hadron collider (LHC) provides a sensitive probe of the properties of the top quark, both in the production and the decay [1–3]. Among many observables investigated by the ATLAS and CMS Collaborations, the correlation between the spins of the top quark and anti-quark is particularly subtle and difficult to measure. It is well known that the Standard Model (SM) predicts a sizeable $t\bar{t}$ spin correlation [4–6]. The spins of t and \bar{t} are not directly measurable but, due to their short lifetime, they can be accessed through the angular distributions of their decay products. For the decay of a top quark $t \rightarrow W^+b$, $W^+ \rightarrow \ell^+\nu/\bar{d}u$, with $\ell = e, \mu, \tau$, the decay products have the angular distribution

$$\frac{1}{\Gamma} \frac{d\Gamma}{d\cos\theta_i} = \frac{1}{2} (1 + P\alpha_i \cos\theta_i), \quad (1)$$

ANGULAR DISTRIBUTION



$$g(\phi; f_{\text{SM}}) \equiv f_{\text{SM}} \left(\frac{1}{\sigma} \frac{d\sigma}{d\phi} \right)_{\text{SM}} + (1 - f_{\text{SM}}) \left(\frac{1}{\sigma} \frac{d\sigma}{d\phi} \right)_{\text{no corr}}.$$

	ATLAS	CMS
7 TeV	1.19 ± 0.09 (stat) ± 0.18 (sys) [18]	–
8 TeV	1.20 ± 0.05 (stat) ± 0.13 (sys) [19]	1.14 ± 0.06 (stat) $^{+0.15}_{-0.17}$ (sys) [13]
13 TeV	1.250 ± 0.026 (stat) ± 0.063 (sys) [20]	–

Table 2: Measurements of the best-fit parameter f_{SM} in (3) in the $t\bar{t}$ dilepton decay mode by the ATLAS and CMS Collaborations.

FOURIER ANALYSIS

PARTICLE PHYSICS

DECONSTRUCTING THE AZIMUTHAL DISTRIBUTION

The distribution $d\sigma/d\phi$ with $\phi = |\phi_{\ell^+} - \phi_{\ell^-}|$ is defined in the interval $[0, \pi]$. One may extend it to $[-\pi, \pi]$ by taking $\phi = \phi_{\ell^+} - \phi_{\ell^-}$, as some authors do, in which case it would be symmetric around zero in this interval. Therefore, the Fourier expansion of these distributions only contain cosines,

$$\frac{1}{\sigma} \frac{d\sigma}{d\phi} = a_0 + \sum_{n=1}^{\infty} a_n \cos n\phi. \quad (4)$$

MORE IMPORTANT AMPLITUDES THEN OTHERS:

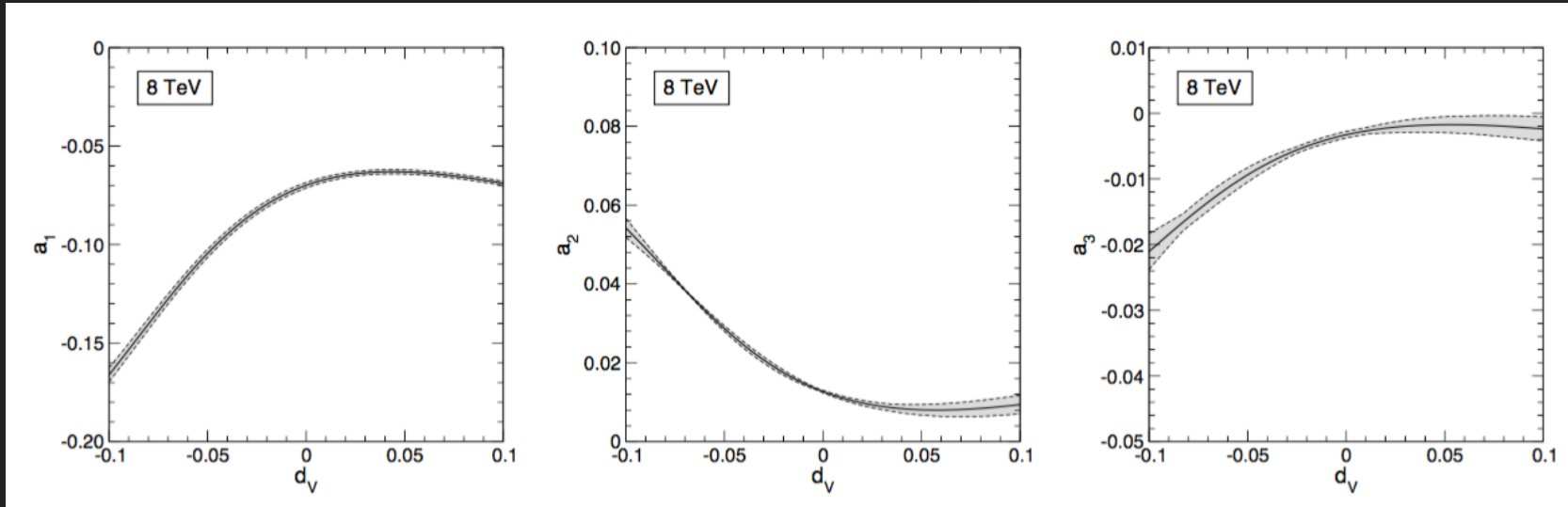
8 TeV	NLO	LO	Uncorrelated $t\bar{t}$
a_1	$-0.0699^{+0.0014}_{-0.0011}$	$-0.0762^{+0.0016}_{-0.0022}$	-0.1156 ± 0.0006
a_2	$0.0127^{+0.0003}_{-0.0002}$	$0.0121^{+0.0026}_{-0.0002}$	0.0256 ± 0.0003
a_3	$(-3.3 \pm 0.3) \times 10^{-3}$	$(-4.0 \pm 0.5) \times 10^{-3}$	-0.0071 ± 0.0007
a_4	$(5.3 \pm 8.4) \times 10^{-4}$	$(1.6 \pm 0.8) \times 10^{-3}$	0.0035 ± 0.0014

FOURIER ANALYSIS

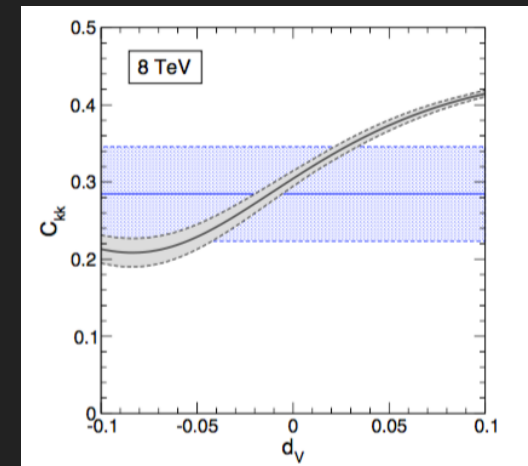
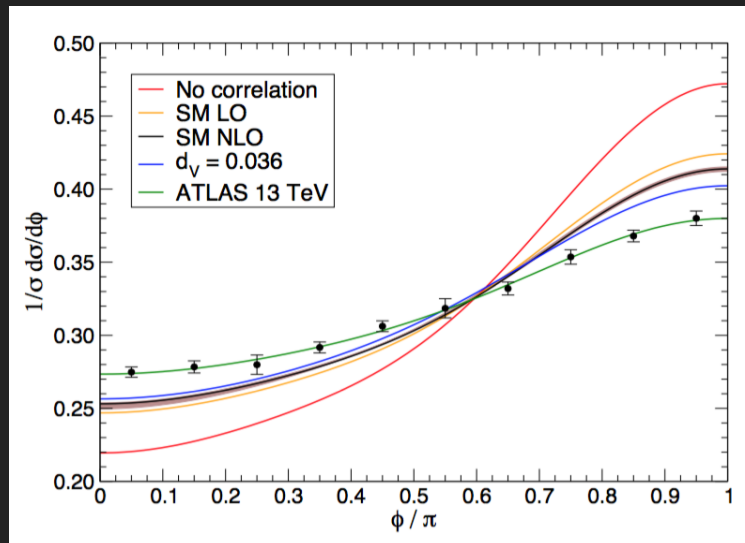
PARTICLE PHYSICS

DEPENDENCE WITH NEW PHYSICS

$$\mathcal{L}_{ttg} = -g_s \bar{t} \gamma^\mu \frac{\lambda^a}{2} t G_\mu^a - \frac{g_s}{m_t} \bar{t} \sigma^{\mu\nu} (d_V + i d_A \gamma_5) \frac{\lambda^a}{2} t G_{\mu\nu}^a$$



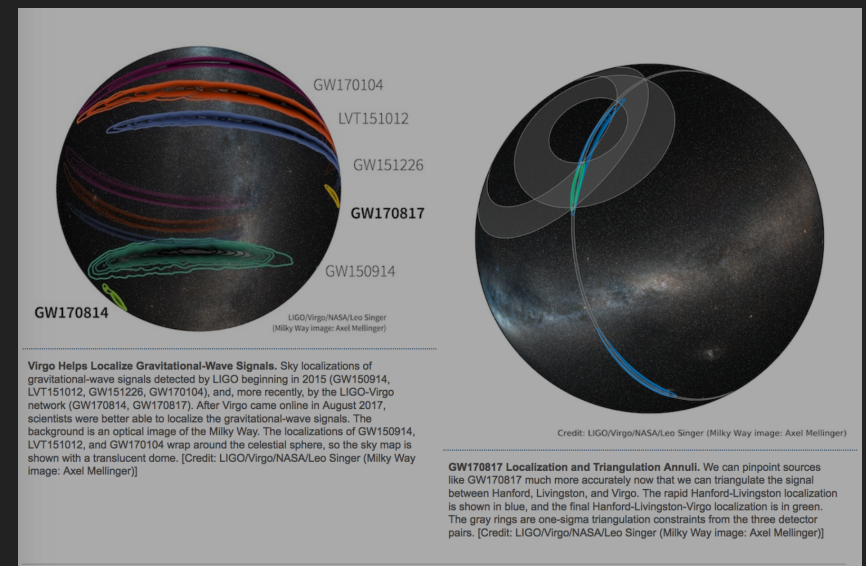
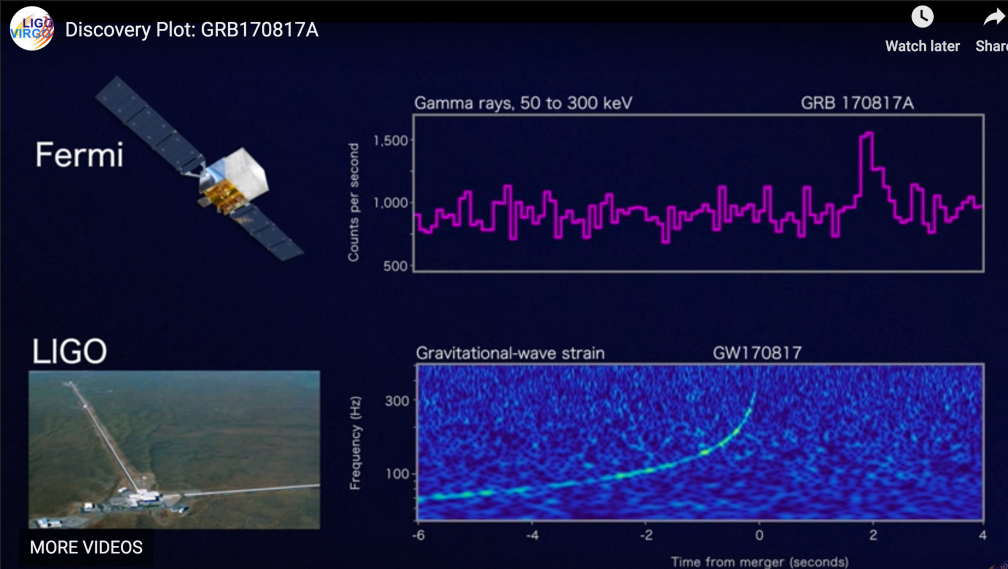
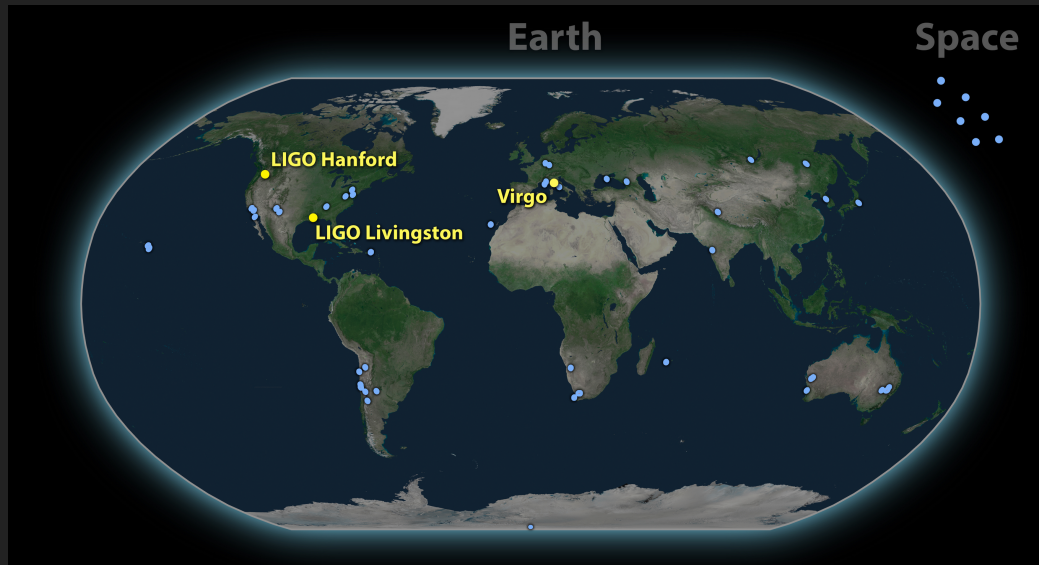
TYPE OF RESULTS:



FOURIER ANALYSIS

ASTROPHYSICS

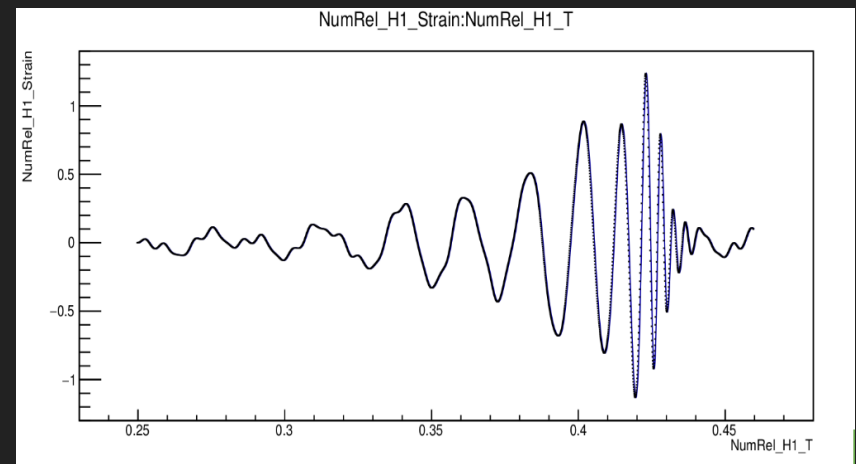
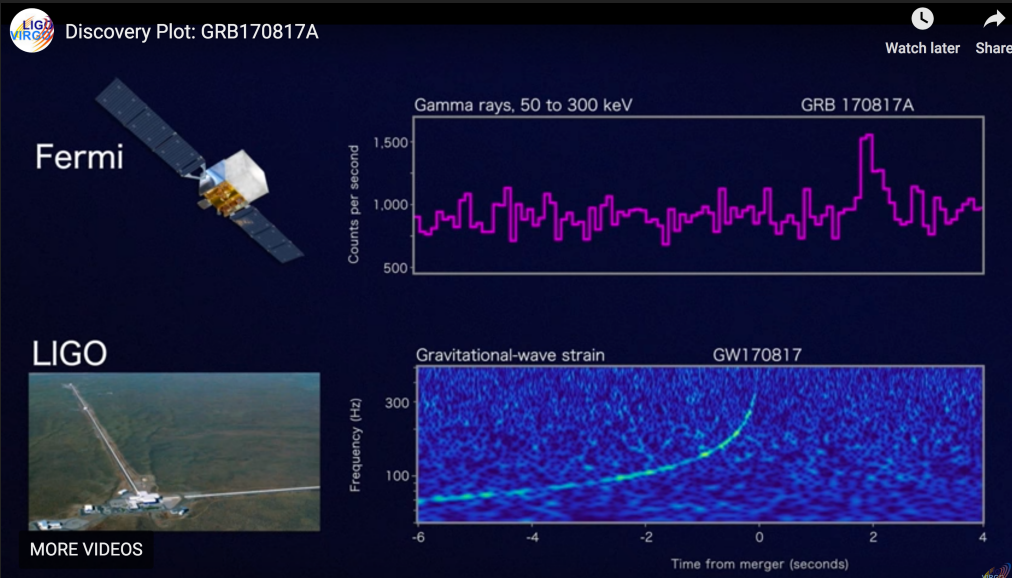
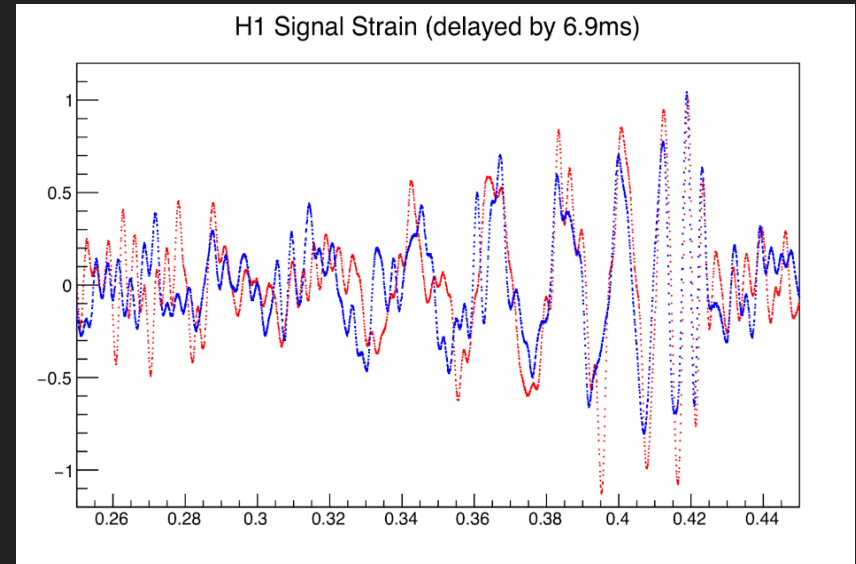
GRAVITATIONAL WAVES



FOURIER ANALYSIS

ASTROPHYSICS

GRAVITATIONAL WAVES



FOURIER ANALYSIS

TOOLS AVAILABLE: ROOT (THERE ARE MORE)

<https://root.cern.ch/building-root>



ROOT
Data Analysis Framework

Menu ▾

[Home](#) » [Documentation](#)

Building ROOT

Introduction

ROOT uses the [CMake](#) [🔗] cross-platform build-generator tool as a primary build system. CMake does not build the project, it generates the files needed by your build tool (GNU make, Ninja, Visual Studio, etc) for building ROOT. The classic build with configure/make is still available but it will not be evolving with the new features of ROOT. The instructions can be found [here](#).

If you are really anxious about getting a functional ROOT build, go to the [Quick Start](#) section. If you are a CMake novice, start on [Basic](#) CMake usage and then go back to the [Quick Start](#) once you know what you are doing. The [Options](#) and [Variables](#) section is a reference for customizing your build. If you already have experience with CMake, this is the recommended starting point.

Preparation

Check the [prerequisites](#) and [supported platforms](#) for the list of packages needed for your setup before starting the build.

Quick Start

The following are the basic instructions for UNIX systems. We use here the command-line, non-interactive CMake interface.

1. Download and unpack the ROOT's sources from the download area or using directly the Git repository. Follow the [instructions for getting the ROOT sources](#)
2. Open a shell. Your development tools must be reachable from this shell through the PATH environment variable.
3. Create a directory for containing the build. It is not supported to build ROOT on the source directory. cd to this directory:

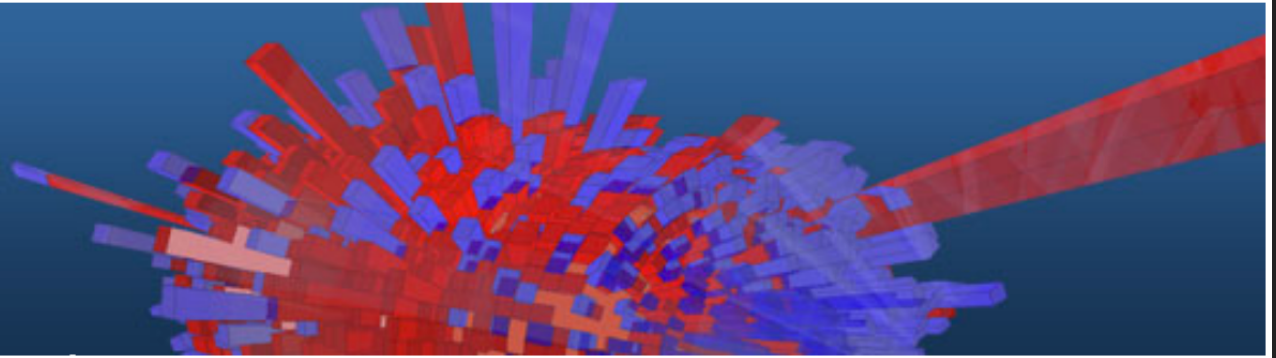
FOURIER ANALYSIS

TOOLS AVAILABLE: **ROOT** (THERE ARE MORE)

<https://root.cern.ch/building-root>



ROOT
Data Analysis Framework



^ Fast Fourier Transforms

FFT.C: This tutorial illustrates the Fast Fourier Transforms interface in ROOT.

From `$ROOTSYS/tutorials/fft/FFT.C`

```
1 #include "TH1D.h"
2 #include "TVirtualFFT.h"
3 #include "TF1.h"
4 #include "TCanvas.h"
5 #include "TMath.h"
6
7 void FFT()
8 {
9
10 //This tutorial illustrates the Fast Fourier Transforms interface in ROOT.
11 //FFT transform types provided in ROOT:
12 // - "C2CFORWARD" - a complex input/output discrete Fourier transform (DFT)
13 //                 in one or more dimensions, -1 in the exponent
14 // - "C2CBACKWARD" - a complex input/output discrete Fourier transform (DFT)
15 //                 in one or more dimensions, +1 in the exponent
16 // - "R2C"         - a real-input/complex-output discrete Fourier transform (DFT)
17 //                 in one or more dimensions,
18 // - "C2R"         - inverse transforms to "R2C", taking complex input
19 //                 (storing the non-redundant half of a logically Hermitian array)
20 //                 to real output
21 // - "R2HC"       - a real-input DFT with output in  $\hat{A}i\tilde{A}^{\text{halfcomplex}}\hat{A}i\tilde{A}$  format.
```

FOURIER ANALYSIS

- 1 General Introduction
 - 2 Orthogonality of Functions
 - 3 Determining the Parameters
 - 4 Example
-

FOURIER ANALYSIS

Consider a function $f(\tau)$ that is periodic with period T .

$$f(\tau + T) = f(\tau) \quad (1)$$

We may always rescale τ to make the function 2π periodic. To do so, define a new independent variable $t = \frac{2\pi}{T}\tau$, so that

$$f(t + 2\pi) = f(t) \quad (2)$$

So let us consider the set of all sufficiently nice functions $f(t)$ of a real variable t that are periodic, with period 2π . Since the function is periodic we only need to consider its behavior on one interval of length 2π , e.g. on the interval $(-\pi, \pi)$.

The idea is to decompose any such function $f(t)$ into an infinite sum, or series, of simpler functions. Following Joseph Fourier (1768-1830) consider the infinite sum of sine and cosine functions

$$f(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} [a_n \cos(nt) + b_n \sin(nt)] \quad (3)$$

where the constant coefficients a_n and b_n are called the Fourier coefficients of f . The first question one would like to answer is how to find those coefficients.

FOURIER ANALYSIS

2 ORTHOGONALITY OF FUNCTIONS

To do so we utilize the **orthogonality** of sine and cosine functions:

$$\begin{aligned}\int_{-\pi}^{\pi} \cos(nt) \cos(mt) dt &= \int_{-\pi}^{\pi} \frac{1}{2} [\cos((m-n)t) + \cos((m+n)t)] dt \\ &= \begin{cases} 2\pi, & m = n = 0 \\ \pi, & m = n \neq 0 \\ 0, & m \neq n \end{cases} \\ &= \begin{cases} 2\pi, & m = n = 0 \\ \pi\delta_{mn}, & m \neq 0 \end{cases} \end{aligned} \quad (4)$$

Similarly,

$$\begin{aligned}\int_{-\pi}^{\pi} \sin(nt) \sin(mt) dt &= \int_{-\pi}^{\pi} \frac{1}{2} [\cos((m-n)t) - \cos((m+n)t)] dt \\ &= \begin{cases} 0 & m = 0 \\ \pi\delta_{mn} & m \neq 0 \end{cases} \end{aligned} \quad (5)$$

and

$$\begin{aligned}\int_{-\pi}^{\pi} \sin(nt) \cos(mt) dt &= \int_{-\pi}^{\pi} \frac{1}{2} [\sin((m-n)t) + \sin((m+n)t)] dt \\ &= 0 \end{aligned} \quad (6)$$

FOURIER ANALYSIS

3 DETERMINING THE PARAMETERS

Using the orthogonality and the assumed expression for the infinite series given in Eq. (3), it follows that the Fourier coefficients are

$$a_n = \frac{1}{\pi} \int_{-\pi}^{\pi} f(t) \cos(nt) dt \quad (7)$$

$$b_n = \frac{1}{\pi} \int_{-\pi}^{\pi} f(t) \sin(nt) dt \quad (8)$$

When determining a the Fourier series of a periodic function $f(t)$ with period T , any interval $(t_0, t_0 + T)$ can be used, with the choice being one of convenience or personal preference. For example, in the rescaled time coordinates considering the interval $(0, 2\pi)$ works just as well as considering $(-\pi, \pi)$ as we have done.

If a function is even so that $f(t) = f(-t)$, then $f(t) \sin(nt)$ is odd. (This follows since $\sin(nt)$ is odd and an even function times an odd function is an odd function.) Therefore, $b_n = 0$ for all n . Similarly, if a function is odd so that $f(t) = -f(-t)$, then $f(t) \cos(nt)$ is odd. (This follows since $\cos(nt)$ is even and an even function times an odd function is an odd function.) Therefore, $a_n = 0$ for all n .

FOURIER ANALYSIS

4 EXAMPLE

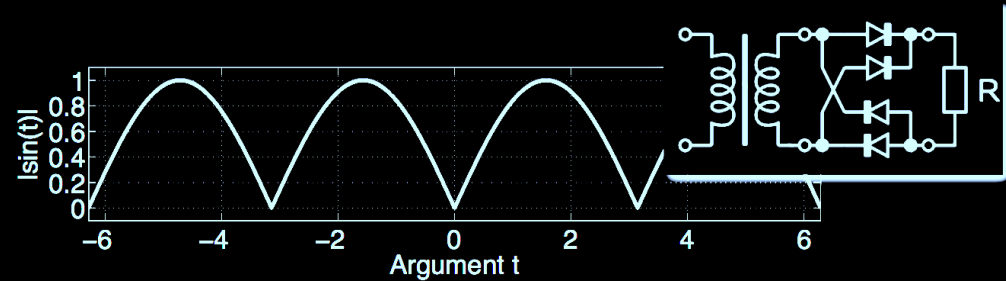


Figure 1: A full-wave-rectifier converts a sinusoidal input, $\sin(\omega t)$, to $|\sin(\omega t)|$.

Example - Rectified sine wave: A first step in converting AC-power from the power-grid to the DC-power that most devices need is to utilize a full-wave rectifier, such as the diode bridge shown in Fig. 1, which converts a sinusoidal input to an output that is the absolute value of the input sine-wave.

Since the output $f = |\sin(\omega t)|$ is even, *i.e.* $f(t) = f(-t)$, no terms of the form $\sin(n\omega t)$ will appear in the answer. It suffices to determine the a_n coefficients. For a_0 one obtains

$$\begin{aligned} a_0 &= \frac{1}{\pi} \int_{-\pi}^0 -\sin(\omega t) d(\omega t) + \frac{1}{\pi} \int_0^{\pi} \sin(\omega t) d(\omega t) \\ &= \frac{2}{\pi} \int_0^{\pi} \sin(\omega t) d(\omega t) = \frac{4}{\pi} \end{aligned} \quad (9)$$

FOURIER ANALYSIS

4 EXAMPLE

and for the remaining a_n one gets

$$\begin{aligned}
 a_n &= \frac{2}{\pi} \int_0^\pi \sin(\omega t) \cos(n\omega t) d(\omega t) \\
 &= \frac{2}{\pi} \int_0^\pi \frac{1}{2} [-\sin((n-1)\omega t) + \sin((n+1)\omega t)] d(\omega t) \\
 &= \frac{1}{\pi} \left[\frac{1}{n-1} \{\cos(n\pi - \pi) - 1\} + \frac{-1}{n+1} \{\cos(n\pi + \pi) - 1\} \right] \\
 &= \begin{cases} -\frac{4}{\pi} \frac{1}{n^2-1}, & n \text{ even} \\ 0, & n \text{ odd.} \end{cases} \quad (10)
 \end{aligned}$$

Note, that the sine and cosine functions are orthogonal on the interval $(-\pi, \pi)$. They are not orthogonal on the interval $(0, \pi)$ and we do get a nonzero contribution for even n . To summarize the result,

$$|\sin(\omega t)| = \frac{2}{\pi} - \frac{4}{\pi} \sum_{n=2,4,6,\dots}^{\infty} \frac{\cos(n\omega t)}{n^2-1}. \quad (11)$$

For an input with frequency f_0 , the output has a DC-offset, the part that we really care about when building a DC-voltage supply. It has *no contribution* at $f = f_0$. It does have contributions at frequencies $2f_0, 4f_0, 6f_0, \dots$

FOURIER ANALYSIS

PROBLEM 1

Show that for a real and periodic signal $x(t)$, we have

$$x_e(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos\left(2\pi \frac{n}{T_0} t\right),$$
$$x_o(t) = \sum_{n=1}^{\infty} b_n \sin\left(2\pi \frac{n}{T_0} t\right),$$

where $x_e(t)$ and $x_o(t)$ are the *even and odd parts* of $x(t)$, defined as

$$x_e(t) = \frac{x(t) + x(-t)}{2},$$
$$x_o(t) = \frac{x(t) - x(-t)}{2}.$$

PROBLEM 2

Calculate the Fourier transform of the following functions:

- 1) $f(t) = \sin^2(\omega t)$
- 2) $f(t) = 1 - 2\cos(\omega t)$
- 3) $f(t) = 2 - 2\cos(\omega t) \sin(\omega t)$

COMPLEX FOURIER ANALYSIS

At this stage in your physics career you are all well acquainted with complex numbers and functions. Let us then generalize the Fourier series to complex functions. To motivate this, return to the Fourier series, Eq. (3):

$$\begin{aligned} f(t) &= \frac{a_0}{2} + \sum_{n=1}^{\infty} [a_n \cos(nt) + b_n \sin(nt)] \\ &= \frac{a_0}{2} + \sum_{n=1}^{\infty} \left[a_n \frac{e^{int} + e^{-int}}{2} + b_n \frac{e^{int} - e^{-int}}{2i} \right] \\ &= \frac{a_0}{2} + \sum_{n=1}^{\infty} \frac{a_n - ib_n}{2} e^{int} + \sum_{m=-1}^{-\infty} \frac{a_{-m} + ib_{-m}}{2} e^{imt} \end{aligned} \quad (13)$$

where we substituted $m = -n$ in the last term on the last line. Equation (13) clearly suggests the much simpler complex form of the Fourier series

$$x(t) = \sum_{n=-\infty}^{+\infty} X_n e^{in(2\pi f_0)t}. \quad (14)$$

with the coefficients given by

$$X_n = \frac{1}{T} \int_{-T/2}^{T/2} x(t) e^{-in(2\pi f_0)t} dt \quad (15)$$

COMPLEX FOURIER ANALYSIS

$$x(t) = \sum_{n=-\infty}^{+\infty} X_n e^{in(2\pi f_0)t}. \quad (14)$$

with the coefficients given by

$$X_n = \frac{1}{T} \int_{-T/2}^{T/2} x(t) e^{-in(2\pi f_0)t} dt \quad (15)$$

Here, the Fourier series is written for a complex periodic function $x(t)$ with arbitrary period $T = 1/f_0$. Note that the Fourier coefficients X_n are complex valued. It is seen from Eq. (13) that for a real-valued function $x(t)$ in Eq. (14) the following holds for the complex coefficients X_n

$$X_n = X_{-n}^* \quad (16)$$

where * denotes the complex conjugate.

COMPLEX FOURIER ANALYSIS

Box Function: Consider the Fourier transform of a box-function

$$b_T(t) = \begin{cases} 1 & t \in [-T/2, T/2] \\ 0 & \text{otherwise} \end{cases} \quad (33)$$

$$\begin{aligned} \hat{b}_T(f) &= \int_{-T/2}^{+T/2} e^{-i2\pi ft} dt \\ &= \frac{e^{-i\pi fT} - e^{i\pi fT}}{-2\pi i f} \\ &= T \frac{\sin(\pi fT)}{\pi fT} = T \operatorname{sinc}(\pi fT) \end{aligned} \quad (34)$$

The result is shown in Fig. 3. In physical optics the diffraction pattern amplitude is described by the Fourier transform of the diffracting element. A slit is described by the box function $b_a(x)$ and therefore the diffraction pattern by $\hat{b}_T(k)$.

ESSENTIAL INSTRUMENTATION

COMPLEX FOURIER ANALYSIS

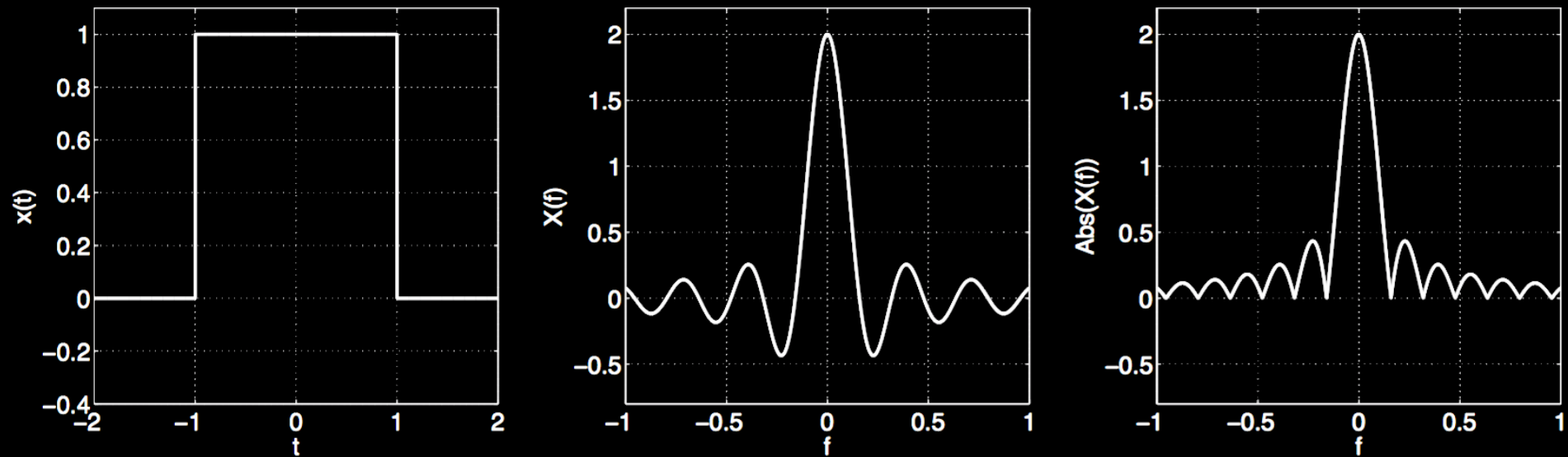


Figure 3: Box function and its Fourier transform

ESSENTIAL INSTRUMENTATION

ANALOG-TO-DIGITAL & DIGITAL-TO-ANALOG CONVERTERS

1 Introduction

2 DACs

3 ADCs

ESSENTIAL INSTRUMENTATION

1. INTRODUCTION

We live in an analog world

Everything in the physical world is an analog signal
Sound, light, temperature, pressure

Need to convert into electrical signals

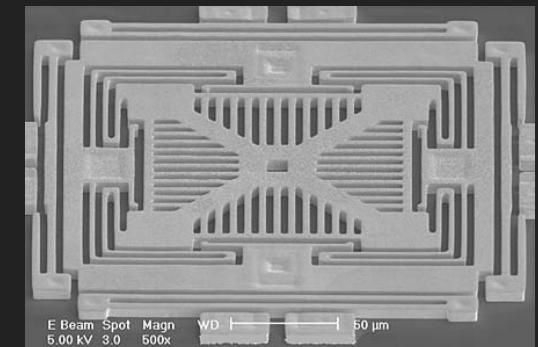
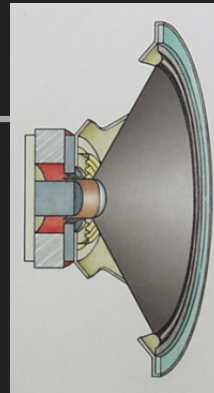
Transducers: converts one type of energy to another
Electro-mechanical, Photonic, Electrical, ...

Examples

Microphone/speaker

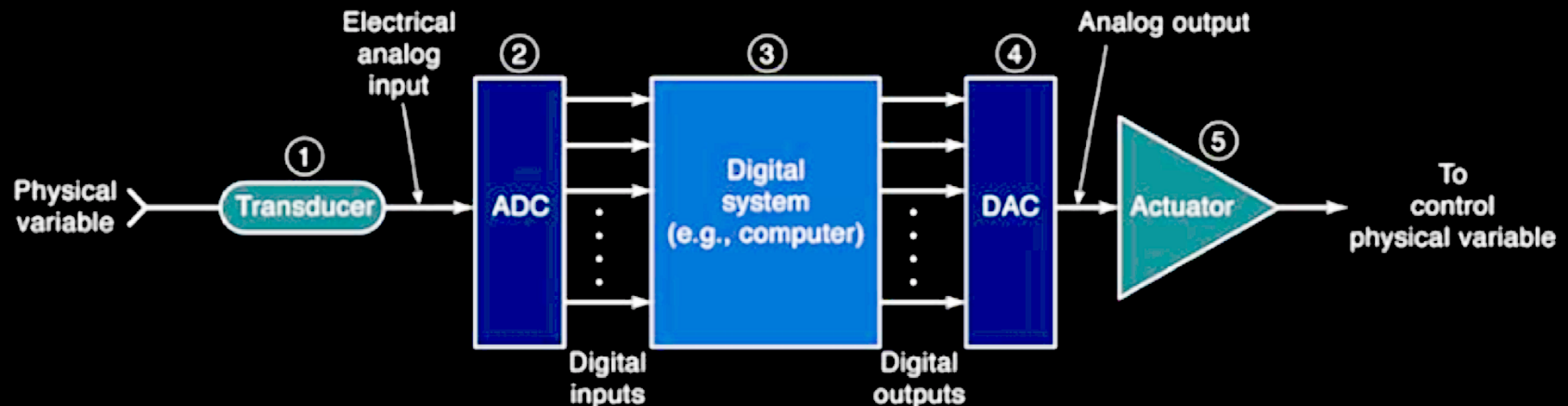
Thermocouples

Accelerometers



1. INTRODUCTION

Real World Applications



Analog-to-digital converters (ADC) and digital-to-analog converters (DAC) are used to interface a computer to the analog world so that the computer can monitor and control a physical variable.

ESSENTIAL INSTRUMENTATION

1. INTRODUCTION

Need to Sample an analog signal and, then convert to digital by A/D converter

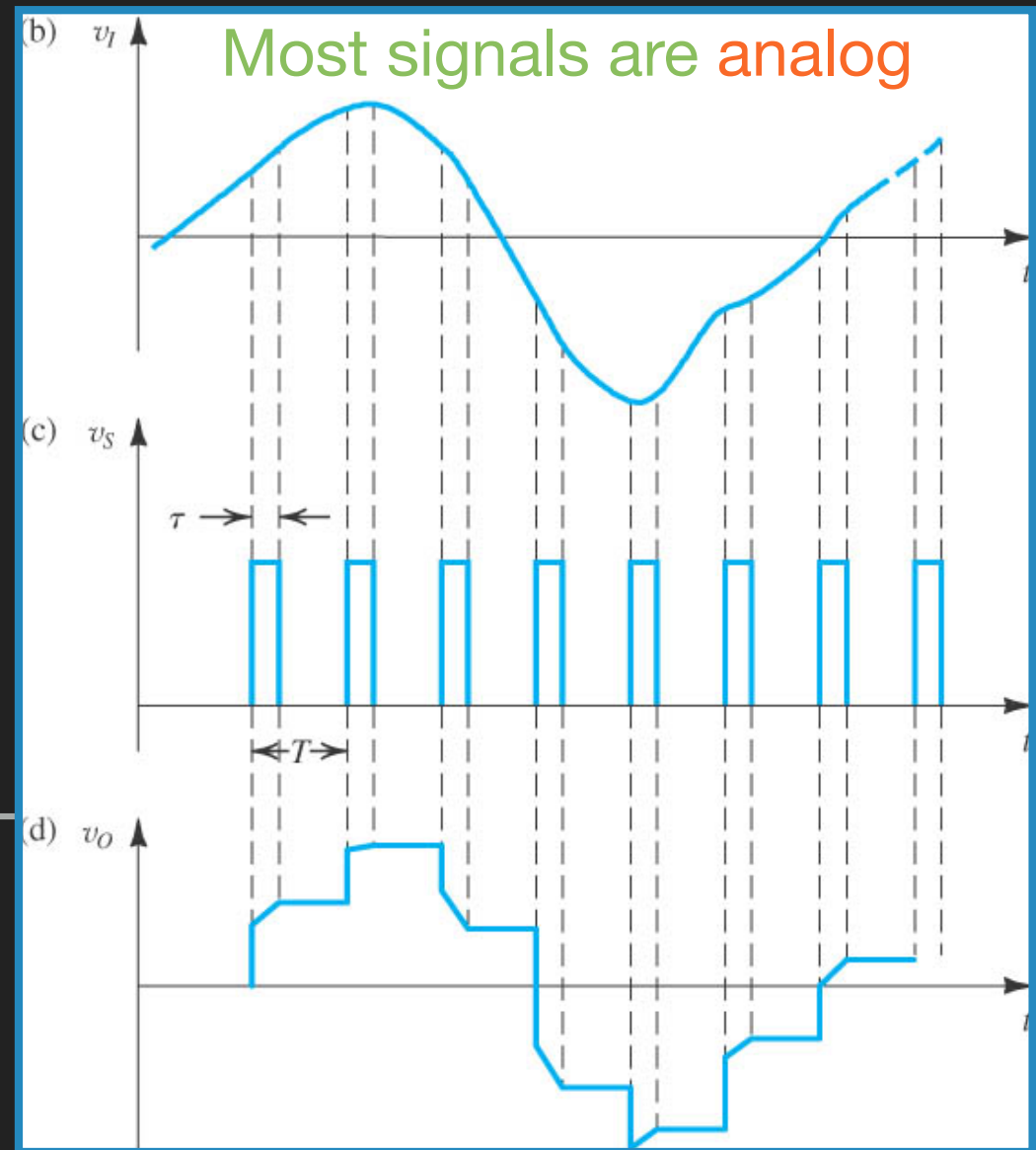
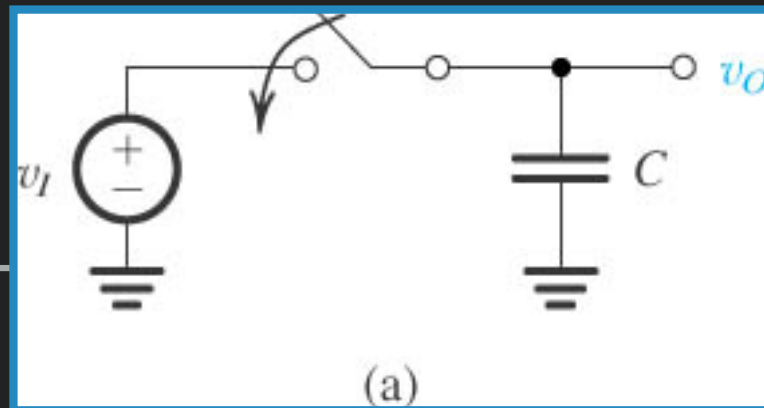
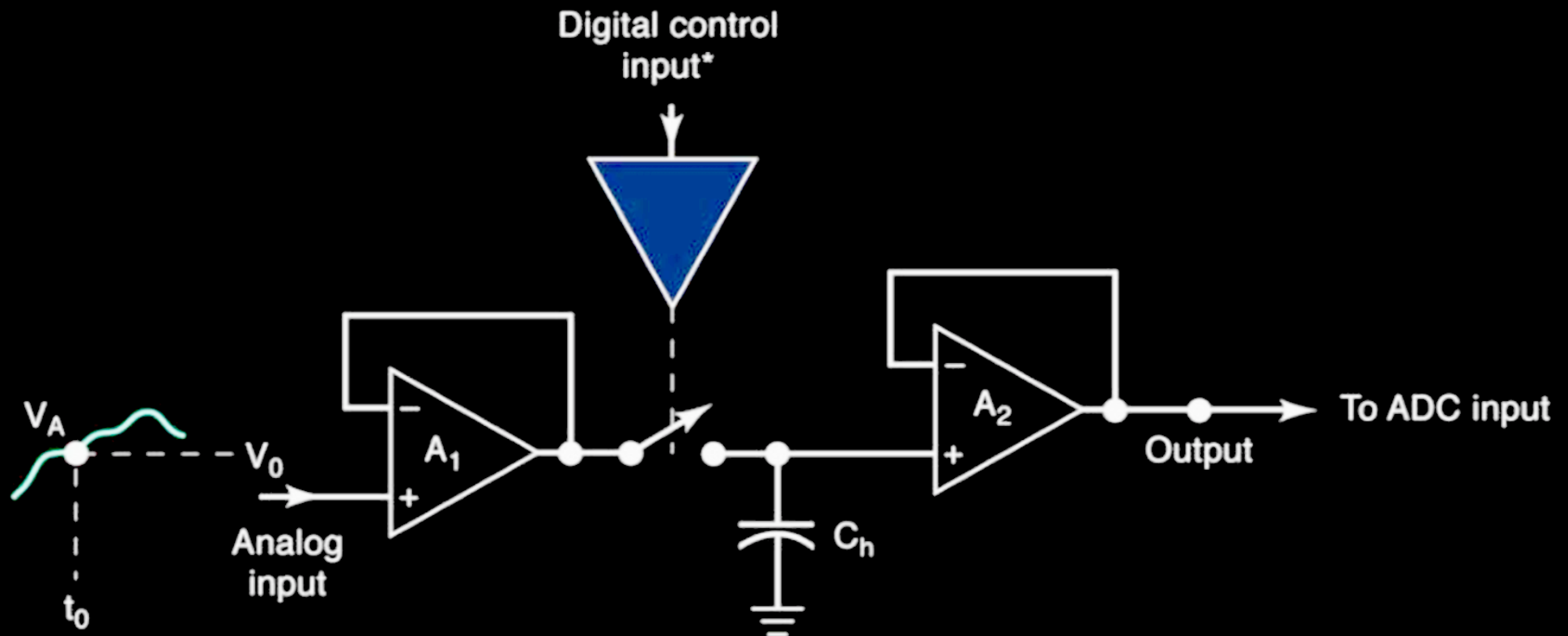


Figure The process of periodically sampling an analog signal. (a) Sample-and-hold (S/H) circuit. The switch closes for a small part (τ seconds) of every clock period (T). (b) Input signal waveform. (c) Sampling signal (control signal for the switch). (d) Output signal (to be fed to A/D converter).

1. INTRODUCTION

Simplified Diagram of a Sample-and-Hold Circuit



*Control = 1 → switch closed → sample mode
Control = 0 → switch open → hold mode

ESSENTIAL INSTRUMENTATION

2. DIGITAL ANALOG CONVERTERS (DAC)

Normal Output from **Digital** domain is a staircase
Filtered to produce smooth **Analog** output

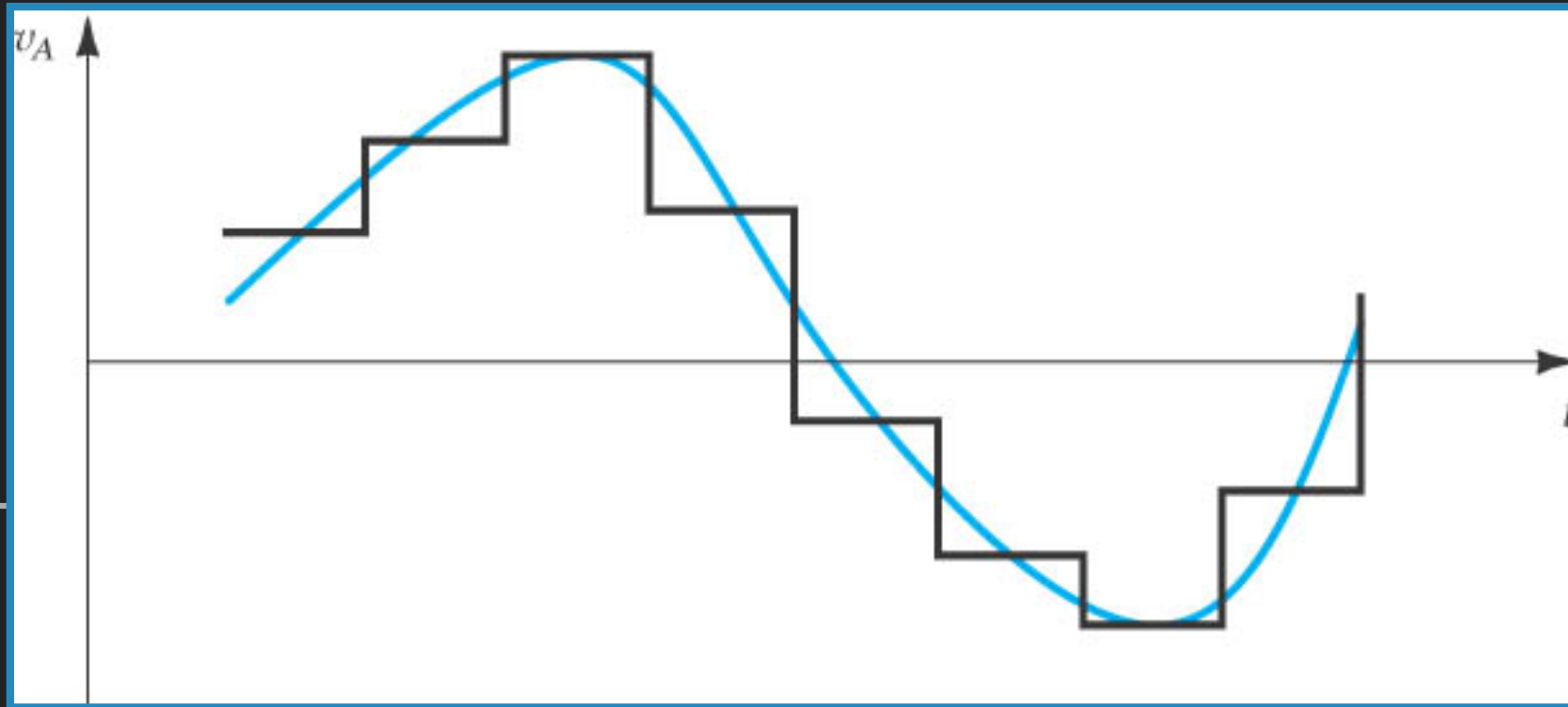


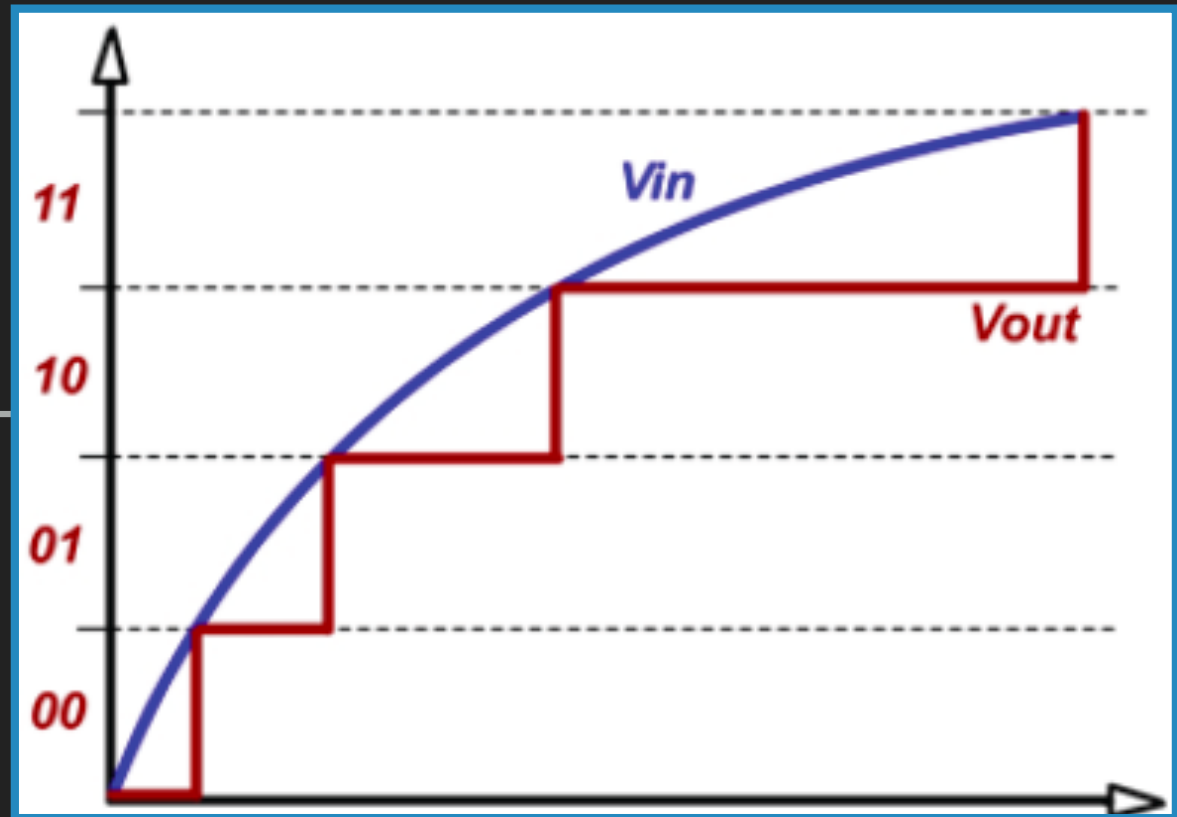
Figure: The analog samples at the output of a D/A converter are usually fed to a sample-and-hold circuit to obtain the staircase waveform shown. This waveform can then be filtered to obtain the smooth waveform, shown in color. The time delay usually introduced by the filter is not shown.

ESSENTIAL INSTRUMENTATION

2. DIGITAL ANALOG CONVERTERS (DAC)

CONVERSION ACCURACY: EG 2-BITS

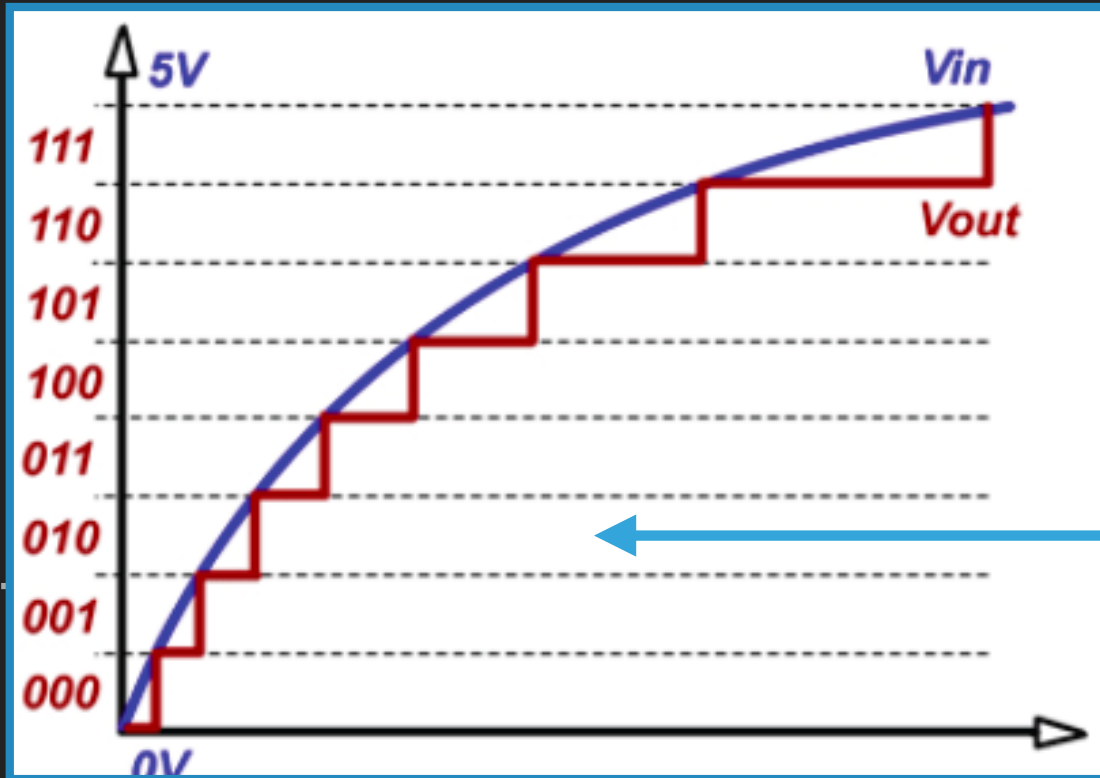
ANALOG IS CONTINUOUS
BUT DIGITAL IS **DISCRETE**
LIMITED BY NUMBER OF BITS



ESSENTIAL INSTRUMENTATION

2. DIGITAL ANALOG CONVERTERS (DAC)

CONVERSION ACCURACY: EG 3-BITS



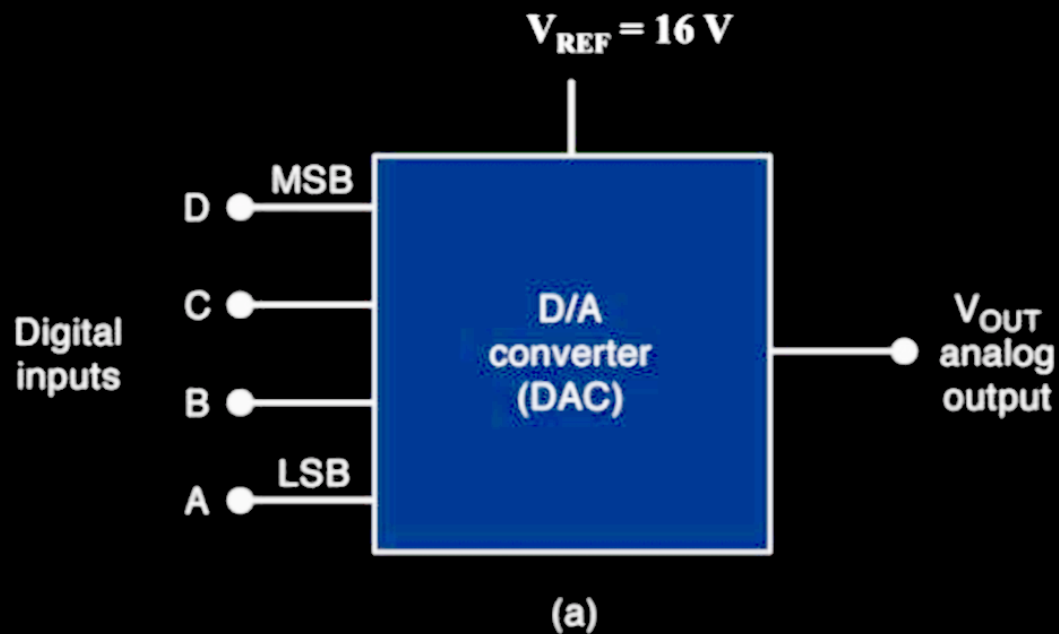
Quantization levels

Voltage levels [V]	Binary representation
0-0.62	000
0.621-1.25	001
1.251-1.87	010
1.871-2.5	011
2.51-3.12	100
3.121-3.75	101
3.751-4.37	110
4.371-5.00	111

Eg 5V divided into 8 levels – each 0.625
Each binary representation is a “range”

2. DIGITAL ANALOG CONVERTERS (DAC)

Four-Bit DAC with Voltage Output



D	C	B	A	V_{OUT}
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
<hr/>				
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

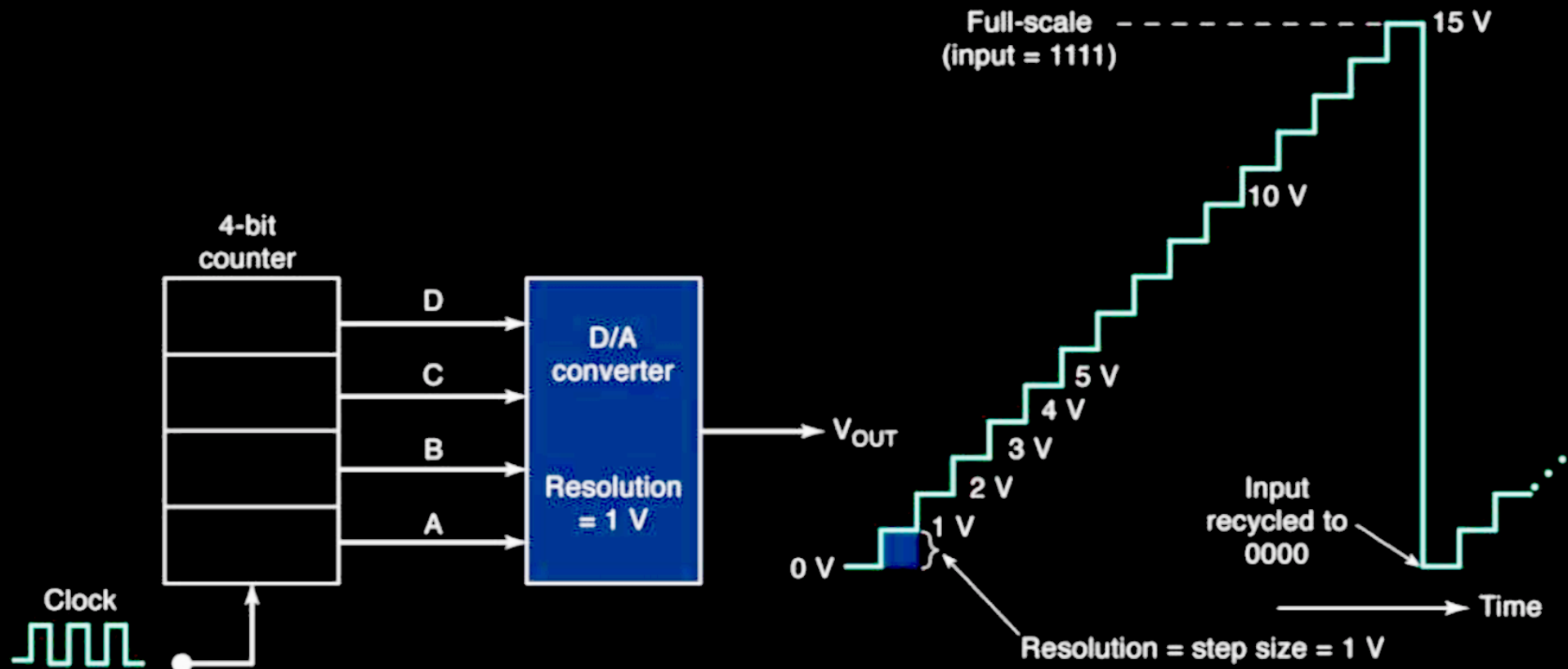
Volts

(b)

$$V_{STEP} = \frac{V_{FS}}{2^N - 1} = \frac{V_{REF}}{2^N}$$

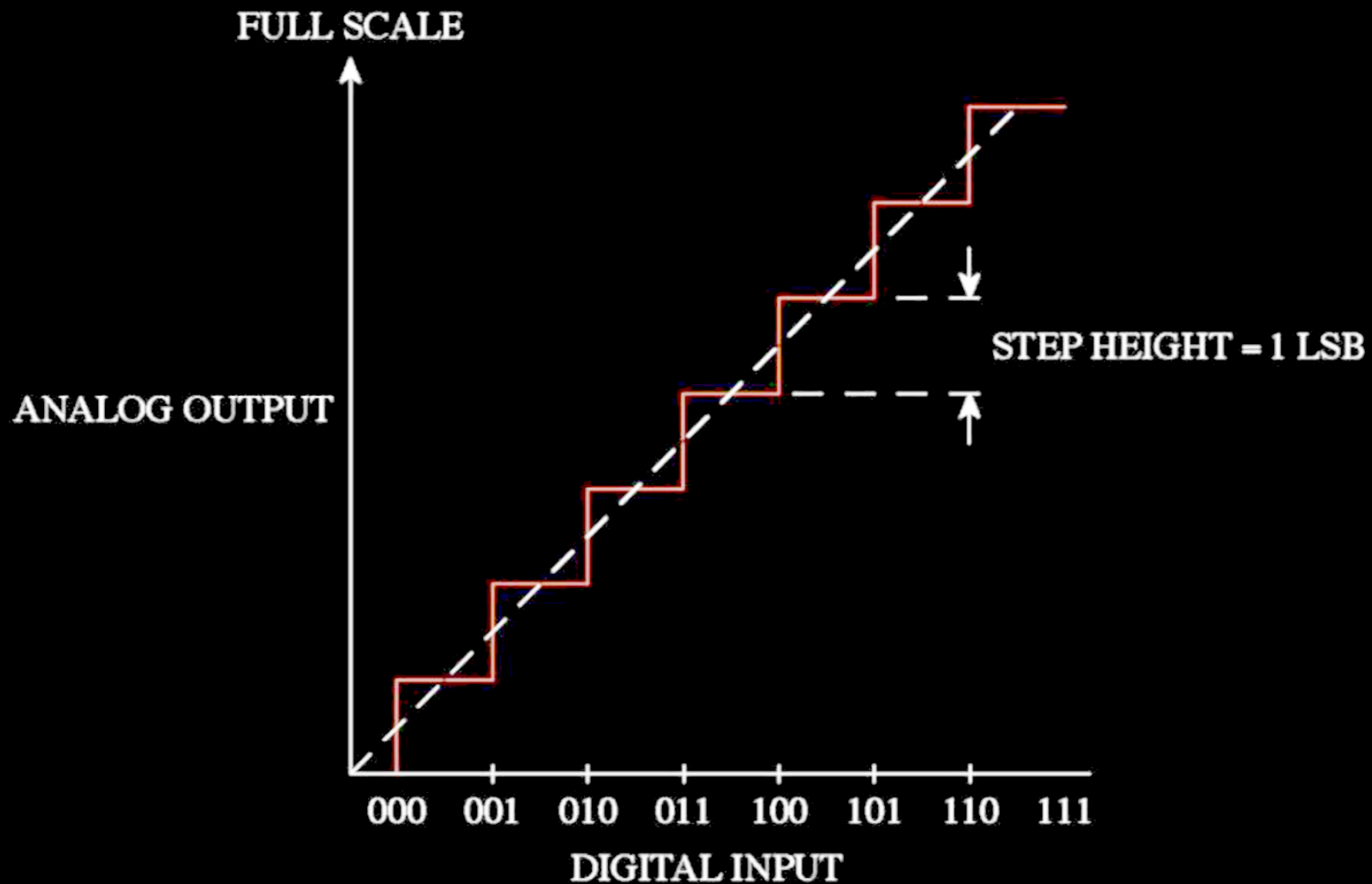
2. DIGITAL ANALOG CONVERTERS (DAC)

Output Waveform of a 4-Bit DAC with a Binary Counter Supplying the Input



2. DIGITAL ANALOG CONVERTERS (DAC)

DAC Transfer Function



2. DIGITAL ANALOG CONVERTERS (DAC)

Definitions

- **Full Scale Output** – the maximum value that the D/A converter can produce.
- **Resolution or Step Size** – the smallest change that can occur in the analog output as a result of a change in the digital input.

$$K = \frac{A_{FS}}{2^N - 1} \quad \text{where } N \text{ is number of bits}$$

- **Analog Output** = $K \cdot$ decimal value of the digital input
- **Percentage Resolution**

$$= \frac{\text{resolution}}{\text{full scale}} \times 100\%$$

- **Accuracy**
 - **Full Scale Error** – maximum deviation of the DAC's output from its ideal value.
 - **Linearity Error** – maximum deviation in step size from the ideal step size.
 - **Offset Error** – the small output voltage that exists when all inputs are "0"
- **Settling Time** – the time required for the DAC output to go from zero to full scale as the binary input goes from all 0's to all 1's.

2. DIGITAL ANALOG CONVERTERS (DAC)

Example Problems

- 1) An eight-bit DAC produces an output voltage of 2.0 V for an input code of 01100100. What will the value of V_{OUT} be for an input code of 10110011?

$$01100100_2 = 100_{10}$$

$$10110011_2 = 179_{10}$$

$$(179/100) = (X/2V)$$

$$X = 3.58V$$

- 2) What is the resolution of the DAC in the previous? Express it in volts and as a percentage. Determine the weight of each input bit.

$$\text{Resolution} = 2V/100 = 20mV$$

$$\text{Full Scale Voltage} = 20mV (2^8 - 1) = 5.1V$$

$$\% \text{ Resolution} = [20mV / \{20mV (2^8 - 1)\}] \times 100\% \approx 0.4\%$$

$$\text{LSB} = 2V/100 = 20mV$$

Other bits: 40mV, 80mV, 160mV, 320mV, 640mV, 1280mV, and 2560mV.

2. DIGITAL ANALOG CONVERTERS (DAC)

Example Problems

- 3) What is the resolution in volts of a 10-bit DAC whose Full-Scale output is 5 V?

10 bits---> $2^{10} - 1 = 1023$ steps

Resolution = $5V/1023 = 4.89 \text{ mV} \approx 5\text{mV}$

- 4) How many bits are required for a DAC so that its Full-Scale output is 10 mA and its resolution is less than $40 \mu\text{A}$?

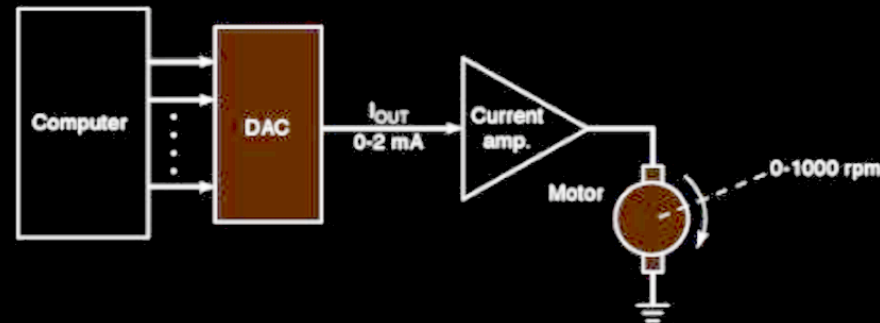
The maximum resolution is $40\mu\text{A}$. The number of steps required to produce 10mA full scale will be at least $10\text{mA}/40\mu\text{A} = 250$.

Therefore, it requires at least 8 bits.

2. DIGITAL ANALOG CONVERTERS (DAC)

Example Problems

- 5) Assuming a 12-bit DAC with perfect accuracy, how close to 250 rpm can the motor speed be adjusted for the motorized system below?



12-bit DAC gives us $2^{12} - 1$ steps = 4095. Step-Size = $2\text{mA}/4095 = 488.4\text{nA}$

To have exactly 250 RPM the output of the DAC must be
 $(250 \text{ RPM} \times 2\text{mA}) / 1000 \text{ RPM} = 500\mu\text{A}$.

In order to have $500\mu\text{A}$ at the output of the DAC, the computer must increment the input of the DAC to the count of $500\mu\text{A}/488.4\text{nA} = 1023.75$.

Thus, the motor will rotate at $(1024/4095) \times 1000 \text{ RPM} = 250.061 \text{ RPM}$ when the computer's output has incremented 1024 steps.

2. DIGITAL ANALOG CONVERTERS (DAC)

Example Problems

- 6) An eight-bit DAC has a full-scale error of 0.2% F.S. If the DAC has a full-scale output of 10 mA, what is the most that it can be in error for any digital input? If the DAC output reads 50 μ A for a digital input of 00000001, is this within the specified range of accuracy? (Assume no offset error.)

Full Scale error = $0.2\% \times 10\text{mA} = 20\mu\text{A}$

Step-Size = $10\text{mA}/255 = 39.2\mu\text{A}$. Ideal output for 00000001₂ is 39.2 μ A.

The possible range is $39.2\mu\text{A} \pm 20\mu\text{A} = 19.2\mu\text{A}$ to 59.2 μ A.

Thus, 50 μ A is within this range.

2. DIGITAL ANALOG CONVERTERS (DAC)

Example Problems

- 7) A particular 6-bit DAC has a full-scale output rated at 1.260 V. Its accuracy is specified as $\pm 0.1\%$ F.S., and it has an offset error of ± 1 mV. Assume that the offset error has not been zeroed out. Consider the measurements made on this DAC in the table below, and determine which of them are not within the device's specifications.

Input Code	Output
000010	41.5 mV
000111	140.2 mV
001100	242.5 mV
111111	1.258 V

$$\text{Step-Size} = 1.26\text{V}/63 = 20\text{mV}$$

$$\pm 0.1\% \text{ F.S.} = \pm 1.26\text{mV}$$

Thus, maximum error will be $\pm 1.26\text{mV} \pm 1\text{mV} = \pm 2.26 \text{ mV}$.

$$000010_2 \rightarrow 2 \times 20\text{mV} = 40\text{mV}$$

$$000111_2 \rightarrow 7 \times 20\text{mV} = 140\text{mV}$$

$$001100_2 \rightarrow 12 \times 20\text{mV} = 240\text{mV}$$

$$111111_2 \rightarrow 63 \times 20\text{mV} = 1.260\text{V}$$

[41.5mV is within specs.] .

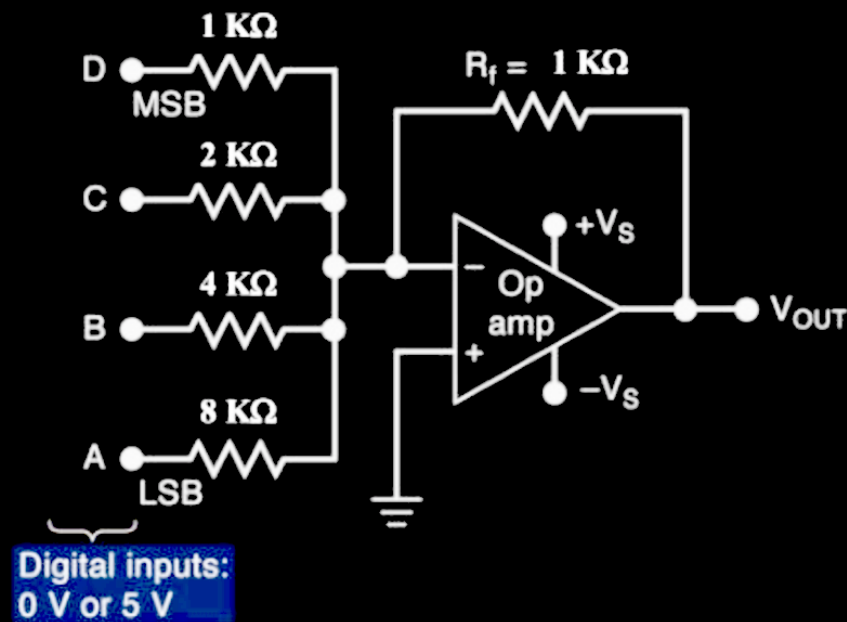
[140.2mV is within specs.] .

[242.5mV isn't within specs.] .

[1.258 V is within specs.] .

2. DIGITAL ANALOG CONVERTERS (DAC)

Simple DAC Using an Op-Amp Summing Amplifier with Binary-Weighted Resistors



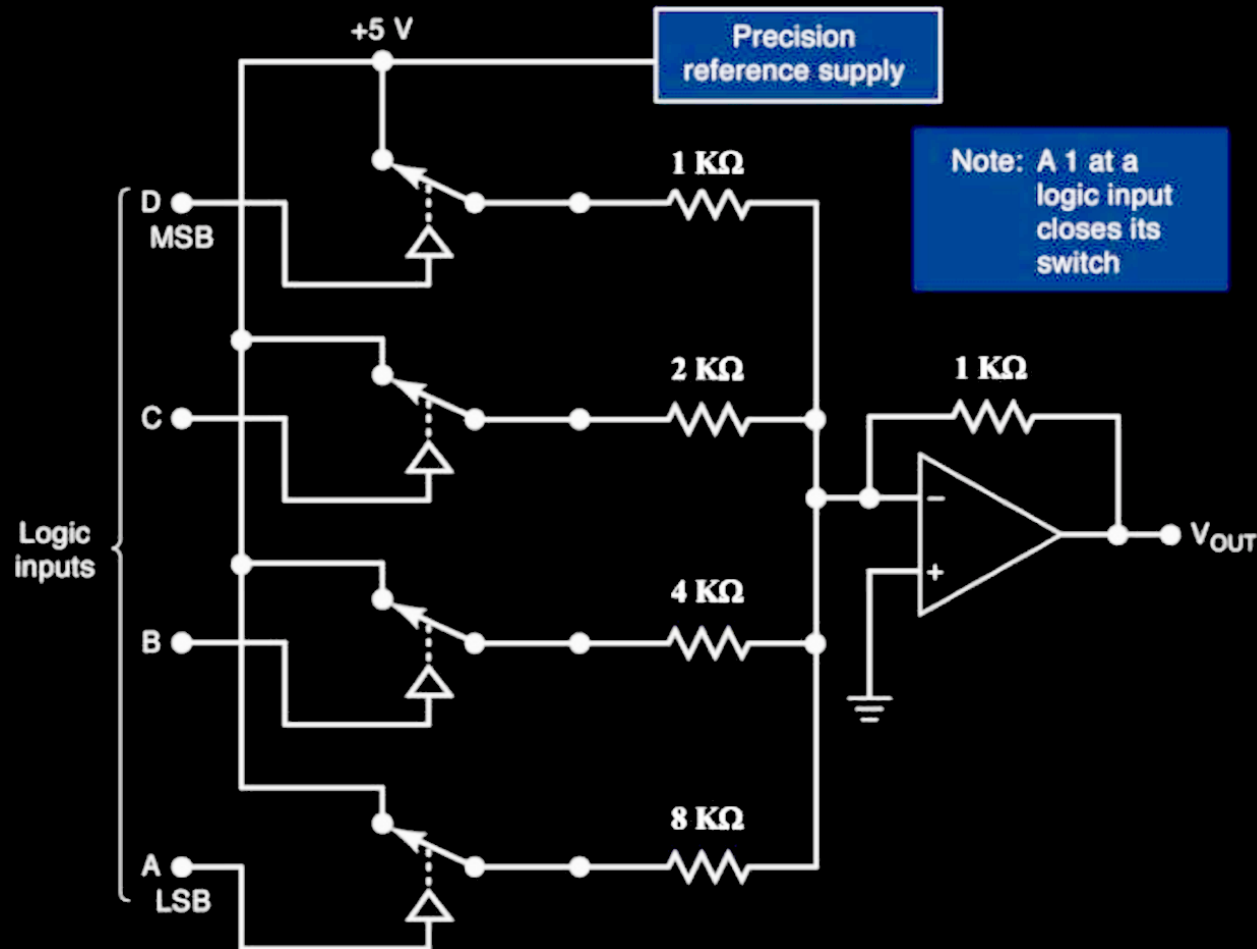
Input code				V_{OUT} (volts)
D	C	B	A	
0	0	0	0	0
0	0	0	1	-0.625 ← LSB
0	0	1	0	-1.250
0	0	1	1	-1.875
0	1	0	0	-2.500
0	1	0	1	-3.125
0	1	1	0	-3.750
0	1	1	1	-4.375
1	0	0	0	-5.000
1	0	0	1	-5.625
1	0	1	0	-6.250
1	0	1	1	-6.875
1	1	0	0	-7.500
1	1	0	1	-8.125
1	1	1	0	-8.750
1	1	1	1	-9.375 ← Full-scale

$$V_{OUT} = -\frac{R_F}{R_D}V_D - \frac{R_F}{R_C}V_C - \frac{R_F}{R_B}V_B - \frac{R_F}{R_A}V_A$$

(b)

2. DIGITAL ANALOG CONVERTERS (DAC)

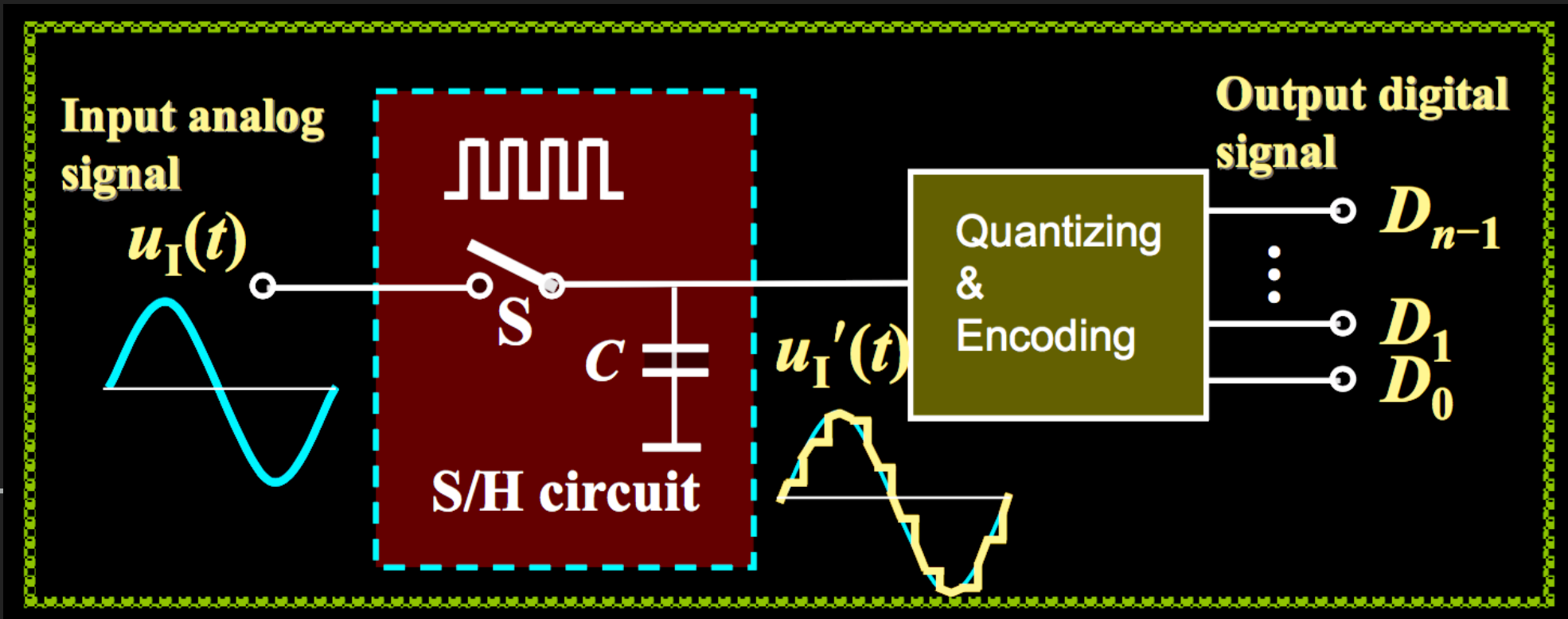
Improved DAC using Summing Amplifier with Precision Voltage Source



ESSENTIAL INSTRUMENTATION

3. ANALOG TO DIGITAL CONVERTERS (ADC)

Analog to Digital process:



2 steps

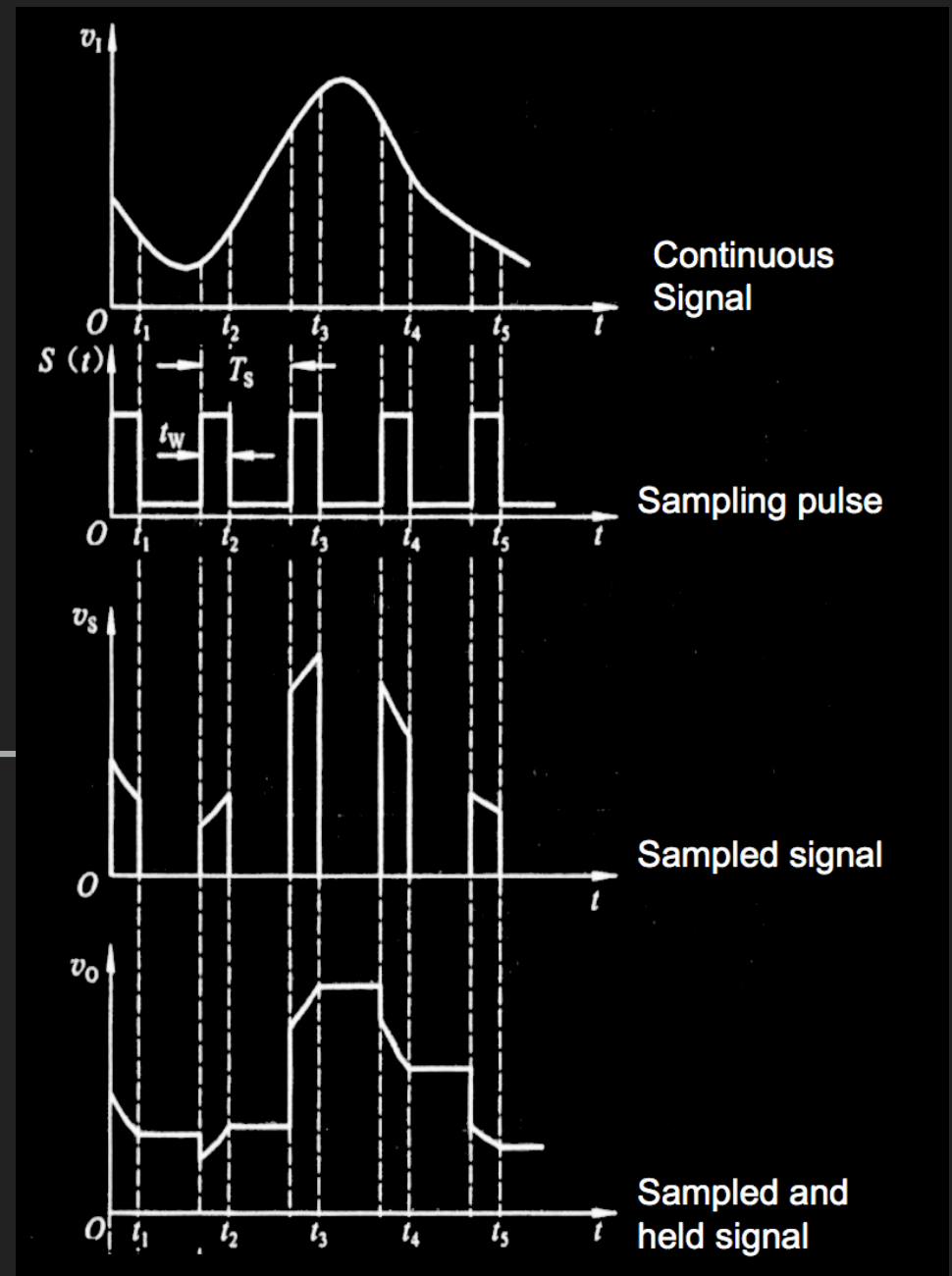
- Sampling and Holding (S/H)
- Quantizing and Encoding (Q/E)

ESSENTIAL INSTRUMENTATION

3. ANALOG TO DIGITAL CONVERTERS (ADC)

Sampling and Holding:

- **Holding** signal benefits the accuracy of the A/D conversion
- Minimum sampling rate should be at least twice the highest data frequency of the analog signal



3. ANALOG TO DIGITAL CONVERTERS (ADC)

Quantizing and Encoding:

■ Resolution

The smallest change in analog signal that will result in a change in the digital output

$$\Delta V = V_{\text{ref}} / 2^N$$

V_{ref} = reference voltage range

N = number of bits in digital output

2^N = number of states

ΔV = resolution

■ The resolution represents the quantisation error inherent in the conversion of the signal to digital form

ESSENTIAL INSTRUMENTATION

3. ANALOG TO DIGITAL CONVERTERS (ADC)

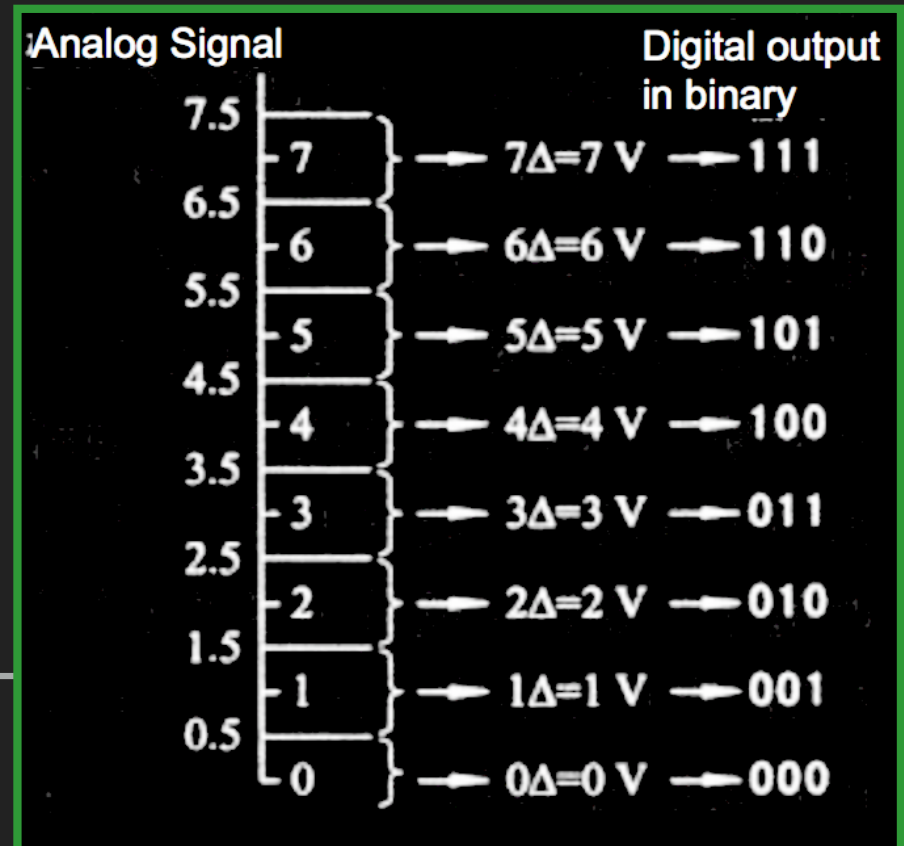
Quantizing and Encoding:

- Quantizing:

Partitioning the reference signal range into a number of discrete quanta, then matching the input signal to the correct quantum.

- Encoding:

Assigning a unique digital code to each quantum, then allocating the digital code to the input signal.



$$\Delta V = 1\text{ V}$$

$$\text{Maximum Quantization error} = \pm \frac{1}{2} \Delta V = \pm 0.5\text{ V}$$

3. ANALOG TO DIGITAL CONVERTERS (ADC)

Quantizing and Encoding:

There are two ways to best improve the accuracy of A/D conversion:

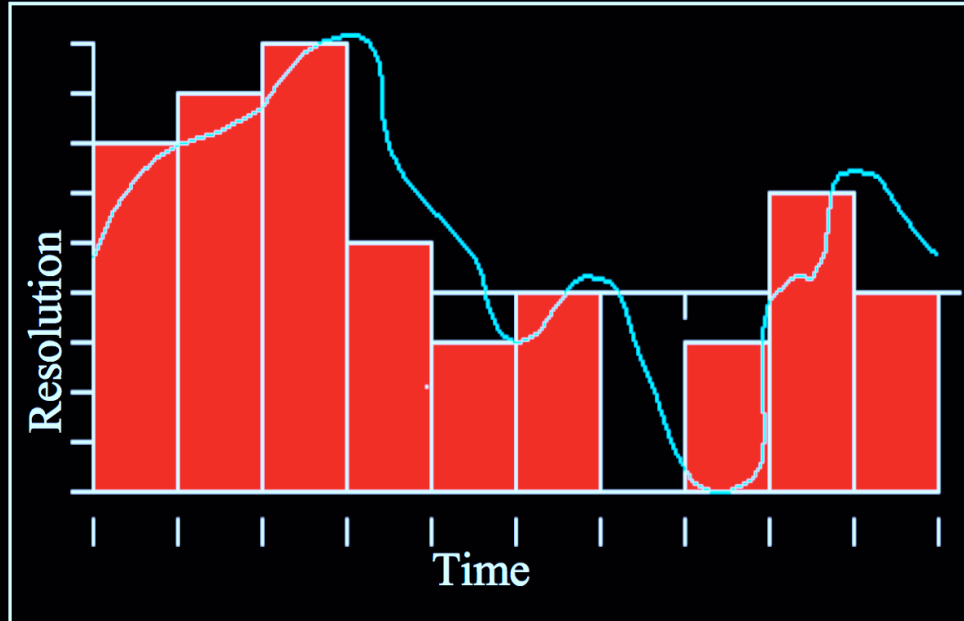
- increasing the resolution which improves the accuracy in measuring the amplitude of the analog signal.
-
- increasing the sampling rate which increases the maximum frequency that can be measured.

ESSENTIAL INSTRUMENTATION

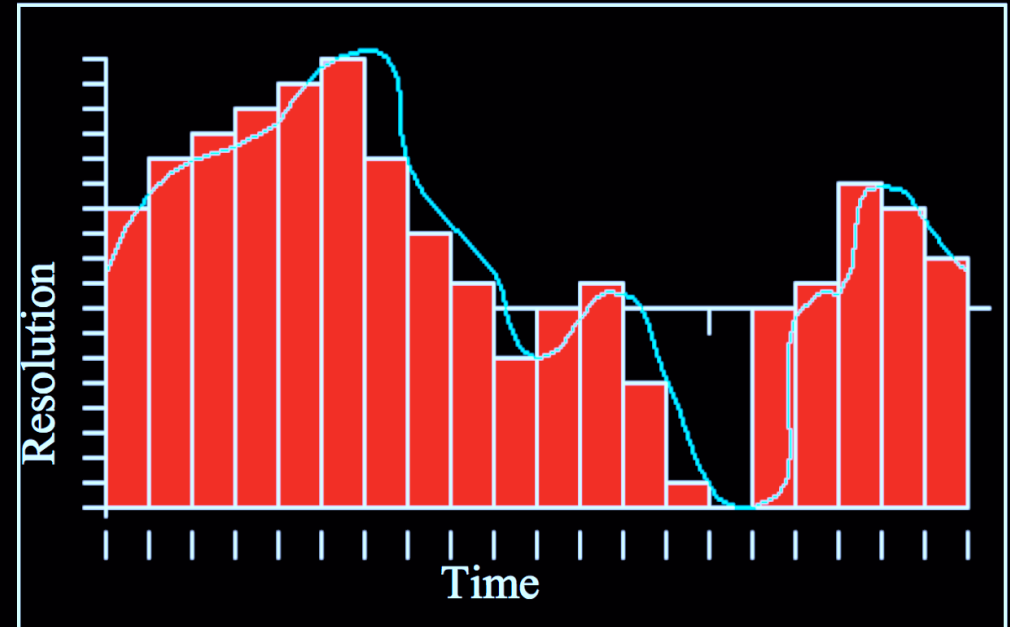
3. ANALOG TO DIGITAL CONVERTERS (ADC)

Quantizing and Encoding:

■ Low Accuracy



■ Improved



3. ANALOG TO DIGITAL CONVERTERS (ADC)

Types of A/D Converters:

- Dual Slope A/D Converter
 - Successive Approximation A/D Converter
 - Flash A/D Converter
 - Delta-Sigma A/D Converter
 - Other
 - Voltage-to-frequency, staircase ramp or single slope, charge balancing or redistribution, switched capacitor, tracking, and synchro or resolver
-

3. ANALOG TO DIGITAL CONVERTERS (ADC)

Types of A/D Converters:

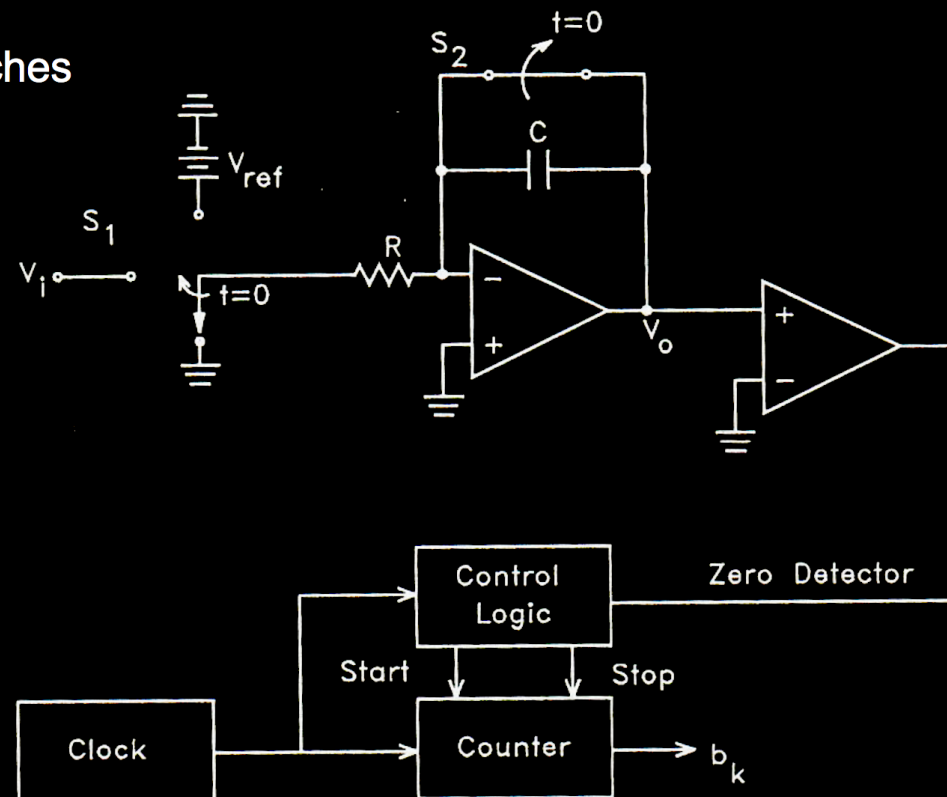
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-
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3. ANALOG TO DIGITAL CONVERTERS (ADC)

Dual Slope A/D Converter:

■ Fundamental components

- Integrator
- Electronically Controlled Switches
- Counter
- Clock
- Control Logic
- Comparator

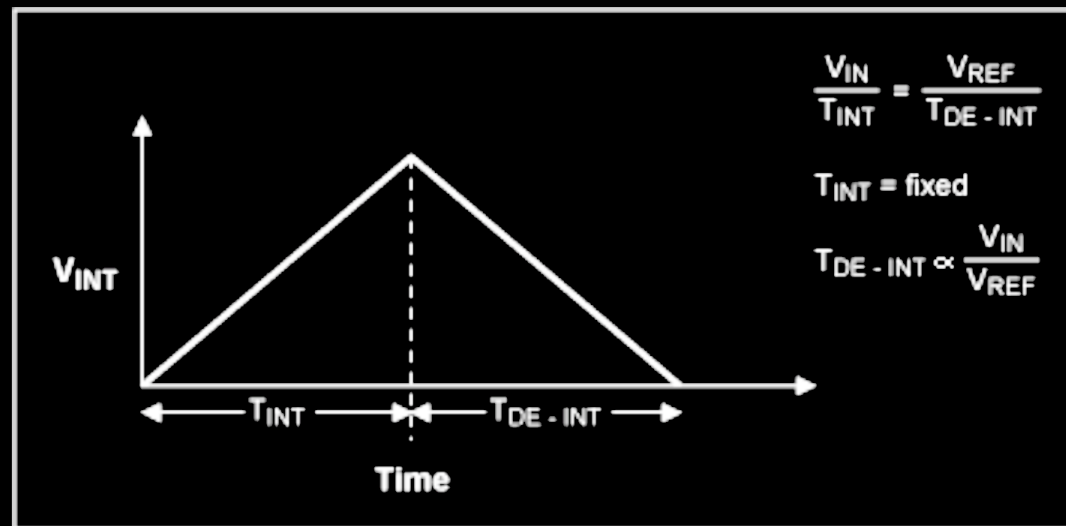


ESSENTIAL INSTRUMENTATION

3. ANALOG TO DIGITAL CONVERTERS (ADC)

How Does it Work?

A dual-slope ADC (DS-ADC) integrates an unknown input voltage (V_{IN}) for a fixed amount of time (T_{INT}), then "de-integrates" (T_{DEINT}) using a known reference voltage (V_{REF}) for a variable amount of time.



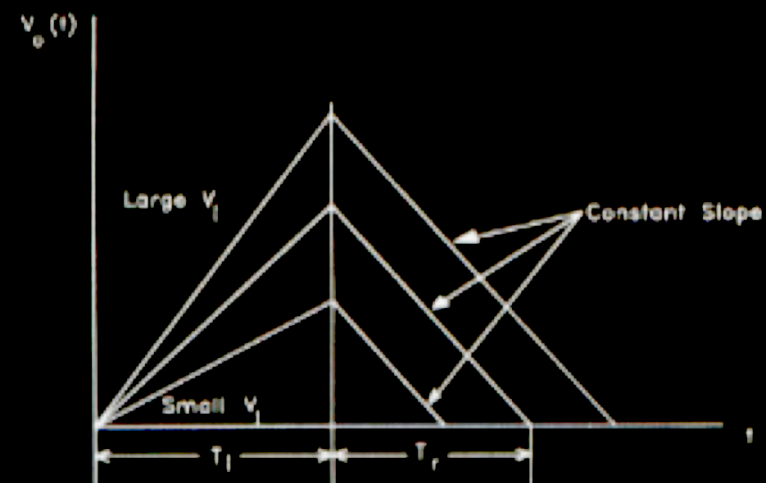
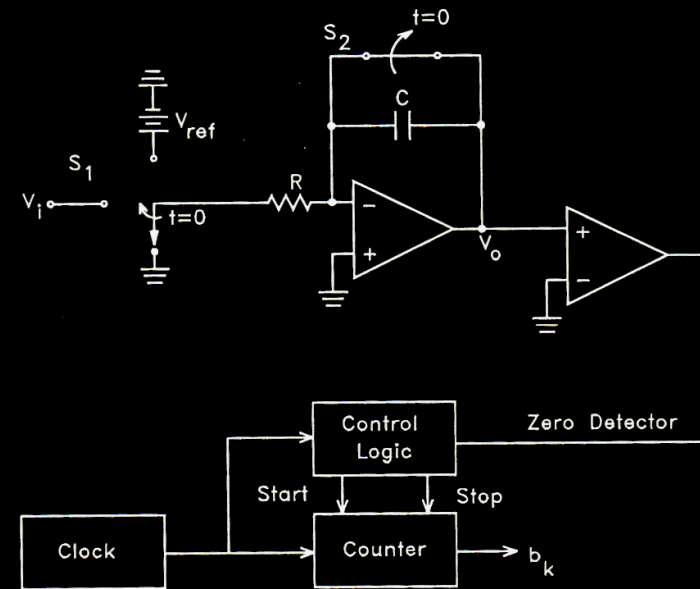
The key advantage of this architecture over the single-slope is that the final conversion result is insensitive to errors in the component values. That is, any error introduced by a component value during the integrate cycle will be cancelled out during the de-integrate phase.

ESSENTIAL INSTRUMENTATION

3. ANALOG TO DIGITAL CONVERTERS (ADC)

How Does it Work?

- At $t < 0$, S_1 is set to ground, S_2 is closed, and counter=0.
- At $t=0$ a conversion begins and S_2 is open, and S_1 is set so the input to the integrator is V_{in} .
- S_1 is held for T_{INT} which is a constant predetermined time interval.
- When S_1 is set the counter begins to count clock pulses, the counter resets to zero after T_{INT}
- V_{out} of integrator at $t=T_{INT}$ is $V_{IN}T_{INT}/RC$ is linearly proportional to V_{IN}
- At $t=T_{INT}$ S_1 is set so $-V_{ref}$ is the input to the integrator which has the voltage $V_{IN}T_{INT}/RC$ stored in it.
- The integrator voltage then drops linearly with a slope $-V_{ref}/RC$.
- A comparator is used to determine when the output voltage of the integrator crosses zero
- When it is zero the digitized output value is the state of the counter.



3. ANALOG TO DIGITAL CONVERTERS (ADC)

How Does it Work?

PROS

- Conversion result is insensitive to errors in the component values.
- Fewer adverse affects from “noise”
- High Accuracy

CONS

- Slow
- Accuracy is dependent on the use of precision external components
- Cost

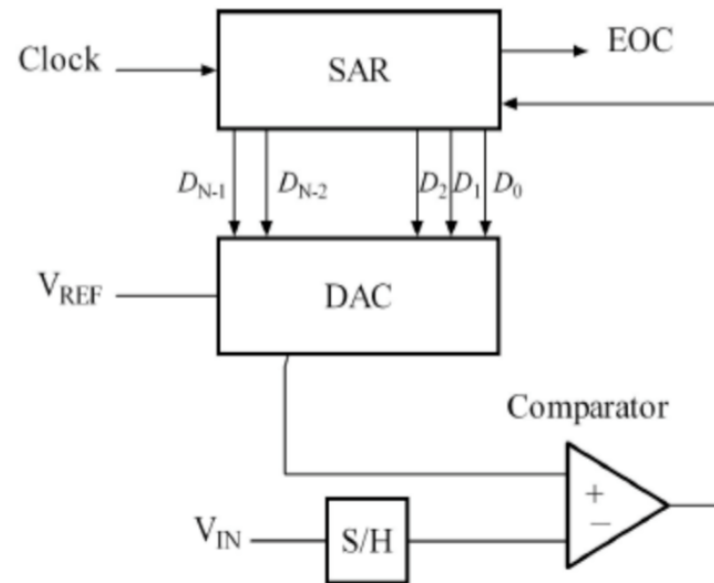
3. ANALOG TO DIGITAL CONVERTERS (ADC)

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3. ANALOG TO DIGITAL CONVERTERS (ADC)

Successive Approximation A/D Converter

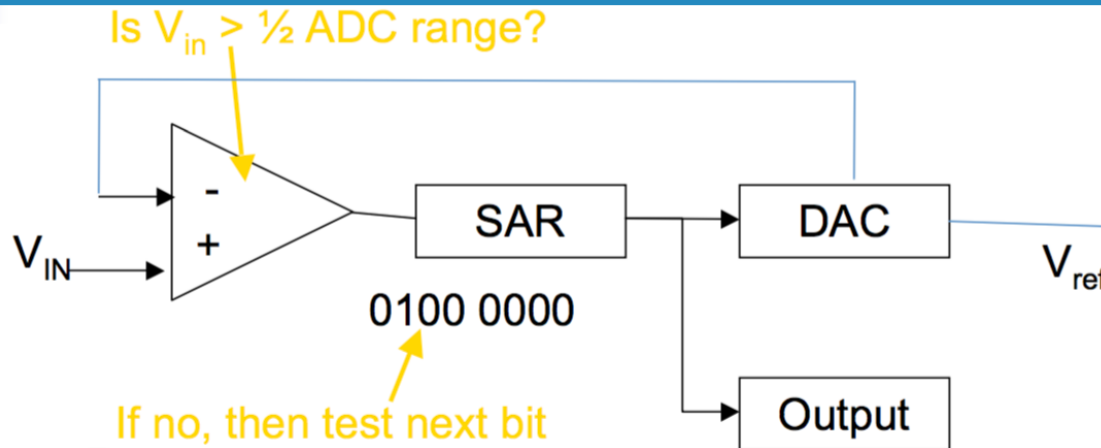


- Uses a n-bit DAC to compare DAC and original analog results.
- Uses Successive Approximation Register (SAR) supplies an approximate digital code to DAC of V_{in} .
- Comparison changes digital output to bring it closer to the input value.
- Uses Closed-Loop Feedback Conversion

3. ANALOG TO DIGITAL CONVERTERS (ADC)

Successive Approximation A/D Converter

HOW DOES IT WORK?



If no, then test next bit

Process

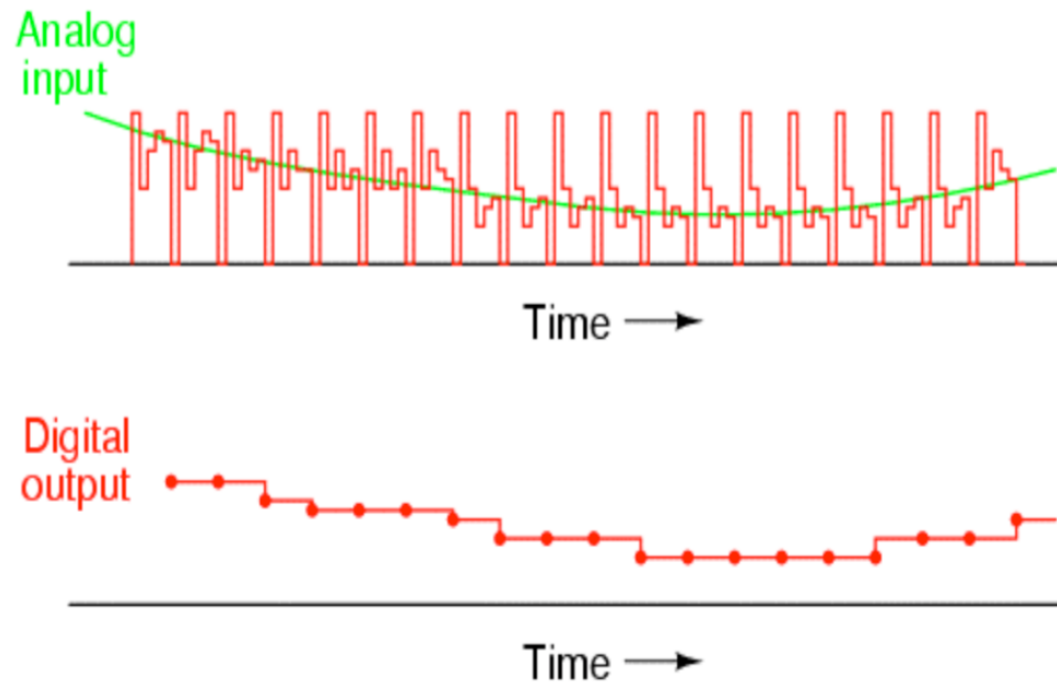
1. MSB initialized as 1
2. Convert digital value to analog using DAC
3. Compares guess to analog input
4. Is $V_{in} > V_{DAC}$
 - Set bit 1
 - If no, bit is 0 and test next bit

Closed-Loop

ESSENTIAL INSTRUMENTATION

3. ANALOG TO DIGITAL CONVERTERS (ADC)

Successive Approximation A/D Converter



3. ANALOG TO DIGITAL CONVERTERS (ADC)

Successive Approximation A/D Converter

Advantages

- Capable of high speed and reliable
- Medium accuracy compared to other ADC types
- Good tradeoff between speed and cost
- Capable of outputting the binary number in serial (one bit at a time) format.

Disadvantages

- Higher resolution successive approximation ADC's will be slower
- Speed limited to ~5Msps

Successive Approximation A/D Converter

EXAMPLE

Example

- 10 bit ADC
- $V_{in} = 0.6$ volts (from analog device)
- $V_{ref} = 1$ volts
- Find the digital value of V_{in}

Bit	Voltage
9	.5
8	.25
7	.125
6	.0625
5	.03125
4	.015625
3	.0078125
2	.00390625
1	.001952125
0	.0009765625

$N = 2^n$ (N of possible states)

$N = 1024$

$V_{max} - V_{min} / N = 1 \text{ Volt} / 1024 = 0.0009765625V$ of V_{ref} (resolution)

Successive Approximation A/D Converter

EXAMPLE

- Next Calculate MSB-1 (bit 8)
 - Compare $V_{in}=0.6\text{ V}$ to $V=V_{ref}/2 + V_{ref}/4= 0.5+0.25 =0.75\text{V}$
 - Since $0.6<0.75$, MSB is turned off
- Calculate MSB-2 (bit 7)
 - Go back to the last voltage that caused it to be turned on (Bit 9) and add it to $V_{ref}/8$, and compare with V_{in}
 - Compare V_{in} with $(0.5+V_{ref}/8)=0.625$
 - Since $0.6<0.625$, MSB is turned off

1	0	0							
---	---	---	--	--	--	--	--	--	--

Successive Approximation A/D Converter

EXAMPLE

- Calculate the state of MSB-3 (bit 6)
 - Go to the last bit that caused it to be turned on (In this case MSB-1) and add it to $V_{ref}/16$, and compare it to V_{in}
 - Compare V_{in} to $V = 0.5 + V_{ref}/16 = 0.5625$
 - Since $0.6 > 0.5625$, MSB-3=1 (turned on)

MSB	MSB-1	MSB-2	MSB-3	...					
1	0	0	1						

Successive Approximation A/D Converter

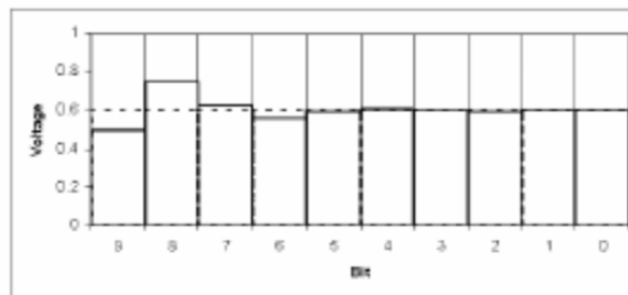
EXAMPLE

- This process continues for all the remaining bits.

•Digital Results:

MSB	MSB-1	MSB-2	MSB-3	...					LSB
1	0	0	1	1	0	0	1	1	0

•Results: $\frac{1}{2} + \frac{1}{16} + \frac{1}{32} + \frac{1}{256} + \frac{1}{512} = .599609375 \text{ V}$



3. ANALOG TO DIGITAL CONVERTERS (ADC)

Types of A/D Converters:

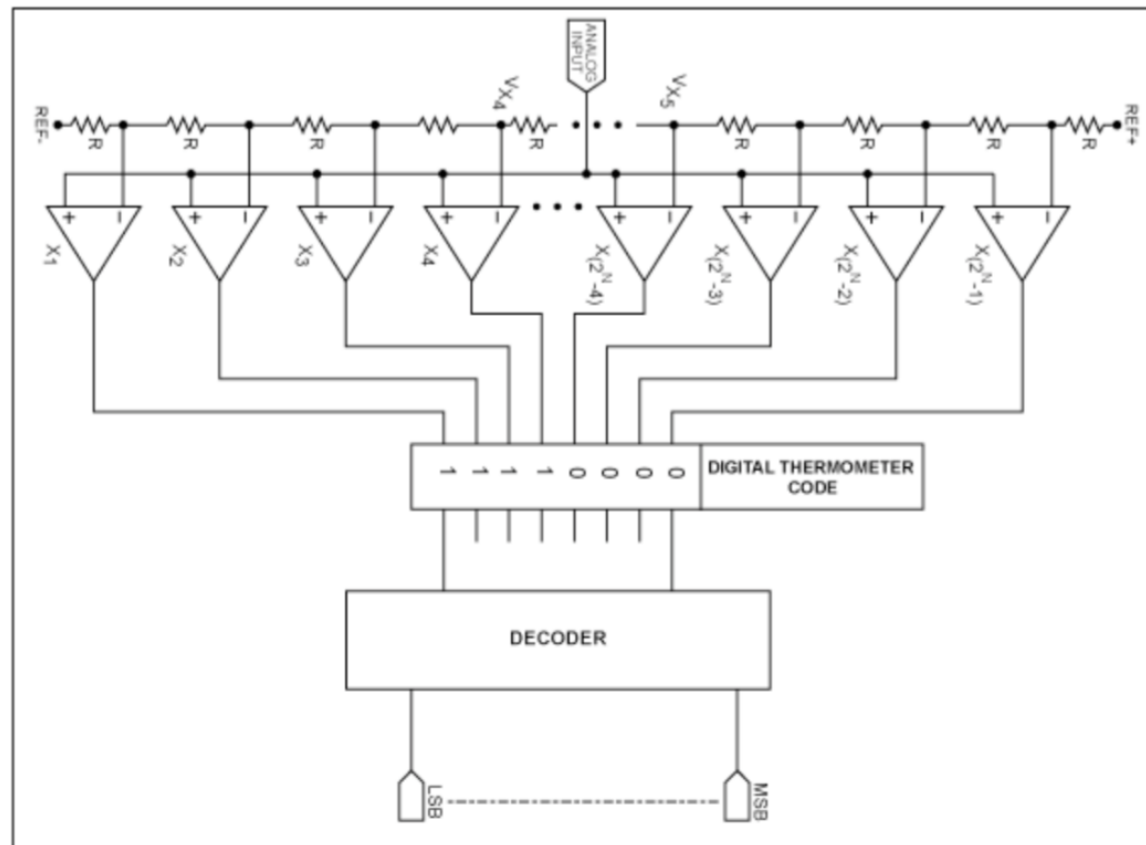
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 - **Flash A/D Converter**
 - Delta-Sigma A/D Converter
 - Other
-
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ESSENTIAL INSTRUMENTATION

3. ANALOG TO DIGITAL CONVERTERS (ADC)

Flash A/D Converter

- Fundamental Components (For N bit Flash A/D)
 - $2^N - 1$ Comparators
 - 2^N Resistors
 - Control Logic



Flash A/D Converter

HOW DOES IT WORK?

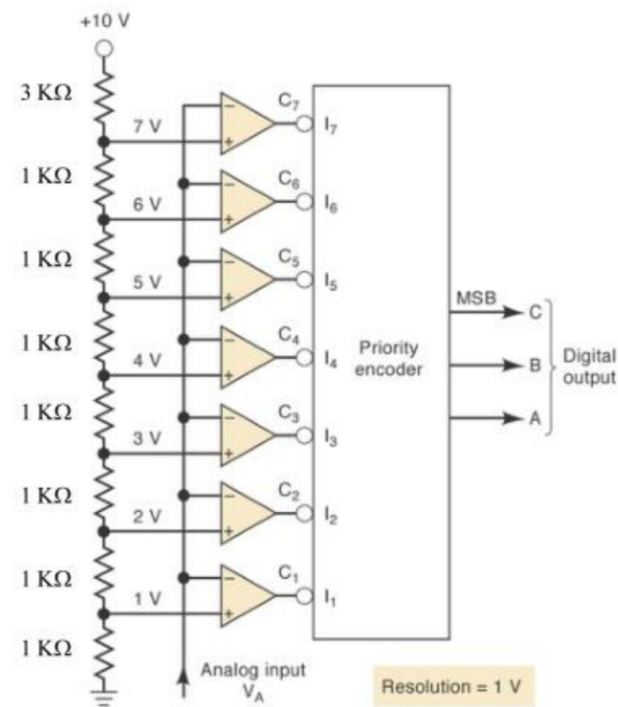
- Uses the 2^N resistors to form a ladder voltage divider, which divides the reference voltage into 2^N equal intervals.
- Uses the 2^N-1 comparators to determine in which of these 2^N voltage intervals the input voltage V_{in} lies.
- The Combinational logic then translates the information provided by the output of the comparators
- This ADC does not require a clock so the conversion time is essentially set by the settling time of the comparators and the propagation time of the combinational logic.

ESSENTIAL INSTRUMENTATION

3. ANALOG TO DIGITAL CONVERTERS (ADC)

Flash A/D Converter

Three-Bit Flash ADC



(a)

Analog in V_A	Comparator outputs							Digital outputs		
	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C	B	A
0-1 V	1	1	1	1	1	1	1	0	0	0
1-2 V	0	1	1	1	1	1	1	0	0	1
2-3 V	0	0	1	1	1	1	1	0	1	0
3-4 V	0	0	0	1	1	1	1	0	1	1
4-5 V	0	0	0	0	1	1	1	1	0	0
5-6 V	0	0	0	0	0	1	1	1	0	1
6-7 V	0	0	0	0	0	0	1	1	1	0
> 7 V	0	0	0	0	0	0	0	1	1	1

Flash A/D Converter

PROS

- Very Fast (Fastest)
- Very simple operational theory
- Speed is only limited by gate and comparator propagation delay

CONS

- Expensive
- Prone to produce glitches in the output
- Each additional bit of resolution requires twice the comparators.

3. ANALOG TO DIGITAL CONVERTERS (ADC)

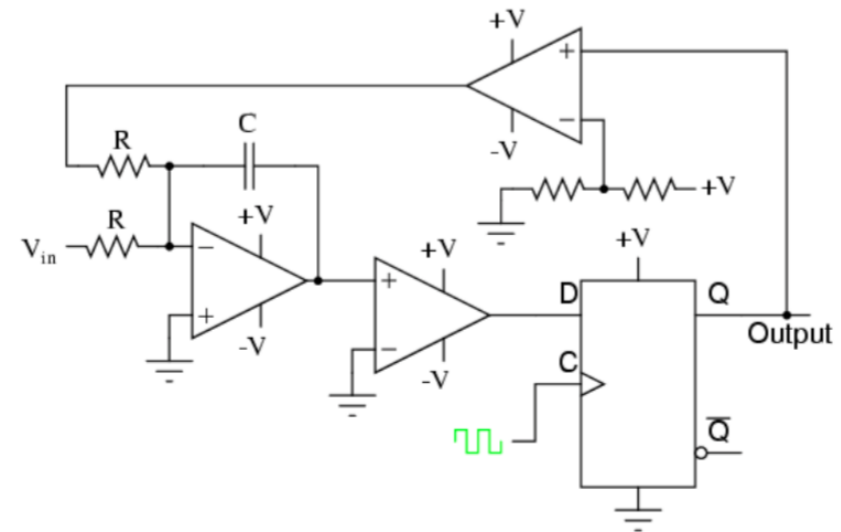
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 - Other
-
- Voltage-to-frequency, staircase ramp or single slope, charge balancing or redistribution, switched capacitor, tracking, and synchro or resolver

Delta-Sigma A/D Converter

Main Components

- Resistors
- Capacitor
- Comparators
- Control Logic
- DAC

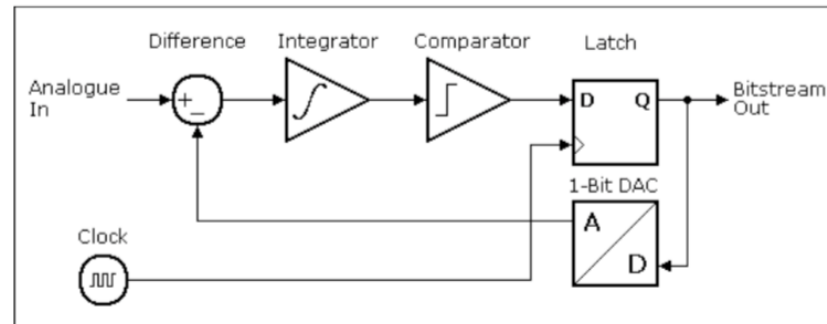


3. ANALOG TO DIGITAL CONVERTERS (ADC)

Delta-Sigma A/D Converter

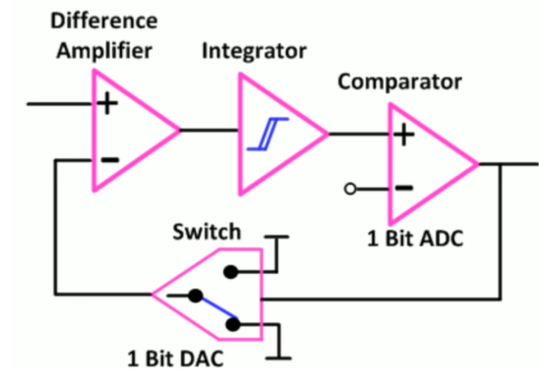
HOW DOES IT WORK?

- Input is over sampled, and goes to integrator.
- The integration is then compared to ground.
- Iterates and produces a serial bit stream
- Output is a serial bit stream with # of 1's proportional to V_{in}



- With this arrangement the sigma-delta modulator automatically adjusts its output to ensure that the average error at the quantizer output is zero.
- The integrator value is the sum of all past values of the error, so whenever there is a non-zero error value the integrator value just keeps building until the error is once again forced to zero.

$\Delta\Sigma$ Modulator



OR EQUIVALENTLY

3. ANALOG TO DIGITAL CONVERTERS (ADC)

Delta-Sigma A/D Converter

PROS

- High Resolution
- No need for precision components

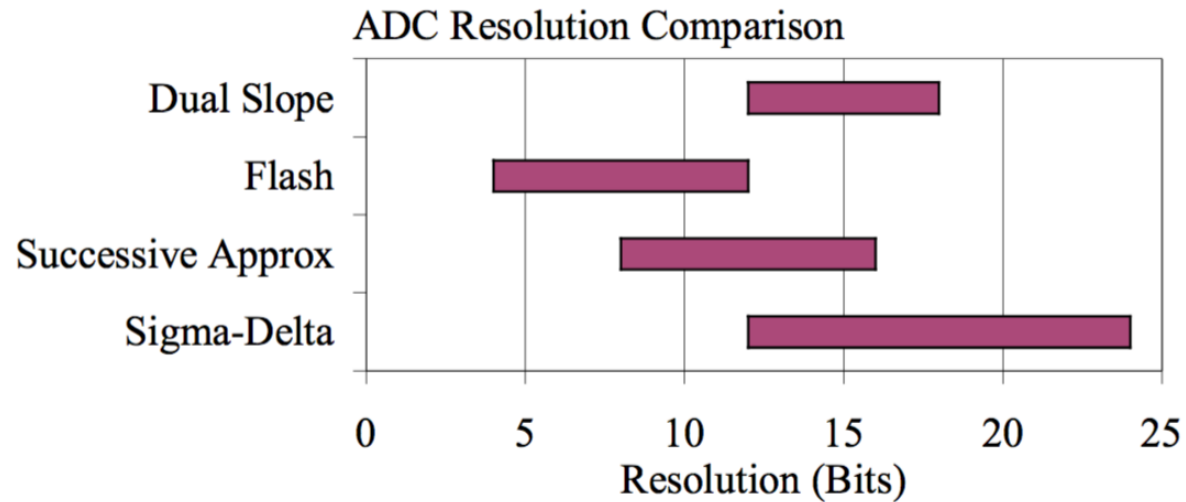
CONS

- Slow due to over sampling
- Only good for low bandwidth

ESSENTIAL INSTRUMENTATION

3. ANALOG TO DIGITAL CONVERTERS (ADC)

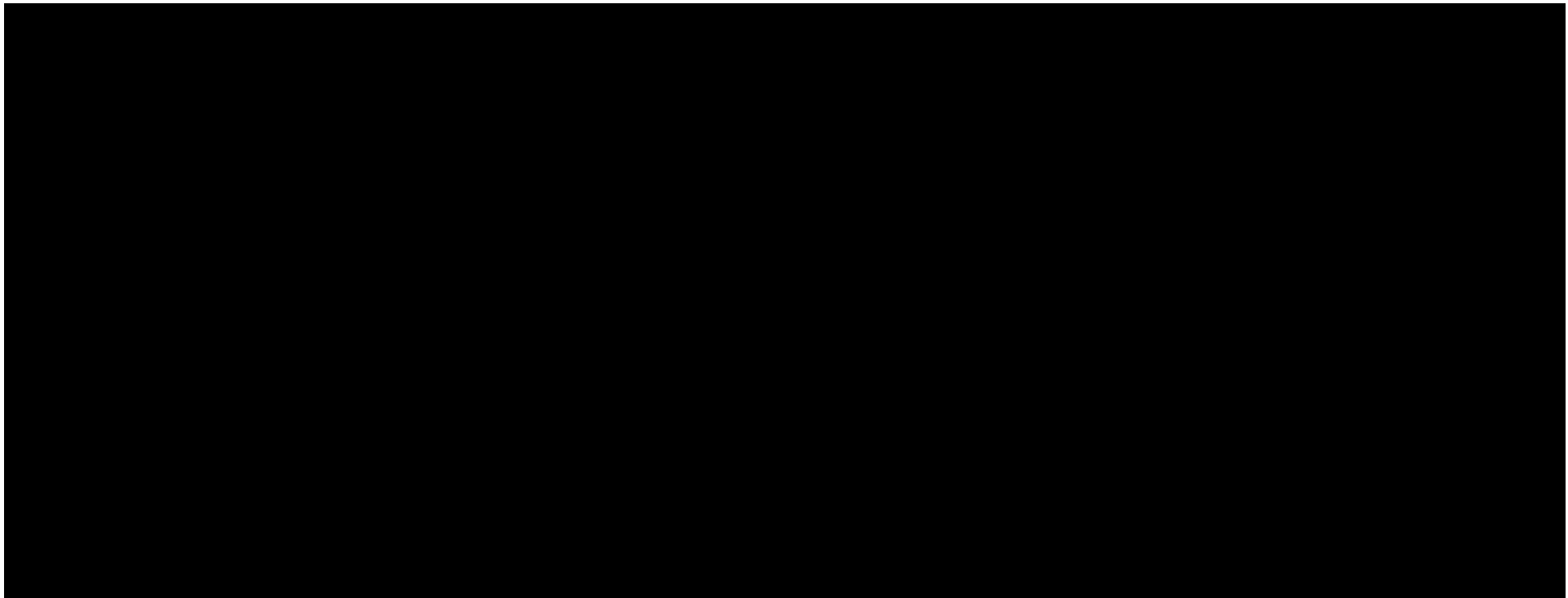
ADC Comparison



Type	Speed (relative)	Cost (relative)
Dual Slope	Slow	Med
Flash	Very Fast	High
Successive Approx	Medium – Fast	Low
Sigma-Delta	Slow	Low

Example Problems

- 1) An eight-bit **digital ramp** ADC with a 40 mV resolution uses a clock frequency of 2.5 MHz. Determine the following values:
 - a) the digital output for an analog voltage of 6.005 V
 - b) the digital output for an analog voltage of 6.035 V
 - c) the maximum and average conversion times



Example Problems

- 1) An eight-bit **digital ramp** ADC with a 40 mV resolution uses a clock frequency of 2.5 MHz. Determine the following values:
- the digital output for an analog voltage of 6.005 V
 - the digital output for an analog voltage of 6.035 V
 - the maximum and average conversion times

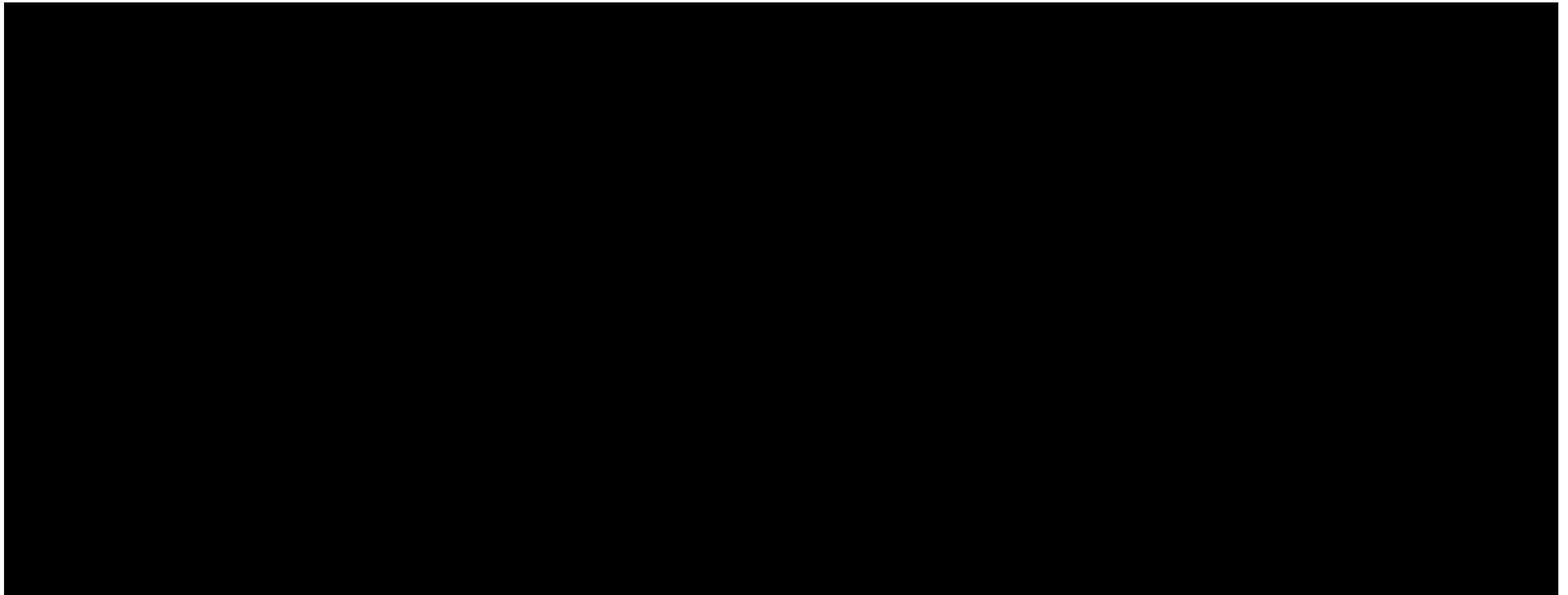
a) $6.005 \text{ V} / 40 \text{ mV} = 150.125 = 151_{10} = 10010111_2.$

b) Using same method as in (a) the digital value is again $10010111_2.$

c) Maximum conversion time = (max. # of steps) x (T_{CLOCK})
 $t_{\text{max_conv}} = (2^8 - 1) \times (0.4 \mu\text{s}) = 102 \mu\text{s}.$
 Average conversion time = $102 \mu\text{s} / 2 = 51 \mu\text{s}$

Example Problems

-
- 2) Why were the digital outputs the same for parts a) and b) of question 1?



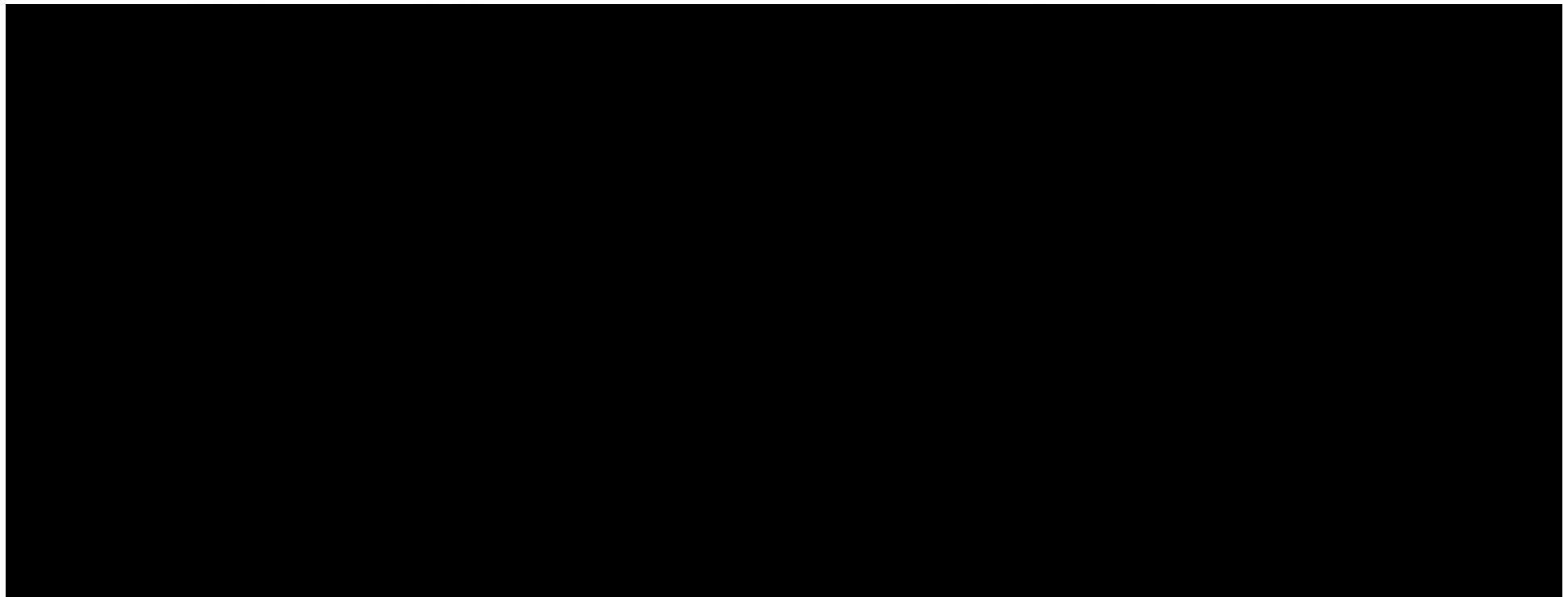
Example Problems

- 2) Why were the digital outputs the same for parts a) and b) of question 1?

Because the difference in the two values of V_A was smaller than the resolution of the converter.

Example Problems

- 3) An ADC has the following characteristics: resolution of 12 bits, full scale error of 0.03%, and full scale input of 5 V. What is the quantization error in volts? What is the total possible error in volts?



Example Problems

- 3) An ADC has the following characteristics: resolution of 12 bits, full scale error of 0.03%, and full scale input of 5 V. What is the quantization error in volts? What is the total possible error in volts?

With 12 bits, percentage resolution is

$$(1/(2^{12}-1)) \times 100\% = 0.024\%.$$

Thus, quantization error = $0.024\% \times 5V = 1.2\text{mV}$.

Error due to 0.03% inaccuracy is

$$0.03\% \times 5V = 1.5\text{mV}.$$

Total Error = $1.2\text{mV} + 1.5\text{mV} = 2.7\text{mV}$.

INFORMAÇÕES

Segundo trabalho laboratorial:

1- Avaliação, próxima Quinta-Feira, dia 6 de Junho, as **14h00**

Último trabalho laboratorial:

1- Parte teórica, dia 11 de Junho (terça-feira), as **09h00-13h00**

2- Parte Laboratorial, dia 17 de Junho (em vez do dia 14 de Junho), as **14h00**

3- Proposta de data para Avaliação deste módulo, dia 3 de Julho, **14h00**

ESSENTIAL INSTRUMENTATION

TRANSDUCERS: SENSORS AND ACTUATORS

1 Introduction

2 Transducers: interfacing the real world

ESSENTIAL INSTRUMENTATION

TRANSDUCERS: SENSORS AND ACTUATORS

Transducer

a device that converts a primary form of energy into a corresponding signal with a different energy form

Primary Energy Forms: mechanical, thermal, electromagnetic, optical, chemical, etc.

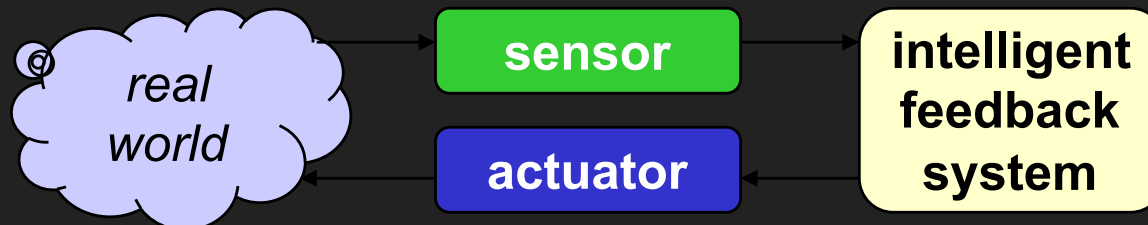
take form of a **sensor** or an **actuator**

Sensor (e.g., thermometer)

a device that detects/measures a signal or stimulus
acquires information from the "real world"

Actuator (e.g., heater)

a device that generates a signal or stimulus



ESSENTIAL INSTRUMENTATION

TRANSDUCERS: SENSORS AND ACTUATORS

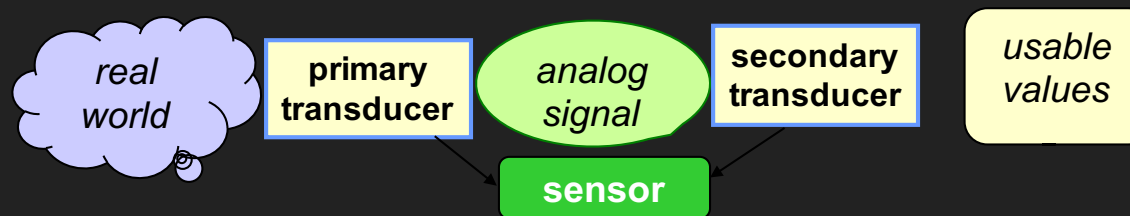
Typically interested in **electronic sensor**

convert desired parameter into electrically measurable signal

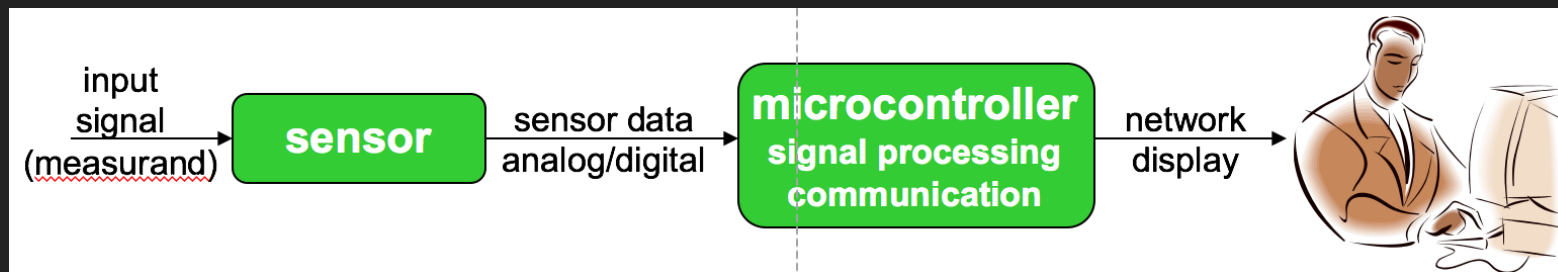
General Electronic Sensor

primary transducer: changes "real world" parameter into electrical signal

secondary transducer: converts electrical signal into analog or digital values



Typical Electronic Sensor System



ESSENTIAL INSTRUMENTATION

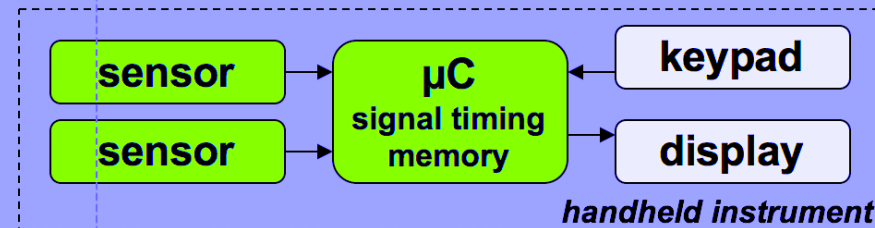
TRANSDUCERS: SENSORS AND ACTUATORS

Example Electronic Sensor Systems

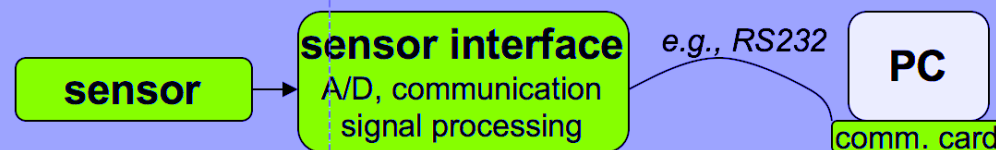
- Components vary with application

- digital sensor within an instrument

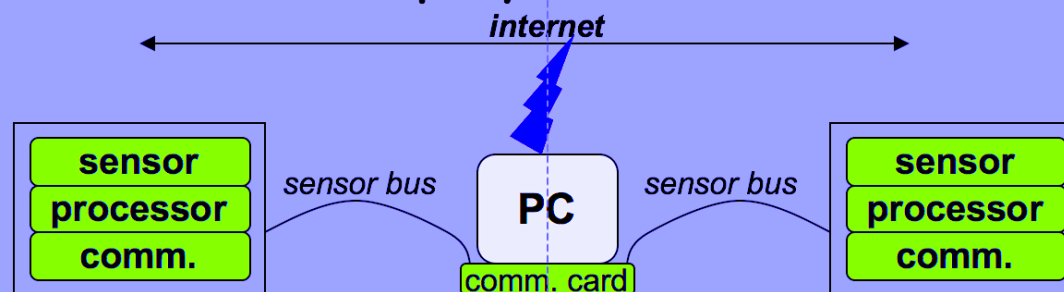
- microcontroller
 - signal timing
 - data storage



- analog sensor analyzed by a PC



- multiple sensors displayed over internet



TRANSDUCERS: SENSORS AND ACTUATORS

Primary Transducers

- **Conventional Transducers**

large, but generally reliable, based on older technology

- thermocouple: **temperature difference**
- compass (magnetic): **direction**

- **Microelectronic Sensors**

millimeter sized, highly sensitive, less robust

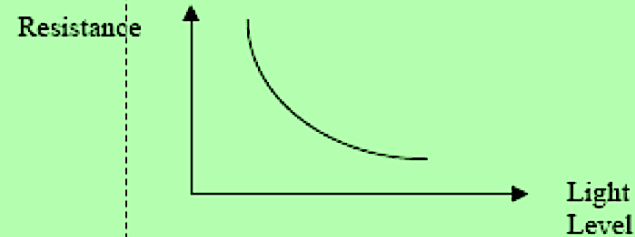
- photodiode/phototransistor: **photon energy (light)**
 - infrared detectors, proximity/intrusion alarms
- piezoresistive pressure sensor: **air/fluid pressure**
- microaccelerometers: **vibration, Δ -velocity (car crash)**
- chemical sensors: **O₂, CO₂, Cl, Nitrates (explosives)**
- DNA arrays: match **DNA sequences**

Example of Primary Transducers

- Light Sensor

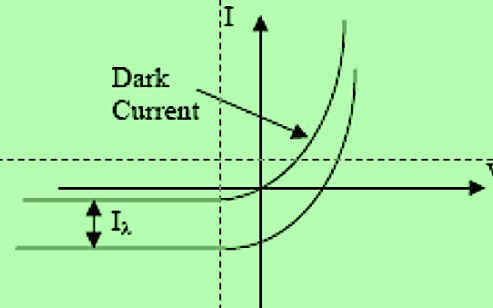
- photoconductor
 - light $\rightarrow \Delta R$

Photoconductor: (Light sensitive semiconductor resistor)



- photodiode
 - light $\rightarrow \Delta I$

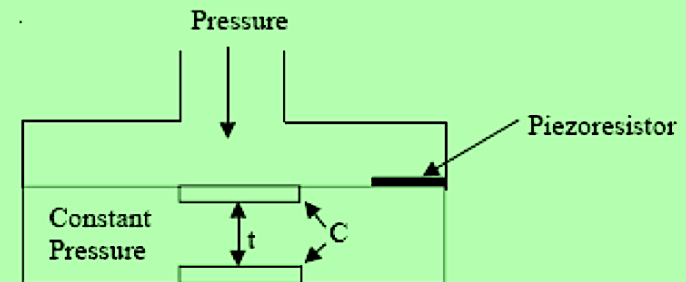
Photodiode:



$$I = I_0 [\exp(eV/kT) - 1] - I_\lambda$$

I_λ is proportion to the light level

- membrane pressure sensor
 - resistive (pressure $\rightarrow \Delta R$)
 - capacitive (pressure $\rightarrow \Delta C$)



$$C = \epsilon A / t$$

TRANSDUCERS: SENSORS AND ACTUATORS

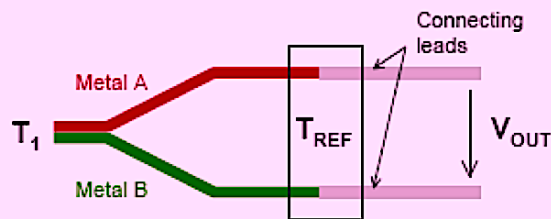
Displacement Measurement

- Measurements of size, shape, and position utilize **displacement sensors**
- Examples
 - diameter of part under stress (direct)
 - movement of a microphone diaphragm to quantify liquid movement through the heart (indirect)
- **Primary Transducer Types**
 - Resistive Sensors (Potentiometers & Strain Gages)
 - Inductive Sensors
 - Capacitive Sensors
 - Piezoelectric Sensors
- **Secondary Transducers**
 - Wheatstone Bridge
 - Amplifiers

TRANSDUCERS: SENSORS AND ACTUATORS

Temperature Sensor Options

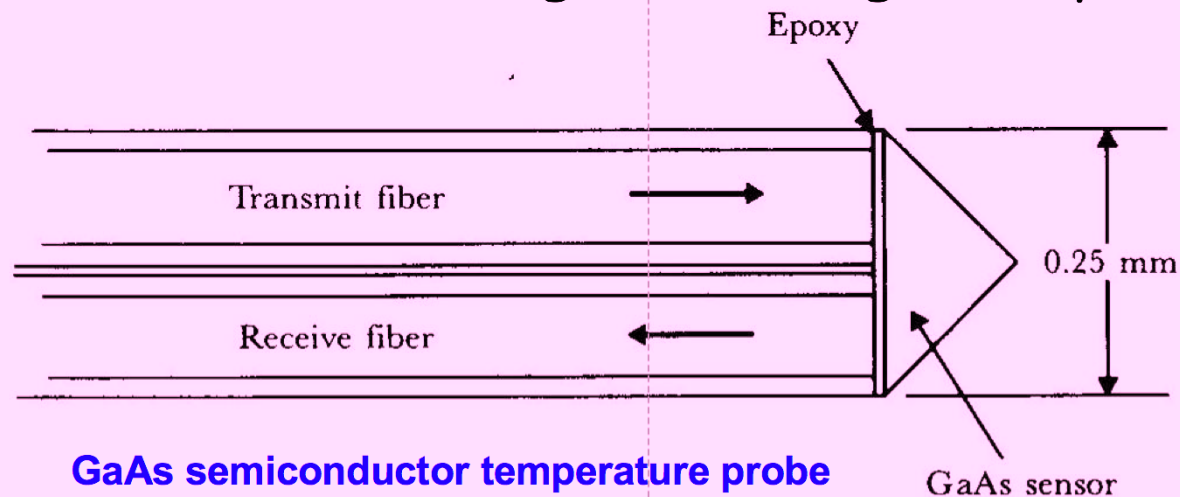
- Resistance Temperature Detectors (RTDs)
 - Platinum, Nickel, Copper metals are typically used
 - positive temperature coefficients $R_T = R_0 [1 + \alpha_1 T + \alpha_2 T^2 + \dots + \alpha_n T^n] \cong R_0 [1 + \alpha_1 T]$
- Thermistors ("thermally sensitive resistor")
 - formed from semiconductor materials, not metals $R_T = R_0 \exp \left[B \left(\frac{1}{T} - \frac{1}{T_0} \right) \right]$
 - often composite of a ceramic and a metallic oxide (Mn, Co, Cu or Fe)
 - typically have negative temperature coefficients
- Thermocouples
 - based on the Seebeck effect: dissimilar metals at diff. temps. → signal



	THERMOCOUPLES	RTD	IC
ACCURACY	Limits of error wider than RTD or IC Sensor	Better accuracy than thermocouple	Best accuracy
RUGGEDNESS	Excellent	Sensitive to strain and shock	Sensitive to shock
TEMPERATURE	-400 to 4200° F	-200 to 1475° F	-70 to 300° F
DRIFT	Higher than RTD	Lower than TC	
LINEARITY	Very non-linear	Slightly non-linear	Very linear
RESPONSE	Fast dependent on size	Slow due to thermal mass	Faster than RTD
COST	Rather inexpensive except for noble metals TCs, which are very expensive	More expensive	Low cost

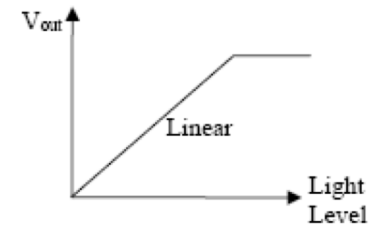
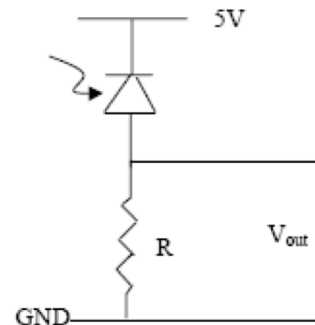
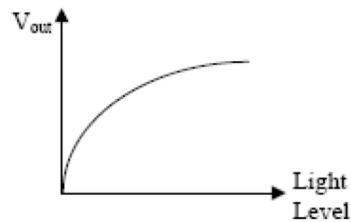
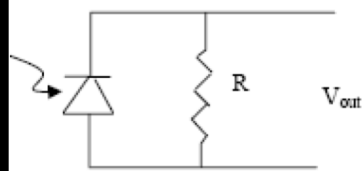
Fiber Optic Temperature Sensor

- Sensor operation
 - small prism-shaped sample of single-crystal undoped GaAs attached to ends of two optical fibers
 - light energy absorbed by the GaAs crystal depends on temperature
 - percentage of received vs. transmitted energy is a function of temperature
- Can be made small enough for biological implantation

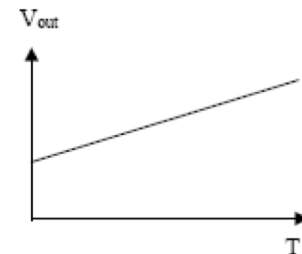
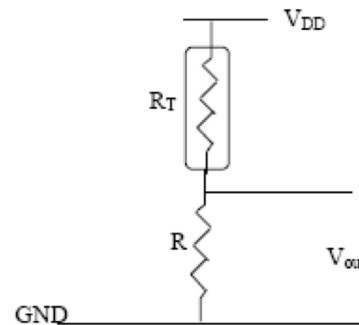


Passive Sensor Readout Circuit

- Photodiode Circuits

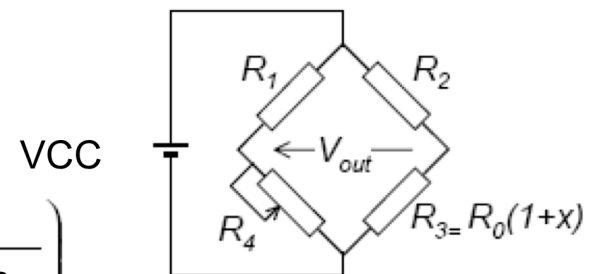


- Thermistor Half-Bridge
 - voltage divider
 - one element varies



- Wheatstone Bridge
 - R3 = resistive sensor
 - R4 is matched to nominal value of R3
 - If $R_1 = R_2$, $V_{out-nominal} = 0$
 - V_{out} varies as R_3 changes

$$V_{out} = V_{CC} \left(\frac{R_3}{R_2 + R_3} - \frac{R_4}{R_1 + R_4} \right)$$



Operational Amplifiers

- **Properties**

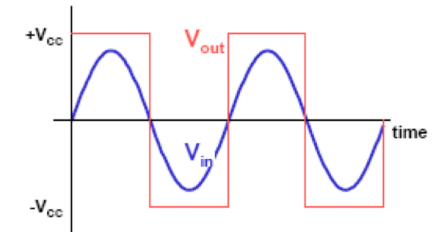
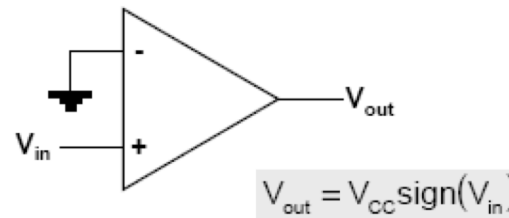
- open-loop gain: ideally infinite: practical values 20k-200k
 - high open-loop gain \rightarrow virtual short between + and - inputs
- input impedance: ideally infinite: CMOS opamps are close to ideal
- output impedance: ideally zero: practical values 20-100 Ω
- zero output offset: ideally zero: practical value $<1\text{mV}$
- gain-bandwidth product (GB): practical values $\sim\text{MHz}$
 - frequency where open-loop gain drops to 1 V/V

- **Commercial opamps** provide many different properties

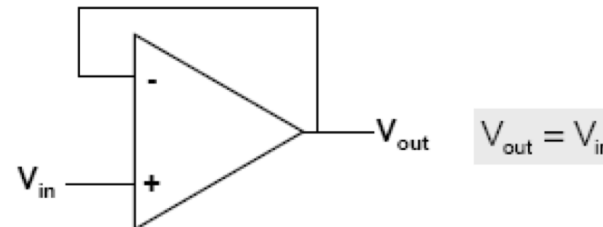
- low noise
- low input current
- low power
- high bandwidth
- low/high supply voltage
- special purpose: comparator, instrumentation amplifier

Basic Opamp Configuration

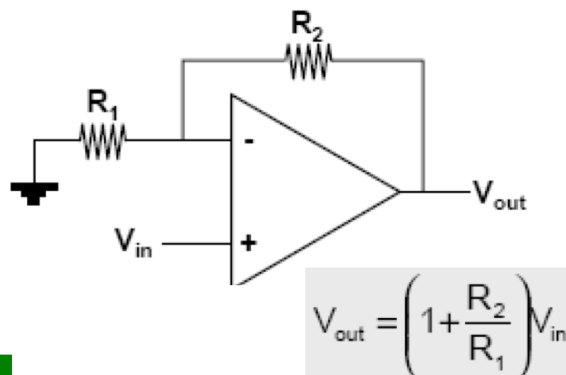
- Voltage Comparator
 - digitize input



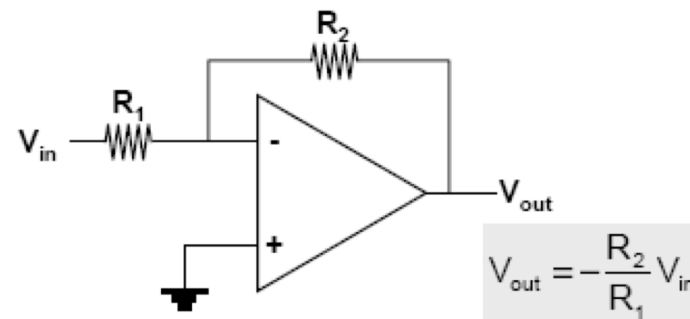
- Voltage Follower
 - buffer



- Non-Inverting Amp

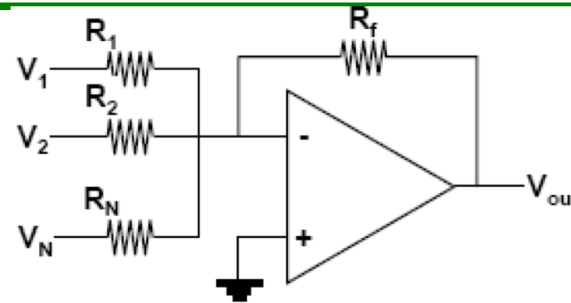


- Inverting Amp



More Opamp Configurations

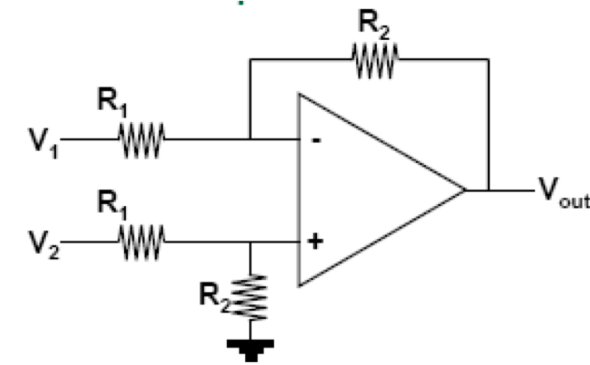
- Summing Amp



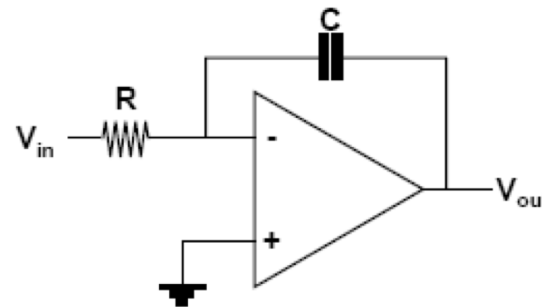
$$V_{out} = -\left(V_1 \frac{R_f}{R_1} + V_2 \frac{R_f}{R_2} + \dots + V_N \frac{R_f}{R_N} \right)$$

- Differential Amp

$$V_{out} = \frac{R_2}{R_1} (V_2 - V_1)$$



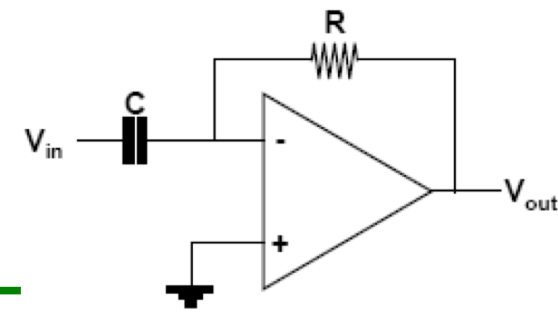
- Integrating Amp



$$V_{out} = -\frac{1}{j\omega CR} V_{in} = -\frac{1}{RC} \int V_{in} dt$$

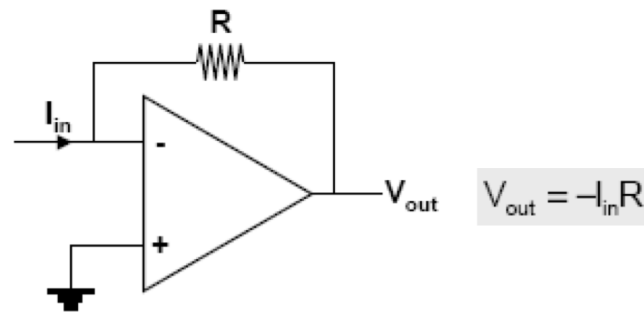
- Differentiating Amp

$$V_{out} = -\frac{R}{j\omega C} V_{in} = -RC \frac{dV_{in}}{dt}$$

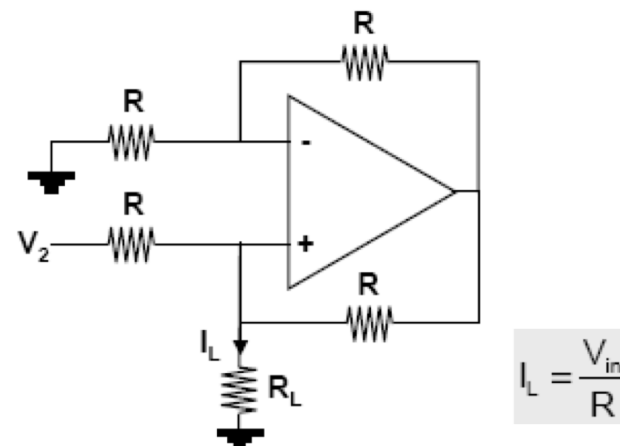


Converting Configuration

- Current-to-Voltage

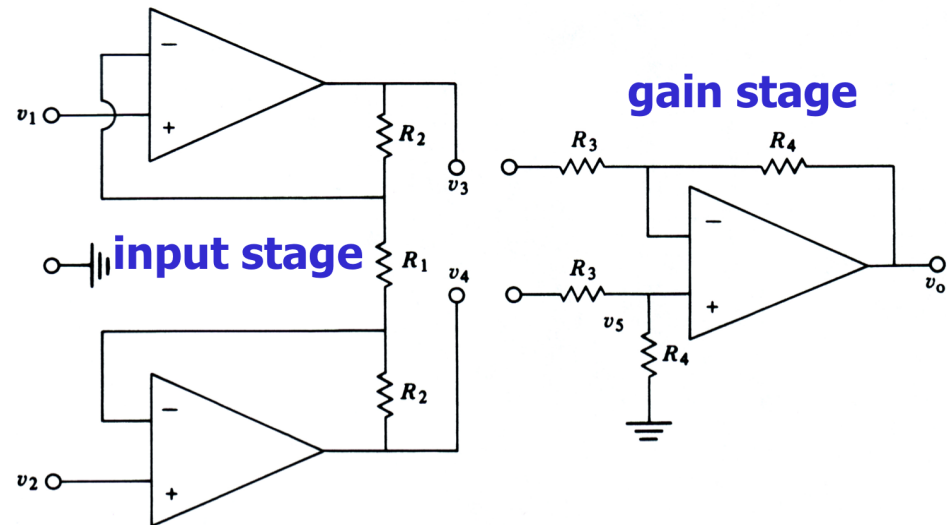


- Voltage-to-Current



Instrumentation Amplifier

- Robust differential gain amplifier
- Input stage
 - high input impedance
 - buffers gain stage
 - no common mode gain
 - can have differential gain



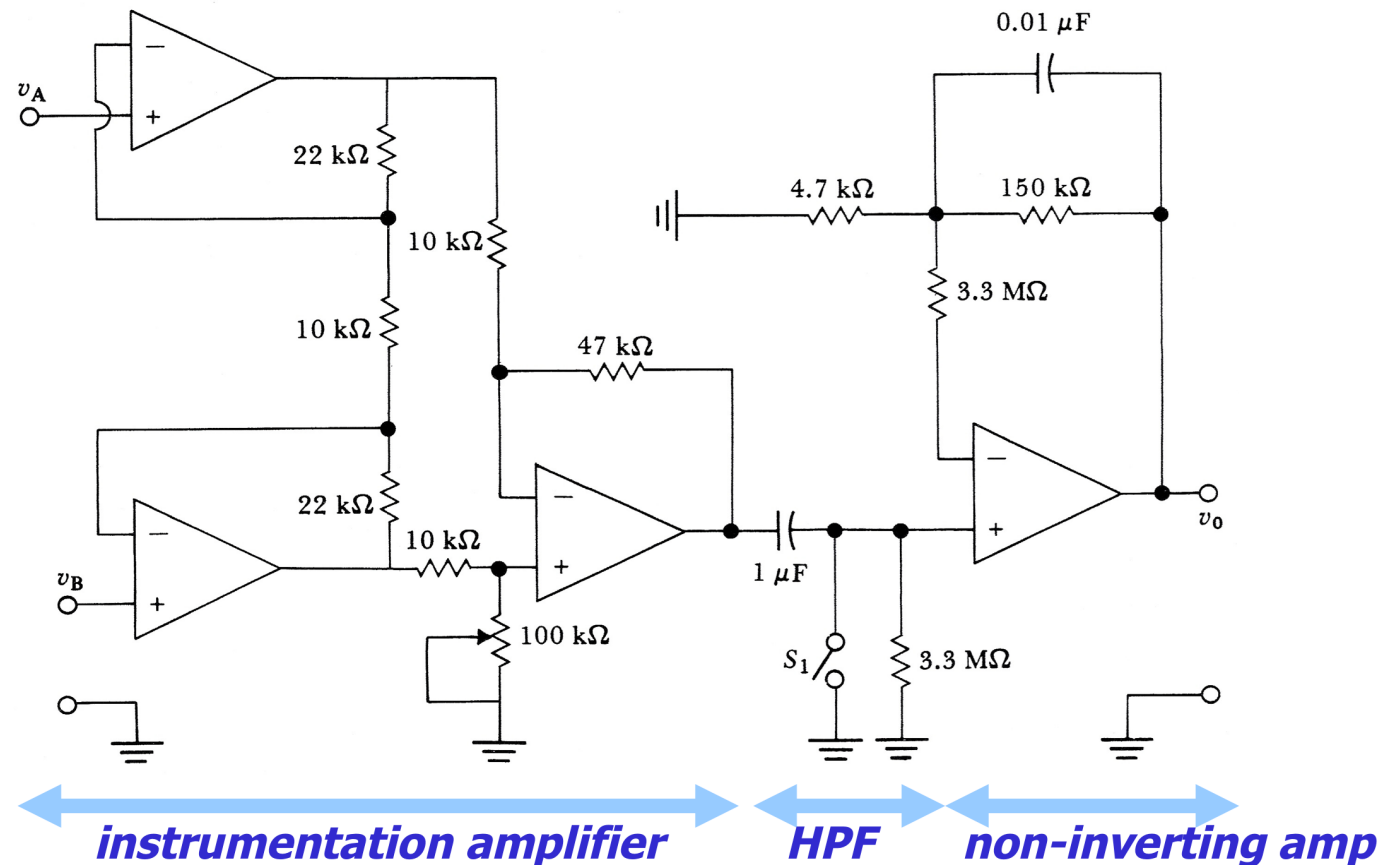
- Gain stage
 - differential gain, low input impedance

total differential gain

$$G_d = \frac{2R_2 + R_1}{R_1} \left(\frac{R_4}{R_3} \right)$$

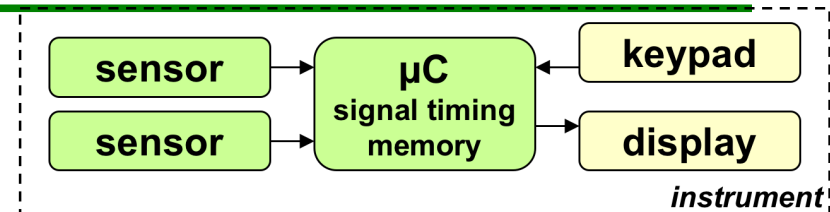
- Overall amplifier
 - amplifies only the differential component
 - high common mode rejection ratio
 - high input impedance suitable for biopotential electrodes with high output impedance

Instrumentation Amplifier w/ BP Filter



With 776 op amps, the circuit was found to have a CMRR of 86 dB at 100 Hz and a noise level of 40 mV peak to peak at the output. The frequency response was 0.04 to 150 Hz for ± 3 dB and was flat over 4 to 40 Hz. The total gain is 25 (instrument amp) \times 32 (non-inverting amp) = 800.

Connecting Sensors to Microcontrollers



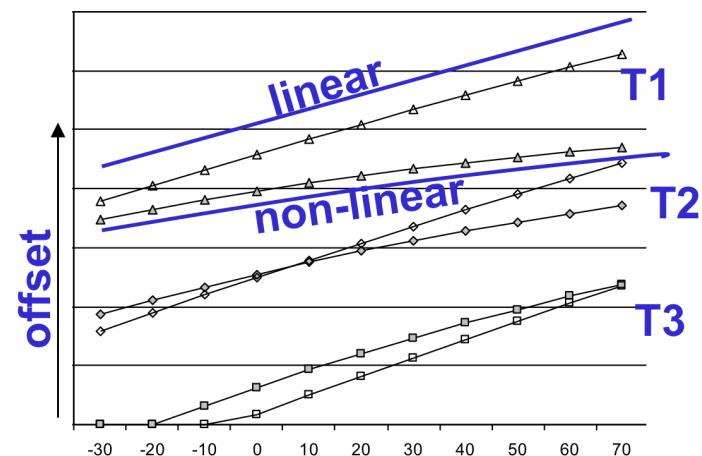
- Analog
 - many microcontrollers have a built-in A/D
 - 8-bit to 12-bit common
 - many have multi-channel A/D inputs
- Digital
 - serial I/O
 - use serial I/O port, store in memory to analyze
 - synchronous (with clock)
 - must match byte format, stop/start bits, parity check, etc.
 - asynchronous (no clock): more common for comm. than data
 - must match baud rate and bit width, transmission protocol, etc.
 - frequency encoded
 - use timing port, measure pulse width or pulse frequency

Connecting Smart Sensors to PC/Network

- "Smart sensor" = sensor with built-in signal processing & communication
 - e.g., combining a "dumb sensor" and a microcontroller
- Data Acquisition Cards (DAQ)
 - PC card with analog and digital I/O
 - interface through LabVIEW or user-generated code
- Communication Links Common for Sensors
 - asynchronous serial comm.
 - universal asynchronous receive and transmit (UART)
 - 1 receive line + 1 transmit line. nodes must match baud rate & protocol
 - RS232 Serial Port on PCs uses UART format (but at +/- 12V)
 - can buy a chip to convert from UART to RS232
 - synchronous serial comm.
 - serial peripheral interface (SPI)
 - 1 clock + 1 bidirectional data + 1 chip select/enable
 - I²C = Inter Integrated Circuit bus
 - designed by Philips for comm. inside TVs, used in several commercial sensor systems
 - IEEE P1451: Sensor Comm. Standard
 - several different sensor comm. protocols for different applications

Sensor Calibration

- Sensors can exhibit non-ideal effects
 - **offset**: nominal output \neq nominal parameter value
 - **nonlinearity**: output not linear with parameter changes
 - **cross parameter sensitivity**: secondary output variation with, e.g., temperature
- **Calibration** = adjusting output to match parameter
 - analog signal conditioning
 - look-up table
 - digital calibration
 - $T = a + bV + cV^2$,
 - T= temperature; V=sensor voltage;
 - a,b,c = calibration coefficients
- **Compensation**
 - remove secondary sensitivities
 - must have sensitivities characterized
 - can remove with polynomial evaluation
 - $P = a + bV + cT + dVT + e V^2$, where P=pressure, T=temperature



ESSENTIAL INSTRUMENTATION

SOURCES AND DETECTORS OF RADIATION

