

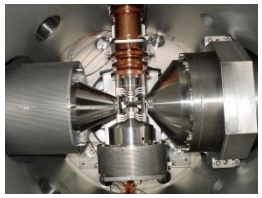
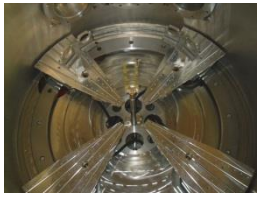

laboratoire de physique corpusculaire

Design of the preamp board for the silicon detectors

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Main specifications for preamplifier

Si detector main characteristics:

6 channels (5 strips + main signal on n side)
Detector capacitor ≈ 120 pF for each strip
Leakage current ≤ 10 nA/strip (assumed, but no value yet)
Rise time ≈ 10 - 20 ns (not crucial)

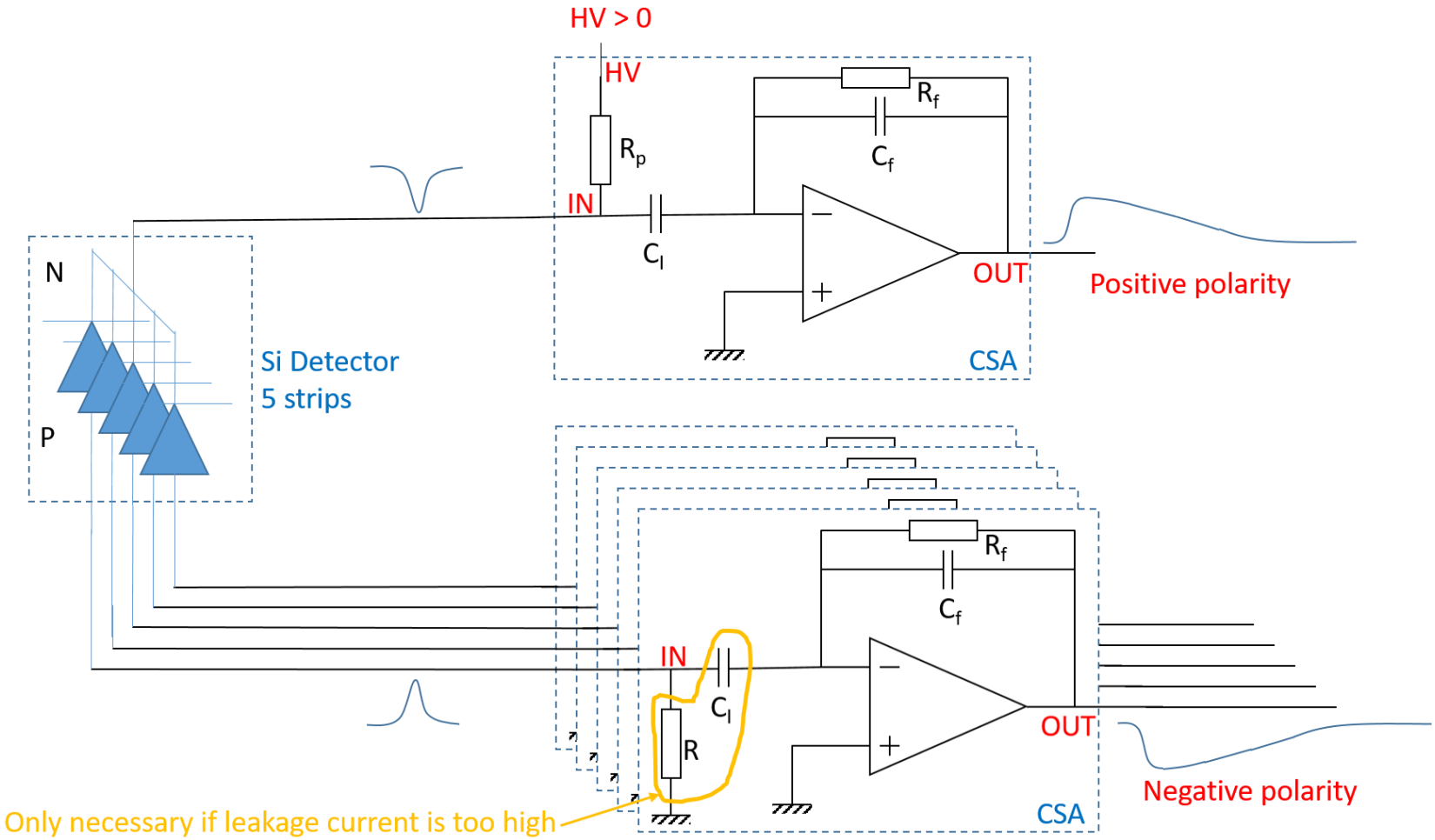
Charge Sensitive Amplifier main requirements:

Resolution in energy < 5 keV FWHM
Energy max ~ 6-7 MeV_{Si}
Counting rate max ≤ 100 events/s
Integral Non Linearity < 0.1 %

Preamp boards requirements:

Total of 48 channels → Low power consumption & compact boards
Cooled environment → Low temperature compatibility

Overview for one detector

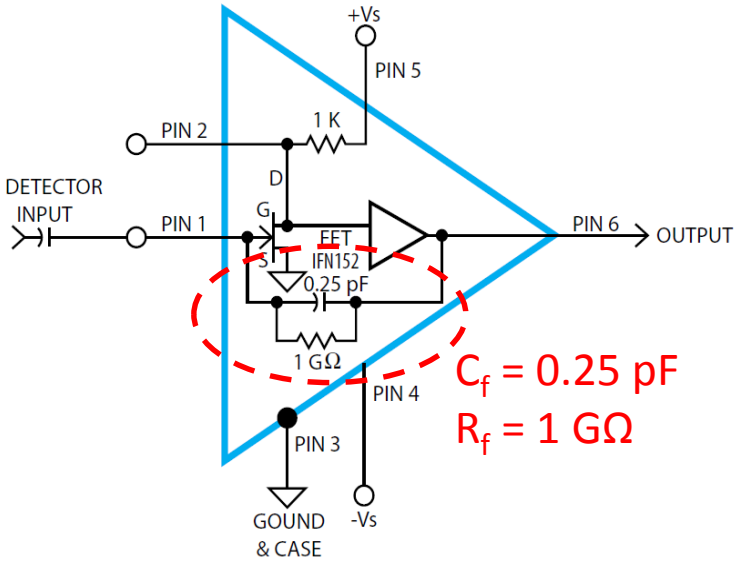


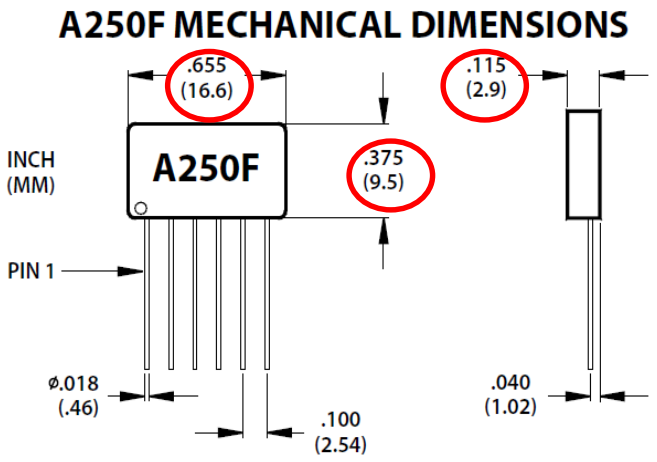
Choice of CSA : the state of the art

Main features of A250F (AMPTEK) :

Positive and negative signal processing
Noise : 5 keV_{Si} FHWM @ Cd = 130 pF and 25 °C
Integral Nonlinearity < 0.03 %
Power : 32 mW typical
Operating temperature min : -55 °C
Very small size

cost ≈ 600 $ per unit

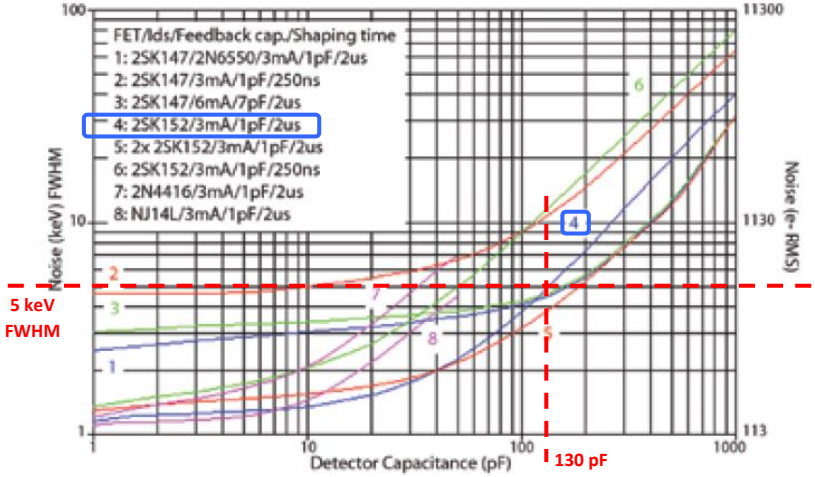




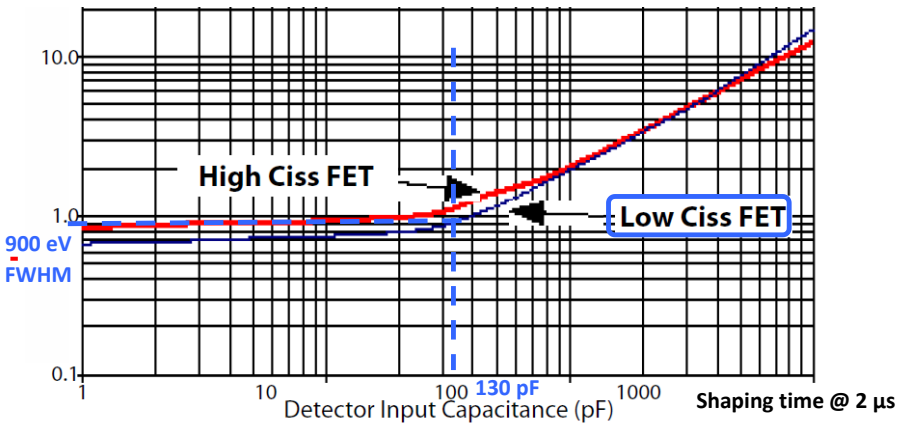
Noise Equivalent Charge with A250F

Estimation of NEC for 130 pF (Cd = 120 pF + Ccoax = 10 pF):

@ 25 °C



@ -50 °C

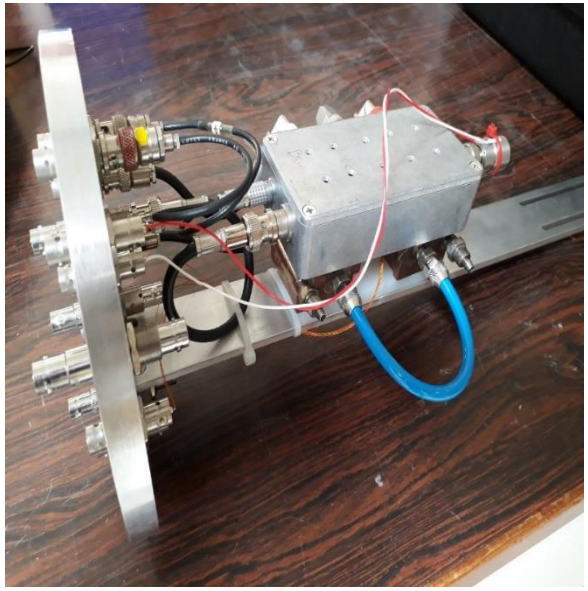


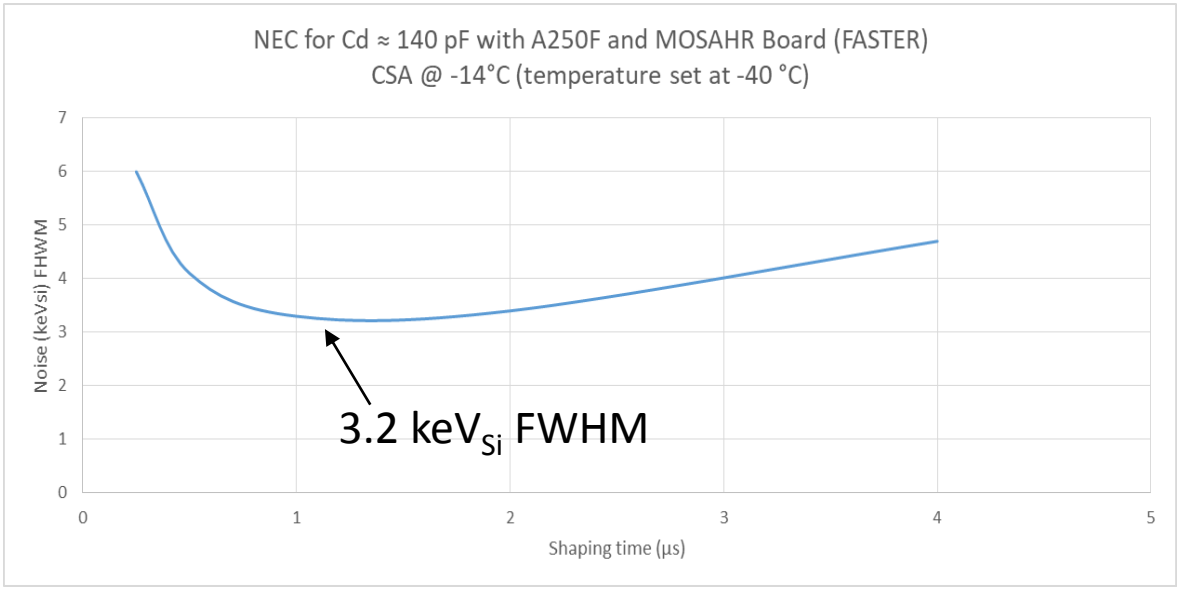
According to these graph of NEC, we can give the expected NEC for differents temperatures :

5 keV_{Si} FWHM @ 25°C 3.5 keV_{Si} FWHM @ -20°C 2.3 keV_{Si} FWHM @ -40°C

The front-end electronic must be cooled !

Measurement of Noise Equivalent Charge for A250F (At LPC)





Testbench (cooling with alcool glycol under vacuum)

This measured value is in agreement with the previously theoretical estimated value (3.5 keV$_{Si}$ FWHM @ -20°C).

First prototype board : AMPTEK Version

Main features :

6 channels with 6 charge sensitive amplifiers A250F

For each channel :

Cf ≈ 0.25 pF ⇨ 175 mV/MeV_{Si} ⇨ 1.05 V for 6 MeV_{Si} in CSA output

Rf ≈ 1 GΩ ⇨ Decay time ≈ 250 µs

2 amplifications stages allowing :

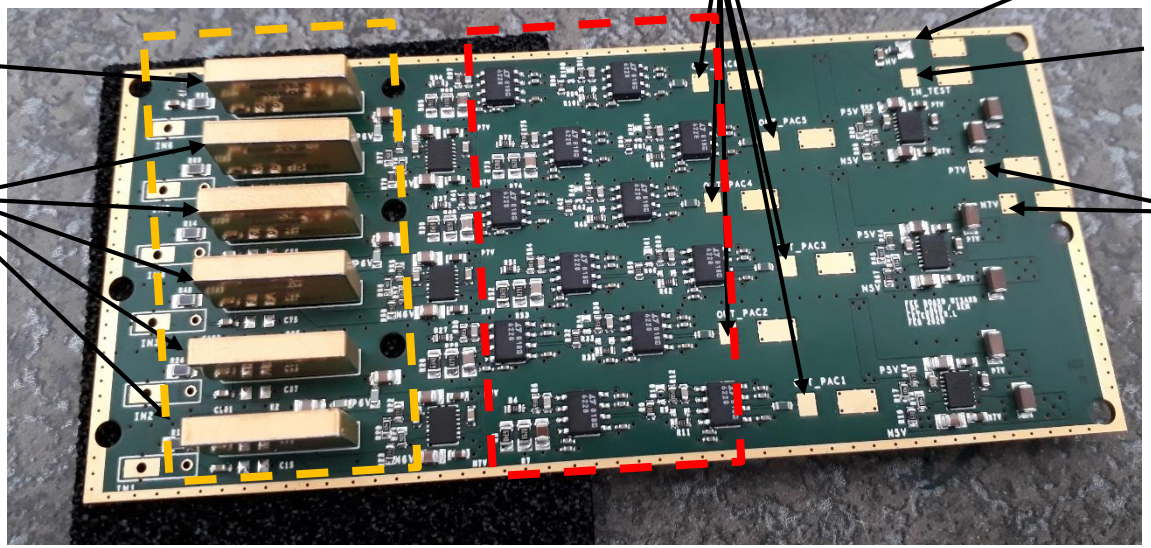
-to amplify the CSA output by a factor of 7.5 ⇨ 7.87 V for 6 MeV_{Si}

-to center the output signal to use input FASTER in ± 5 V

-to choose the polarity of output

Power consumption ≈ 550 mW / channel (additional amplification stages)

First prototype board : AMPTEK Version



Board size: 54mm x 120mm

To be checked asap …

Another choice of CSA to test :

Main features of A1422H (CAEN) version F2 :

Positive and negative signal processing
Low noise ≈ 3 keV @ Cd =130pF & 25 °C
Integral Nonlinearity < 0.05 %
Cost ≈ 200 € per unit

Power : 288 mW typical but more gain
Size : 39 x 20 x 3 mm
Operating temperature min : ?

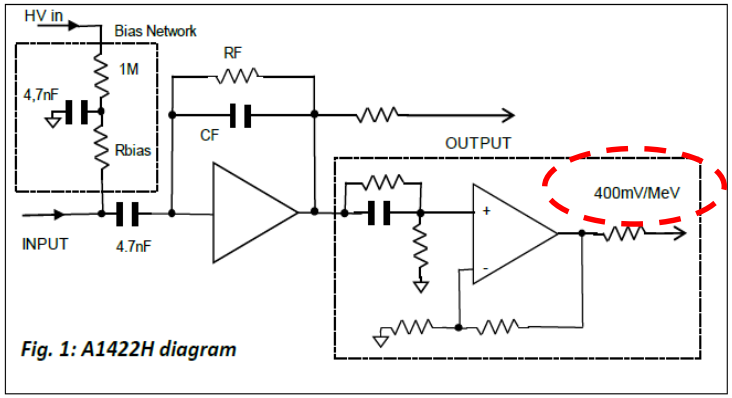


Fig. 1: A1422H diagram

Hybrid pin out

Pin 1	Input/Detector
Pin 2	GND
Pin 3	Test input - 1pF or 10 pF (5 mV/MeV)
Pin 4	GND
Pin 5	NC
Pin 6	High Voltage Bias
Pin 7	NC
Pin 8	GND
Pin 9	+12V Power Supply
Pin 10	GND
Pin 11	GND
Pin 12	-12V Power Supply
Pin 13	GND
Pin 14	NC
Pin 15	Output/Energy