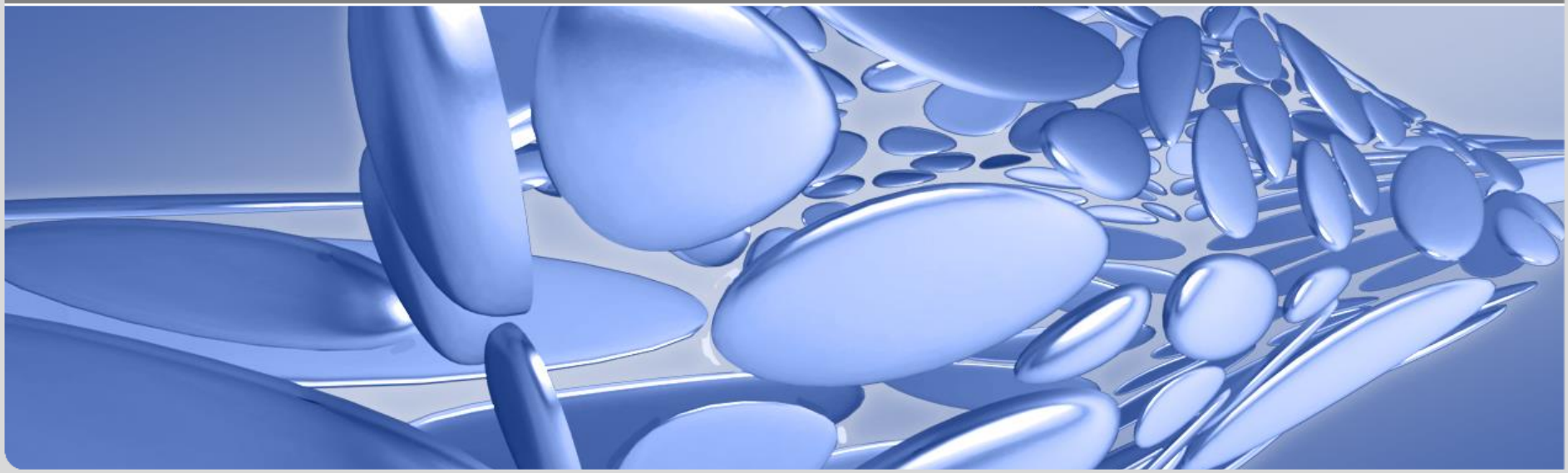
High-voltage monolithic active pixel detectors for the mighty tracker

Ivan Peric

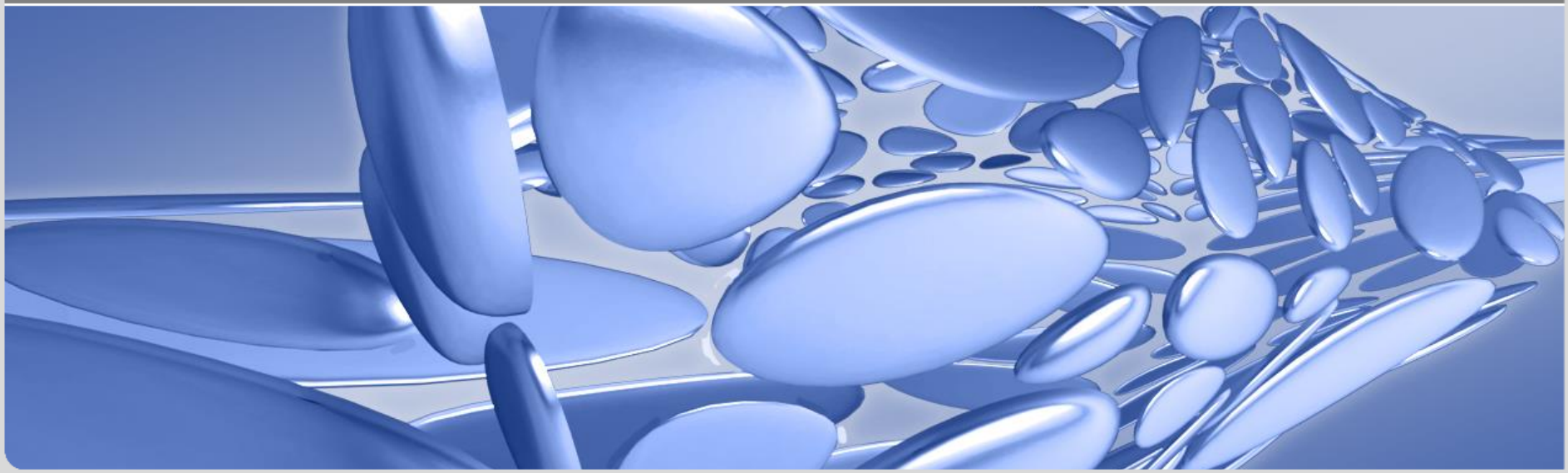


- Our Group
- HVMAPS technology
- Mighty pixel
- Project timeline

Our group

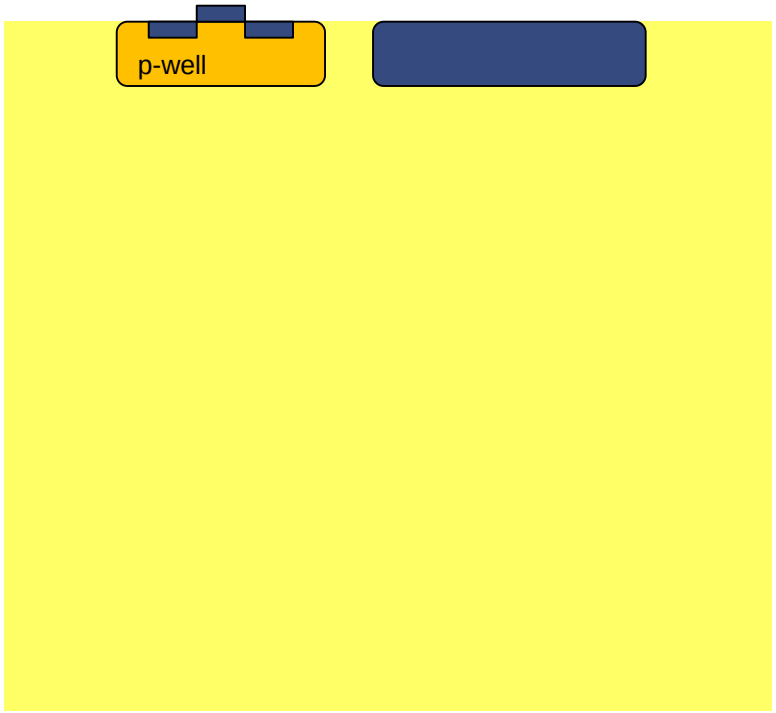
- ASIC and Detector Lab (ADL) develops integrated electronics and sensors for particle physics experiments and medicine
- Contribution to Belle II and Mu3e pixel detectors
- R&D for ATLAS and CLIC detectors
  - Development and production of the ICs for the readout of the Belle II Pixel Detector.
  - Developed the monolithic sensor chip for Mu3e pixel detector (MuPix) from the first small prototype (2011) to the final size MuPix10 (2020)
  - Developed (2011 - 2020) the radiation hard depleted HVCMOS pixel sensors for ATLAS (ATLASPix)
  - Detector development for COMPASS, planned is to use a variant of MuPix or ATLASPix
- Team: 1 professor, 1 researcher with permanent position, 1 postdoc, 5 doctoral students
- Equipment: ASIC design software tools, PCB design software, the equipment for ASIC tests such as wafer prober, voltage supplies, oscilloscopes

The high-voltage monolithic active pixel sensors (HV-MAPS)

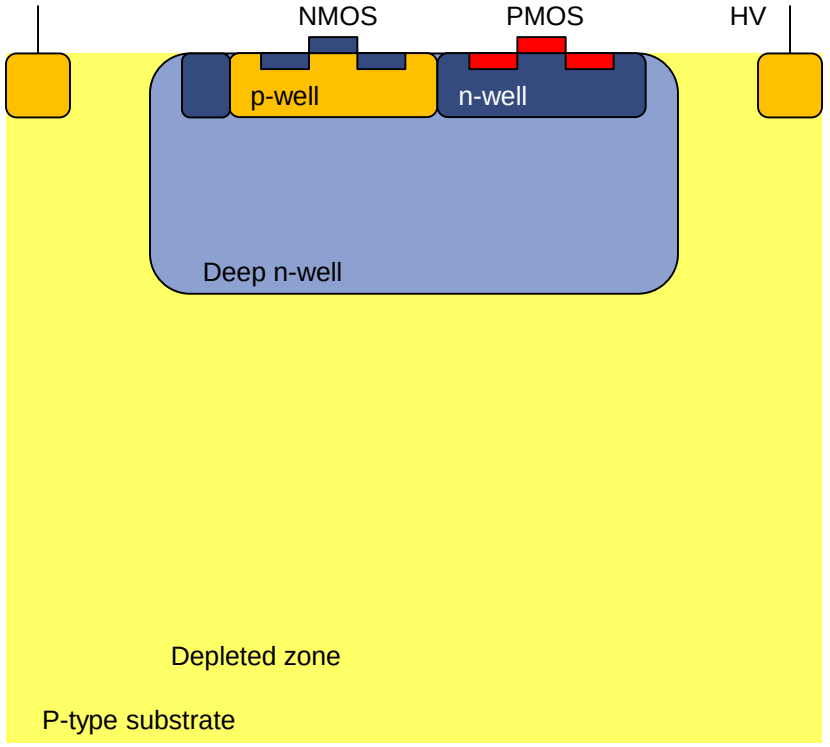


- HVMAPS is a sensor type that we developed
- It can be implemented in standard CMOS technologies

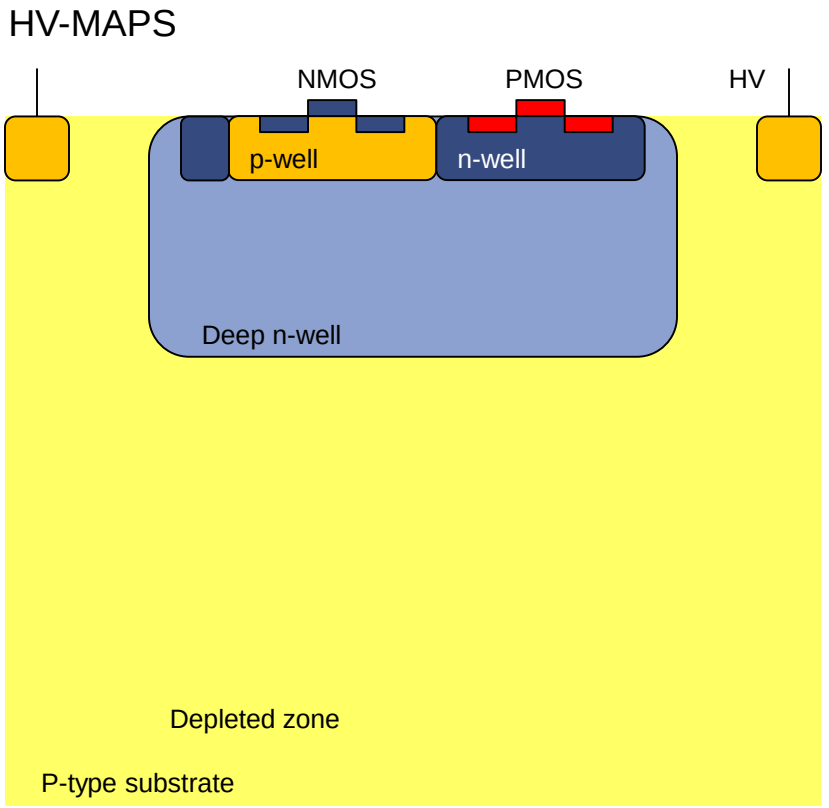
Standard CMOS sensor



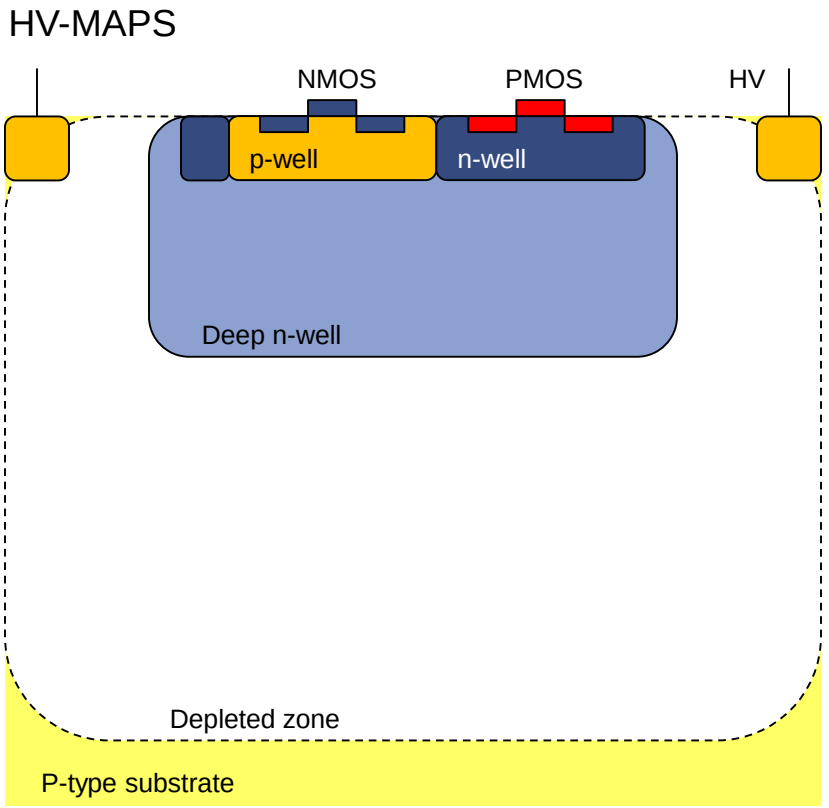
HV-MAPS



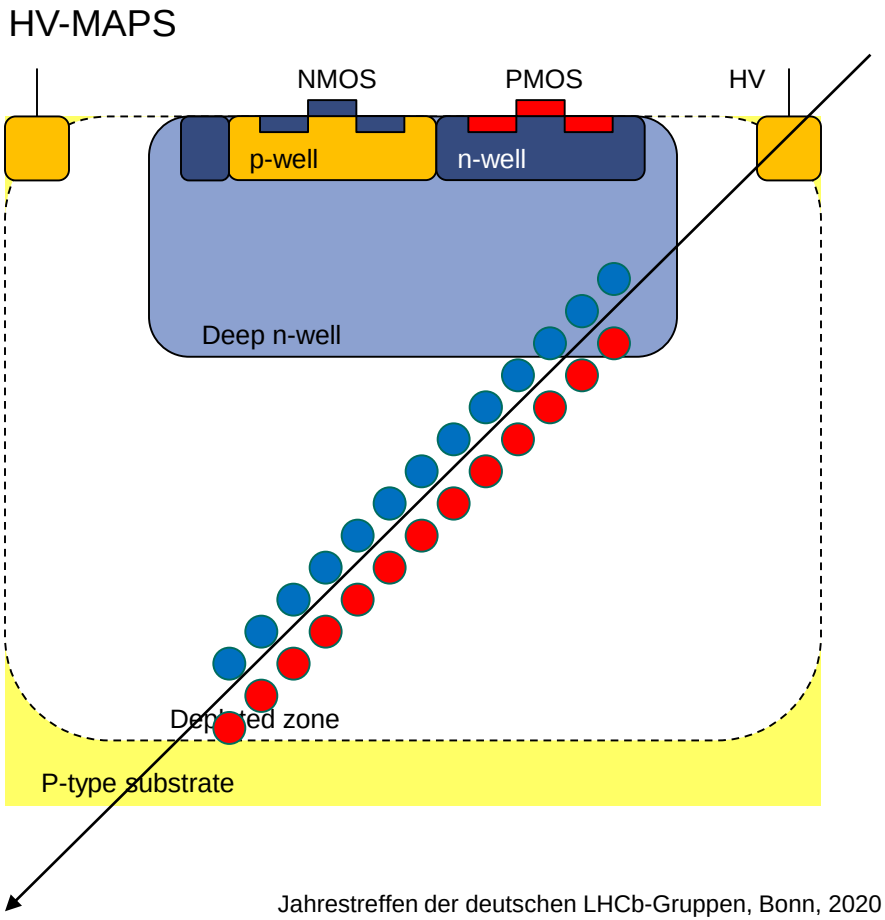
- Pixels are based on the so called “smart diode” – the readout electronics is placed inside the n-region of a sensor diode (the cathode)
- The deep-n-well fulfils two tasks:
- 1. Local substrate for electronics (isolated from p-substrate)
- 2. Charge collecting electrode



- The p-substrate region below the deep n-well is depleted by setting substrate to negative HV



- Average MIP signals are >5000e



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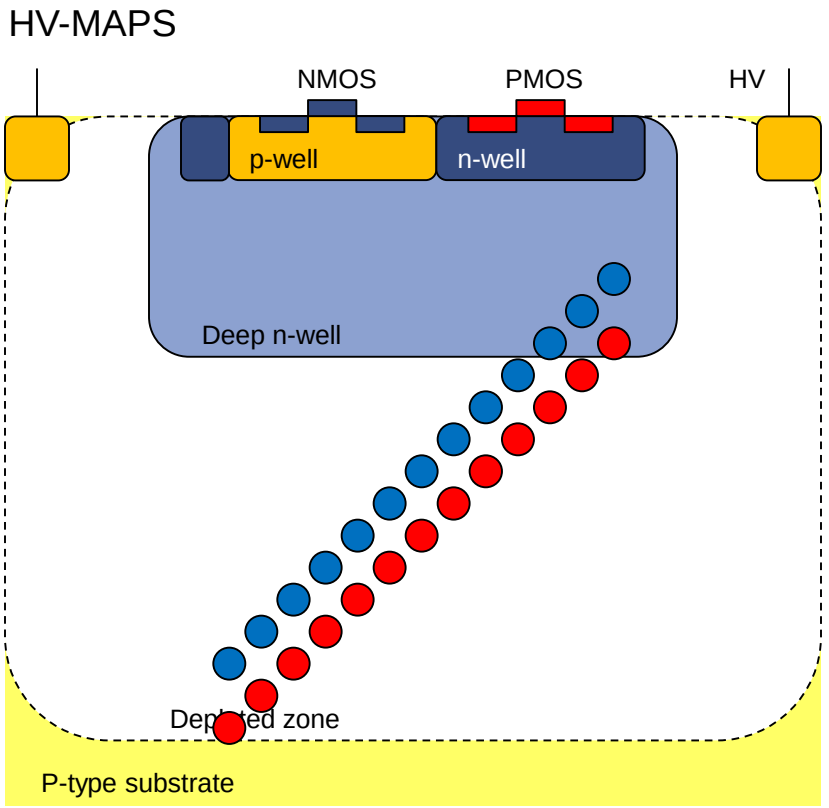

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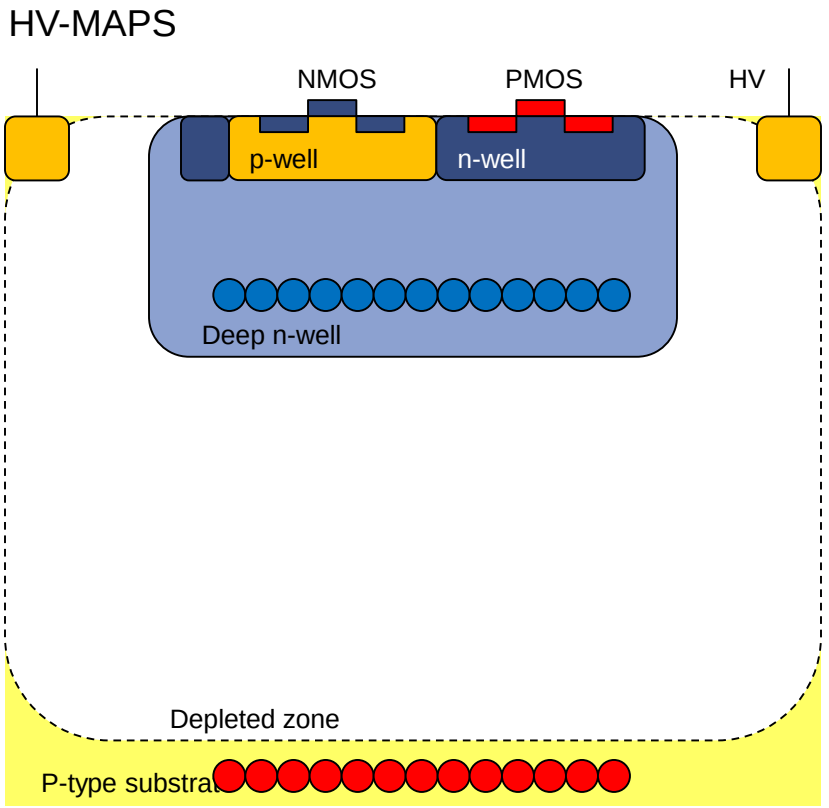
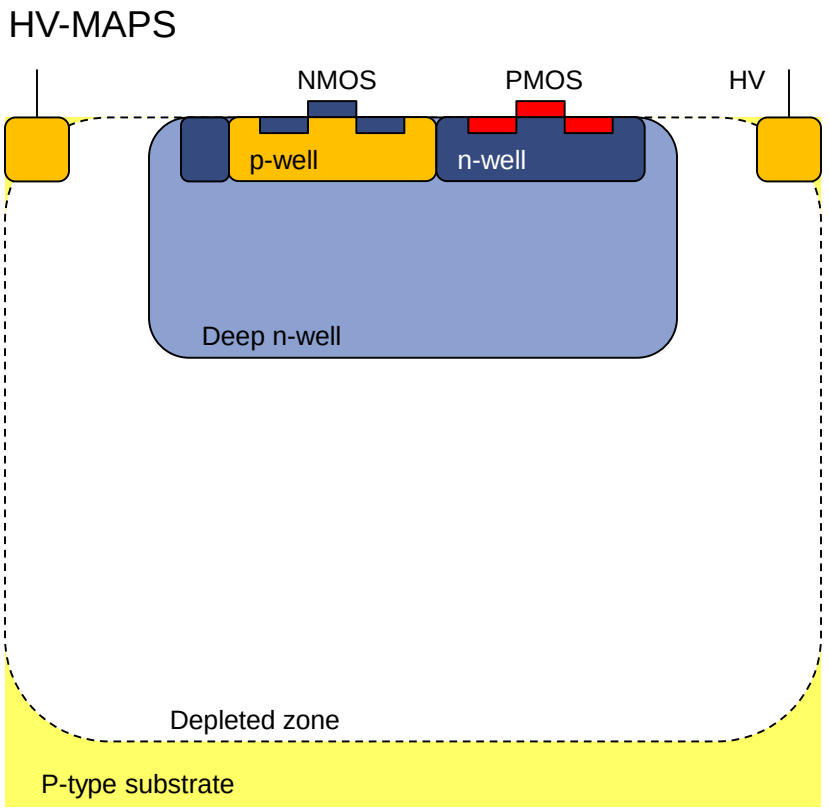
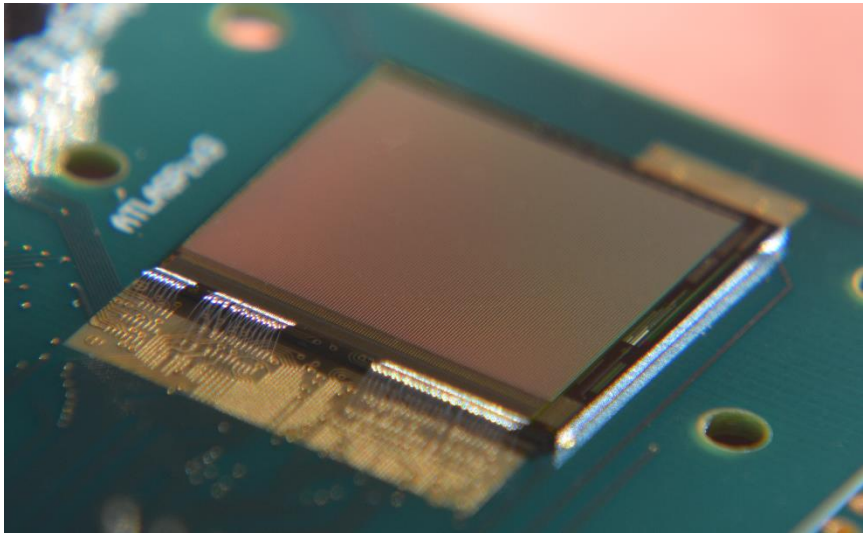
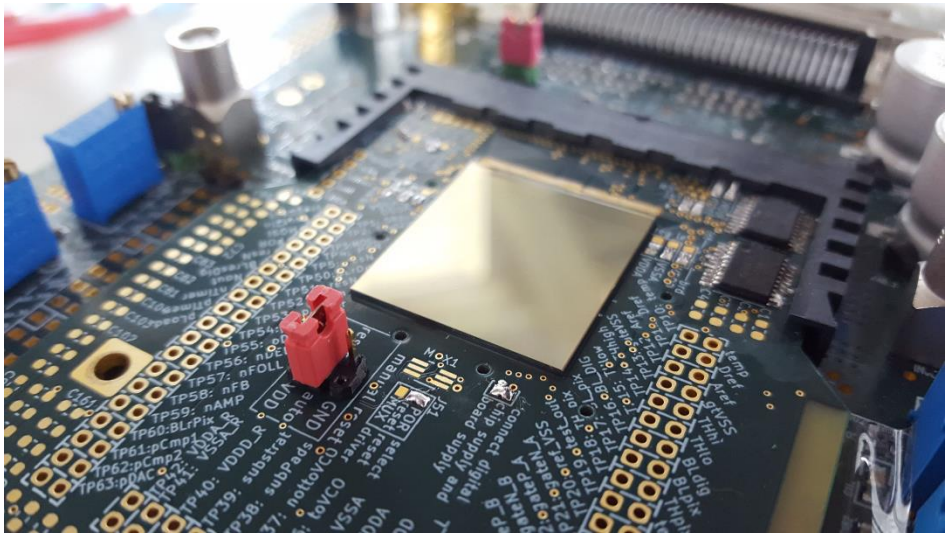


- Radiation tolerant
- Can be implemented in standard IC-processes -> not expensive
- Can be thin
- Can have a high time resolution



- First HVMAPS publication in 2007 [1]
- R&D development (5 chip submissions)
- Development for ATLAS (20)
- Development for Mu3e (9)
- Development for CLIC (3)
- Latest achievements: ATLASpix3 (left) and MuPix10 (right)
- Reticle size sensors with binary zero-suppression and bunch crossing identification (time-stamping)





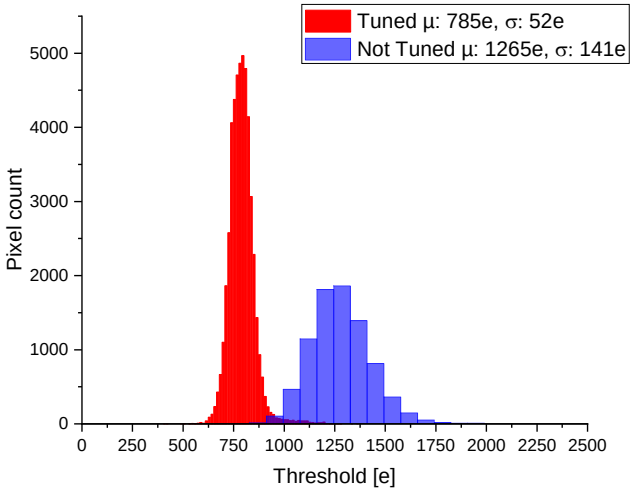
- [1] I. Peric, A novel monolithic pixelated particle detector implemented in high-voltage CMOS technology, Nucl. Instrum. Meth. A582, pp. 876--885, 2007.
- [2] ATLASPix3: https://adl.ipe.kit.edu/downloads/ATLASPIX3_um_v1.pdf
- [3] MuPix10: H. Augustin, et al., The MuPix sensor for the Mu3e experiment, Nucl. Instrum. Meth. A979, 2020. https://doi.org/10.1016/j.nima.2020.164441

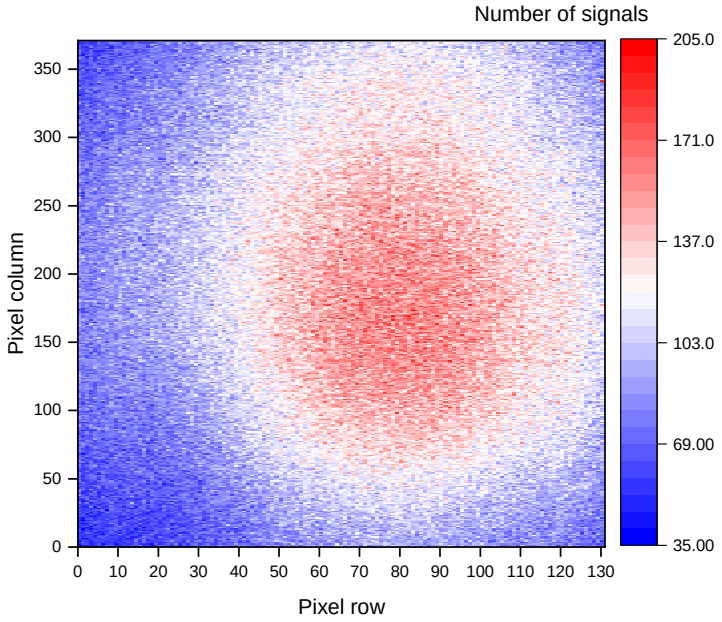
Properties of ATLASPix3 and MuPix10

- Sensor thickness (µm) 250 (ATLASPix3) 50 (MuPix10)
- Pixel Size (µm) 50 x 150 (ATLASPix3) 80 x 80 (MuPix10)
- Time Resolution (ns RMS) < 5 (after correction) (ATLASPix3) (required 4ns)
- Power consumption (W/cm^2) 0.15 (ATLASPix3)
- Data transmission (Gbps) 1 x 1.28 (ATLASPix3) 3 x 1.6 (MuPix10)
- Output Protocol Aurora 64b66b (ATLASPix3) Aurora 8b10b (MuPix10)
- Radiation tolerance TID (MRad) 100 (measured on ATLASPix1 [1], to be tested)
- Radiation tolerance NIEL (1 MeV n_{eq}/cm^2) 5 x 10^{15}

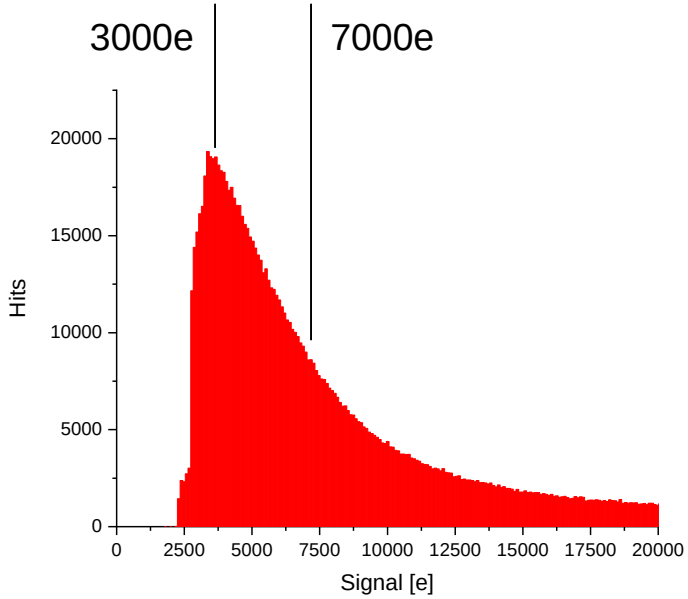
- [1] M. Kiehn, Performance of the ATLASPix1 pixel sensor prototype in ams aH18 CMOS technology for the ATLAS ITk upgrade, JINST C08013, 2020.

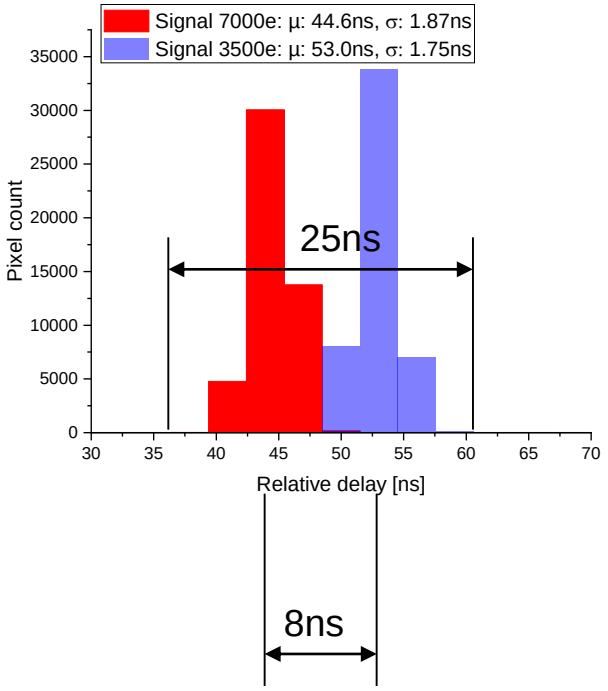
- Efficiency measured in PSI test beam about 99.6%
- Noise rate/pixel about 1.9Hz (pixels were not tuned)
- Time resolution for single pixel 8.1ns (RMS) uncorrected and 3.4ns (RMS) full corrected (required 4ns)
- Signal to noise ratio ~ 50
- MIP MPW signal >3600e
- Production yield so far ~ 85%



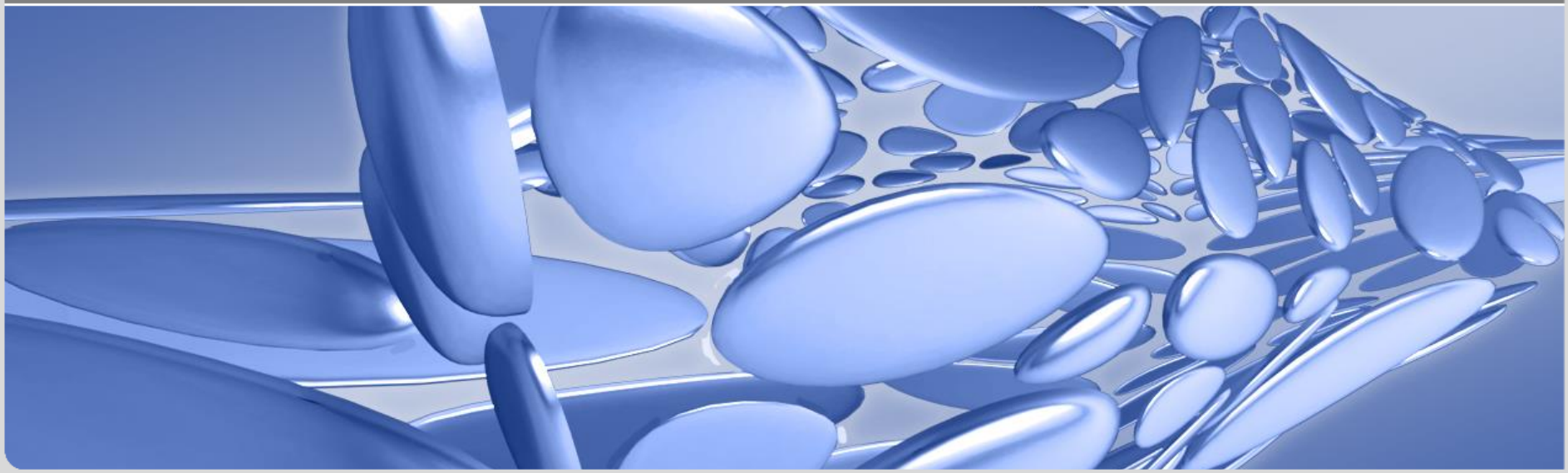


- Achieving required time resolution requires carefully controlling the time-walk (i.e. the time variation in the individual pixel) and the time-spread (time variation across the pixels in the chip)
- The sensor can be tuned in order to reduce time spread. So far test beam measurements were done with untuned chips. Corrections were done in software



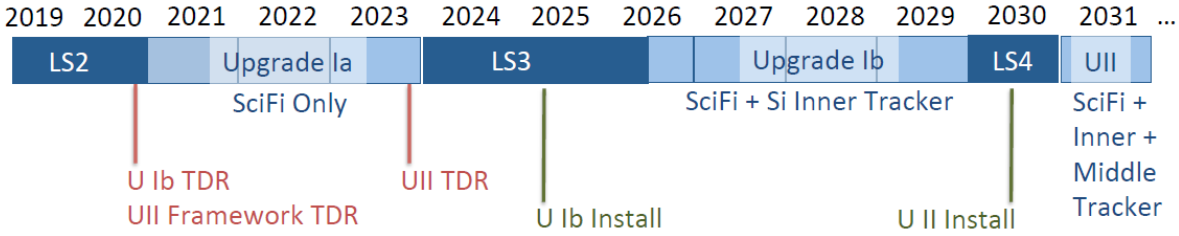


The Mighty Tracker

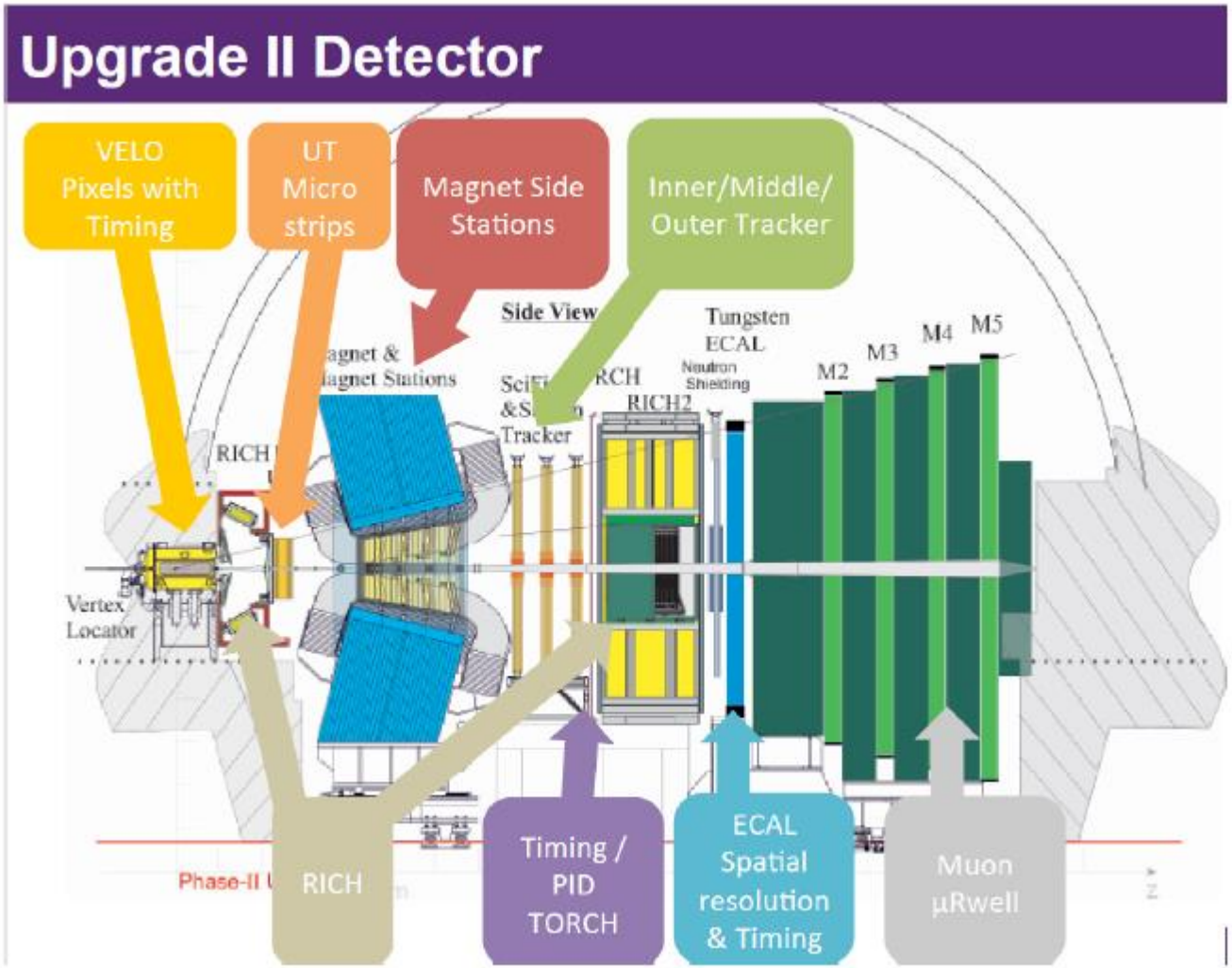


- Mighty Tracker: Design studies for the downstream silicon tracker in Upgrade Ib and II (LHCb-INT-2019-007)
- Preliminary Specification of a HV-CMOS Pixel Chip for LHCb Upgrade II

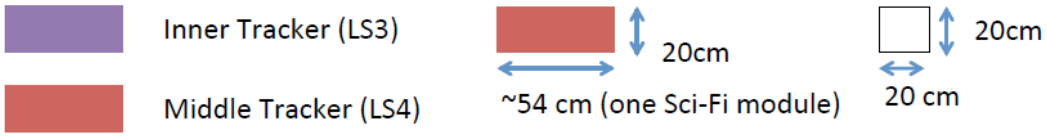
- A new silicon detector is proposed to be installed in the inner part of the LHCb downstream tracking stations.
- Two steps:
- 1. During LS3, scheduled for 2025-2027, the inner part of the SciFi detector will be replaced with silicon sensors
- 2. The area covered by silicon will expand further during LS4 which is scheduled for 2031
- The combined hybrid technology silicon and SciFi tracker is called the Mighty Tracker (from Middle and Inner Tracker), and is composed of an Inner Tracker, Middle Tracker and SciFi region
- The baseline technology for the new Inner and Middle tracker is a High-Voltage Monolithic Active Pixel Sensor (HV-MAPS)

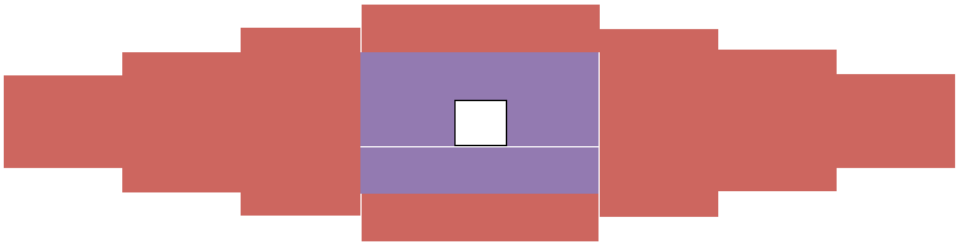


- Where is it placed?



- Detector area and structure

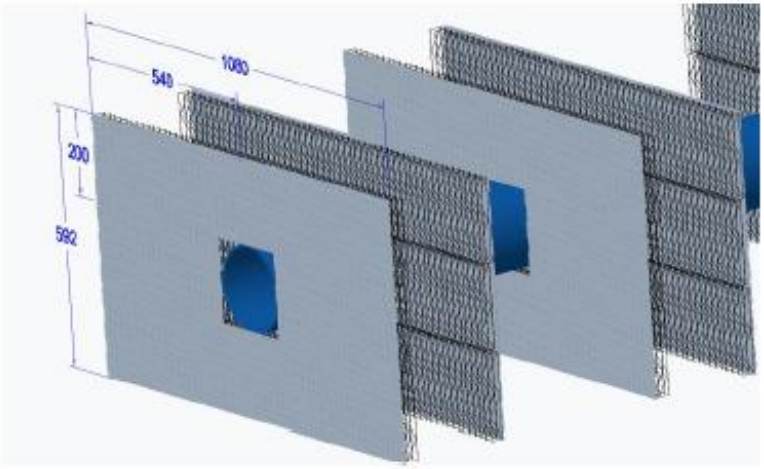


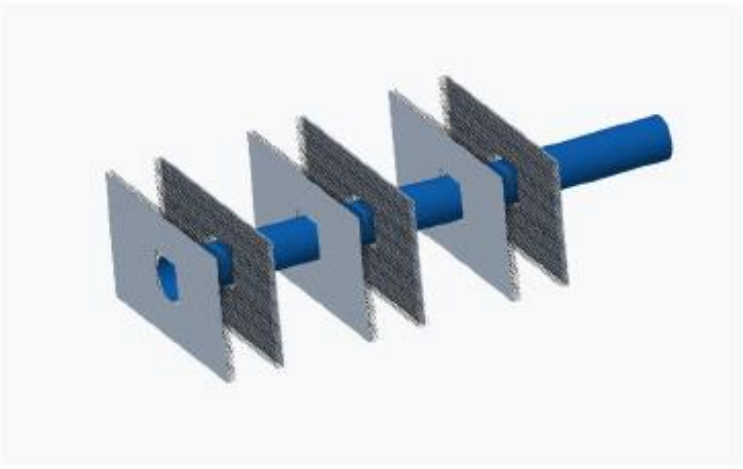


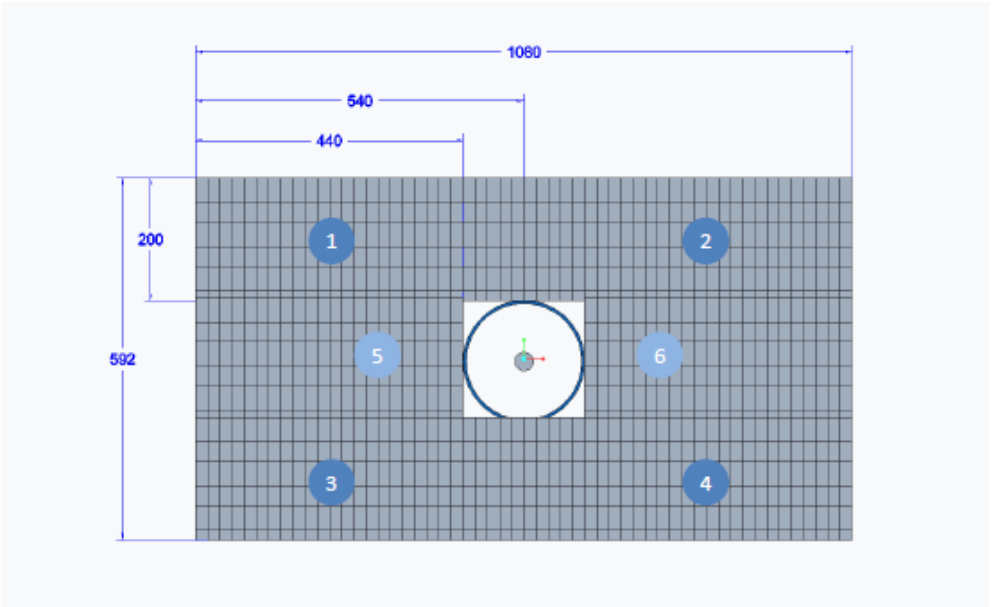
IT
Area per layer = 6 lots of 20x54 cm = 0.7 m^2 (minus beam hole)
Total Area = 6 layers of 0.7 m^2 = 3.9 m^2 (minus beam hole)

IT+MT
Area per layer = 28 lots of 20x54 cm = 3.0 m^2 (minus beam hole)
Total Area = 6 layers of 0.7 m^2 = 18.1 m^2 (minus beam hole)

- Inner tracker structure

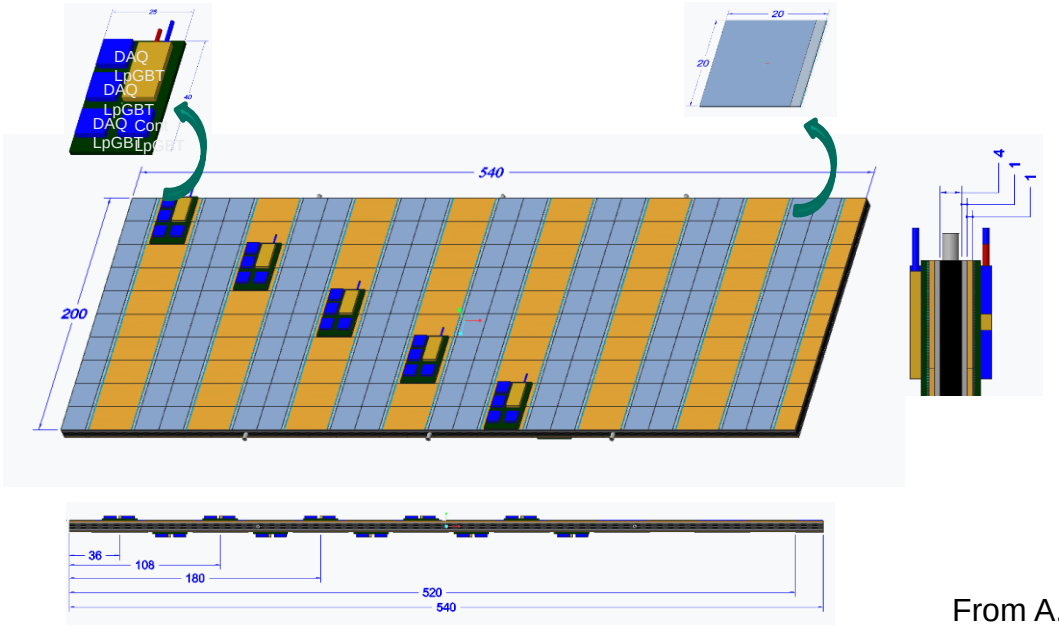






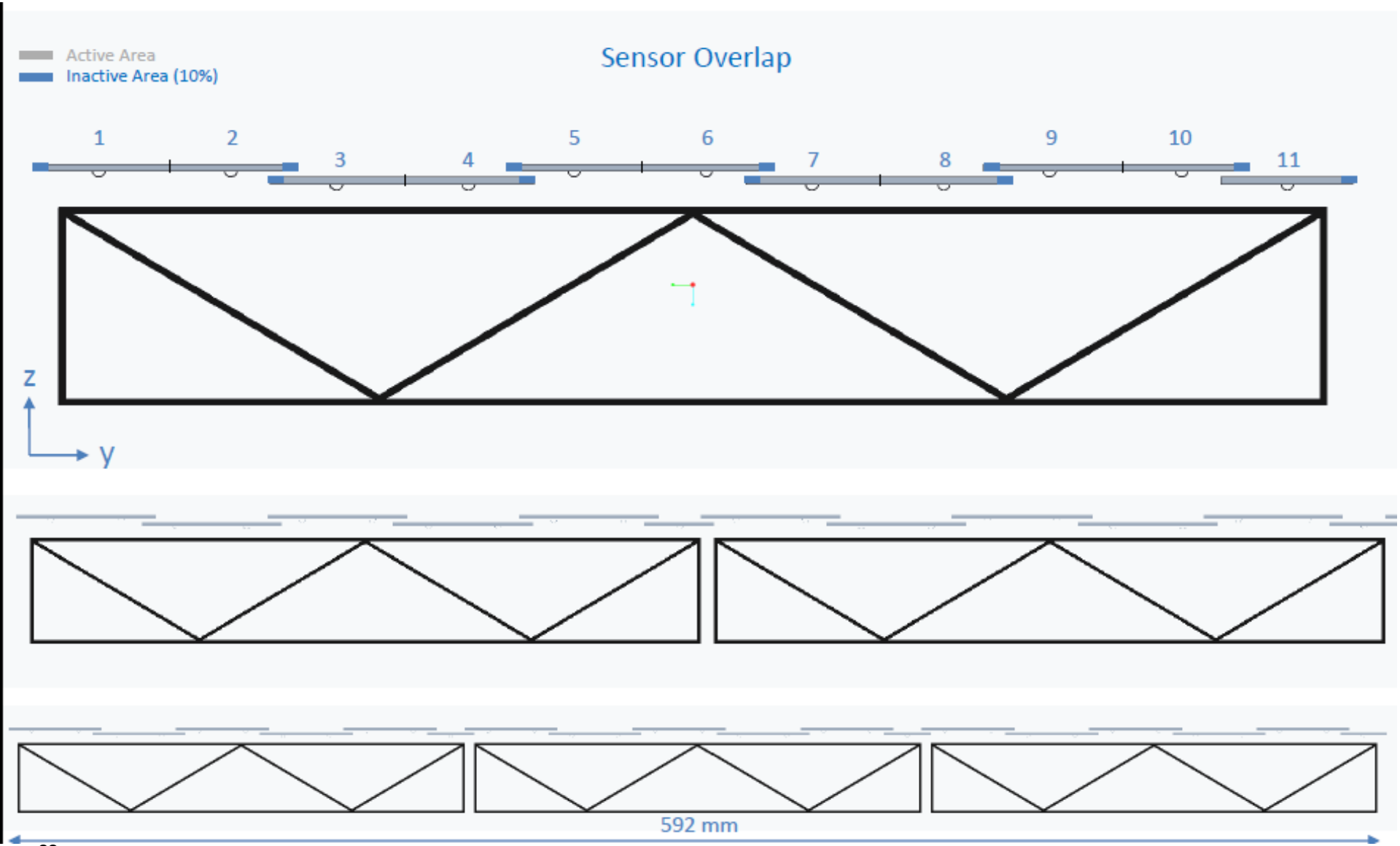
From A. Bitadze:
https://indico.cern.ch/event/913514/contributions/3842972/attachments/2029553/3396228/LHCb_MT_V0.4.pdf

- The lot



From A. Bitadze:
https://indico.cern.ch/event/913514/contributions/3842972/attachments/2029553/3396228/LHCb_MT_V0.4.pdf

- Double sided sensors and mechanical structure



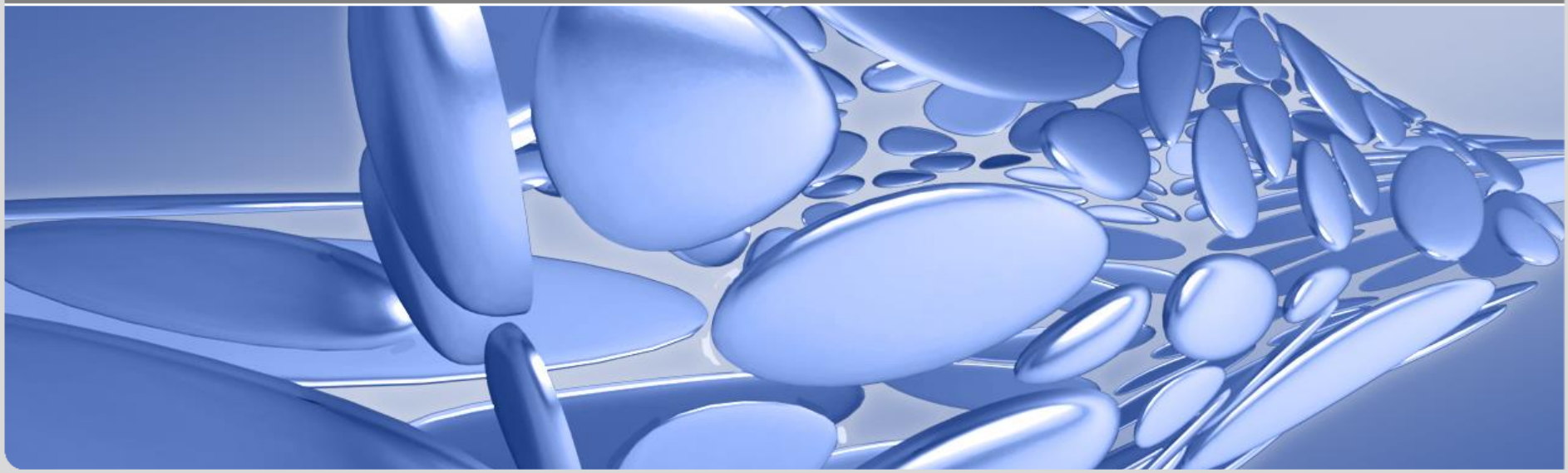
- To summarize:
- Six layers would be arranged as three double-sided layers with the sensors separated by a maximum of 40 mm
- The silicon module support consists of a CFRP faced carbon foam structure with integrated cooling pipes
- Full coverage can be achieved by overlapping the silicon sensors
- Kapton flex-circuit and can be attached to the silicon sensors by tab bonding
- This module will be mounted directly onto the Hybrid module structure. It will be encased by a CFRP box, utilizing the SciFi structure

Specification of the sensor chip for the Mighty Tracker

- Specification of the sensor chip for the Mighty Tracker
- Chip size ~ 2 cm x 2 cm
- Sensor thickness (µm) 200
- Pixel size (µm) 100 x 300 (with smaller sizes to be explored)
- Time resolution (ns) Must be within 25 ns window
- Inactive area < 5%
- Power consumption (W/cm^2) 0.15
- Data transmission (Gbps) 4 links of 1.28 Gb/s each, multiplexed to 2 and 1 links
- NIEL n_{eq}/cm^2 : 3 x 10^{14} (6 x 10^{14} with safety factor)

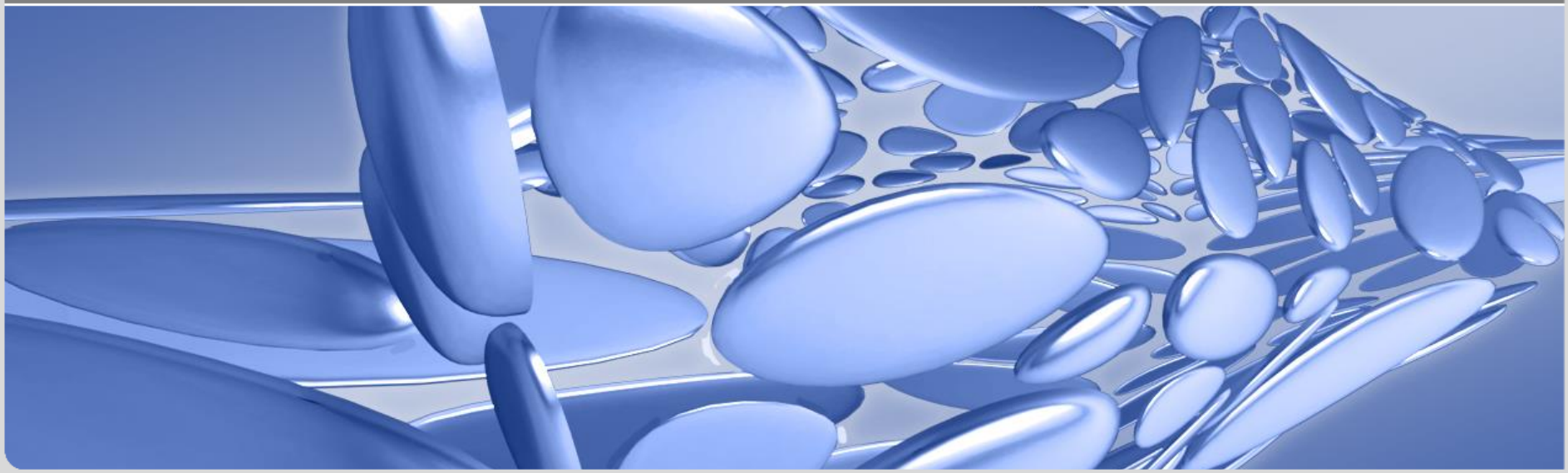
- Chip would have links with up to 2Gb/s and run these on kapton cables to the end of the inner tracker modules, a distance of up to 50cm
- At the end of the module a board can be used to transmit the signals on optical fibres and for voltage regulation
- The optical board would multiplex the signals so that 10Gb/s is sent on each optical fibre.
- The data would then be received on the PCIe40 boards for processing, before passing to the trigger. Clusterisation could occur in FPGAs or in software
- More ambitious possibility is performing doublet pattern recognition between the chips on the two-sides of the inner tracker modules
- Data rate rapidly falls off with distance from the beam. A significant cost and material driver will be the number of electronic channels needed, and the vast majority of the detector has a relatively low data rate. The option to multiplex these to provide both two and one output links per chip is recommended. If needed one could also consider daisy chaining chips.

Project timeline

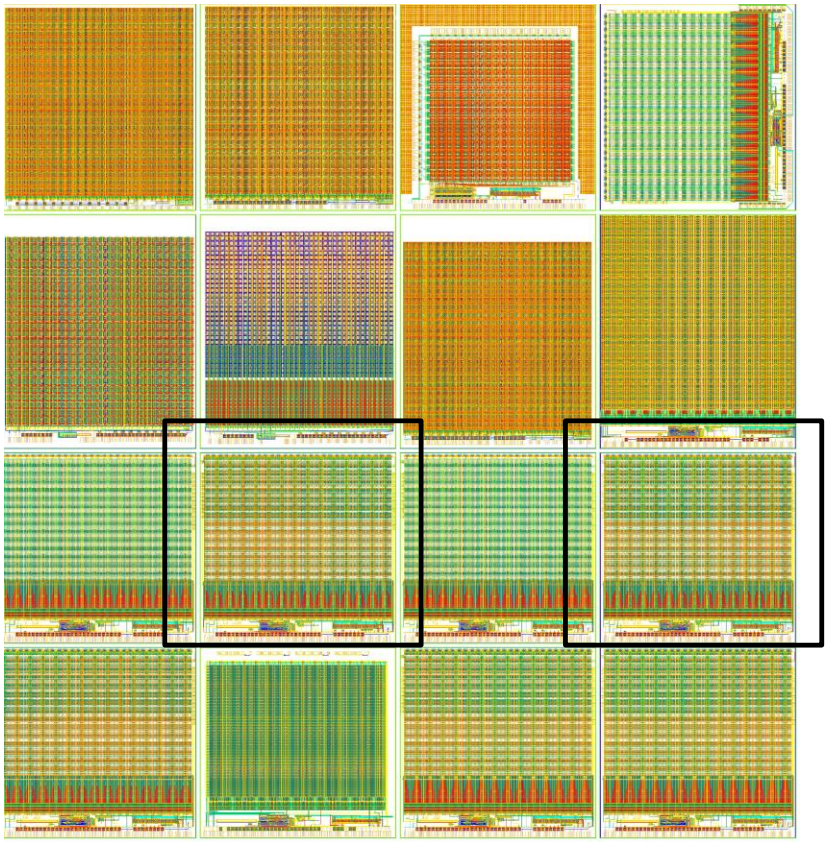


- From Mighty Pixel document:
- Project starts in Q1 2020 with the preparation of this specifications document and it ends in Q4 2023 with the production readiness of a full size detector.
- Q1 2020 Specifications document (done)
- Design work for MPW1 to prototype matrices with a few pixel sizes (done)
- Q2 2020 Submission of MPW1 (done)
- Q3 2020 Reception and evaluation of MPW1 (started)
- Design work for MPW2 to prototype a matrix with one pixel size and LHCb compatible readout electronics
- Q1 2021 Submission of MPW2
- Q2 2021 Reception and evaluation of MPW2
- Design work for ENG1 to demonstrate a full reticle size detector
- Q1 2022 Submission of ENG1
- Q2 2022 Reception and evaluation of ENG1
- Design work for ENG2 (production chip)
- Q3 2022 Evaluation of detector module based on ENG1
- Q1 2023 Submission of ENG2
- Q2 2023 Evaluation in full detector system of ENG2
- Q4 2023 Production readiness based on ENG2

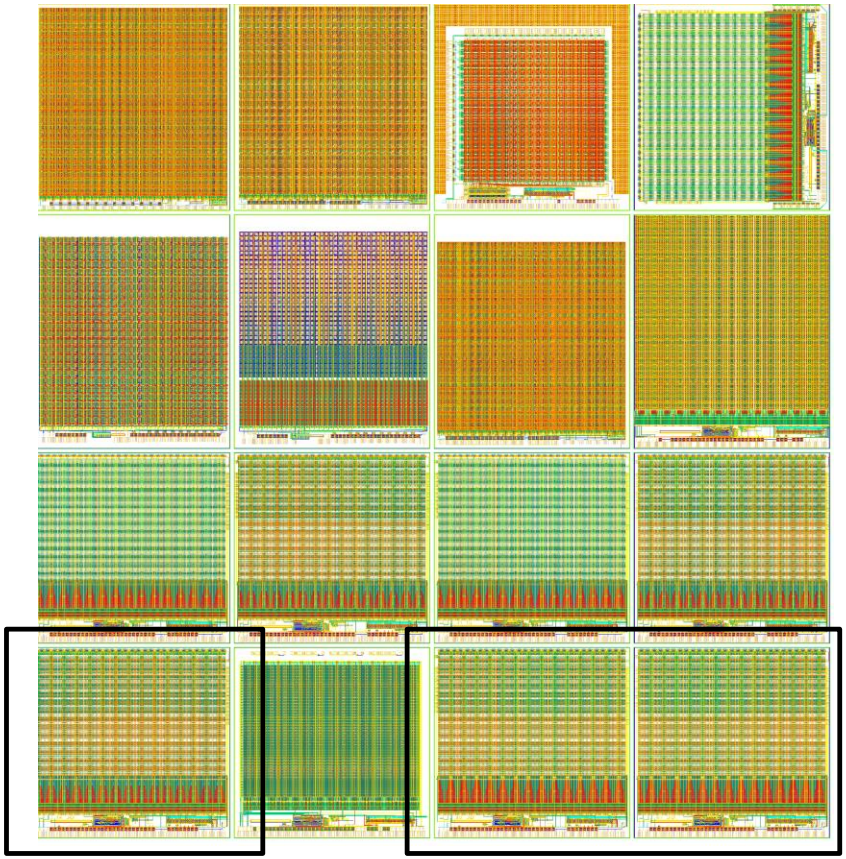
Our contribution until today



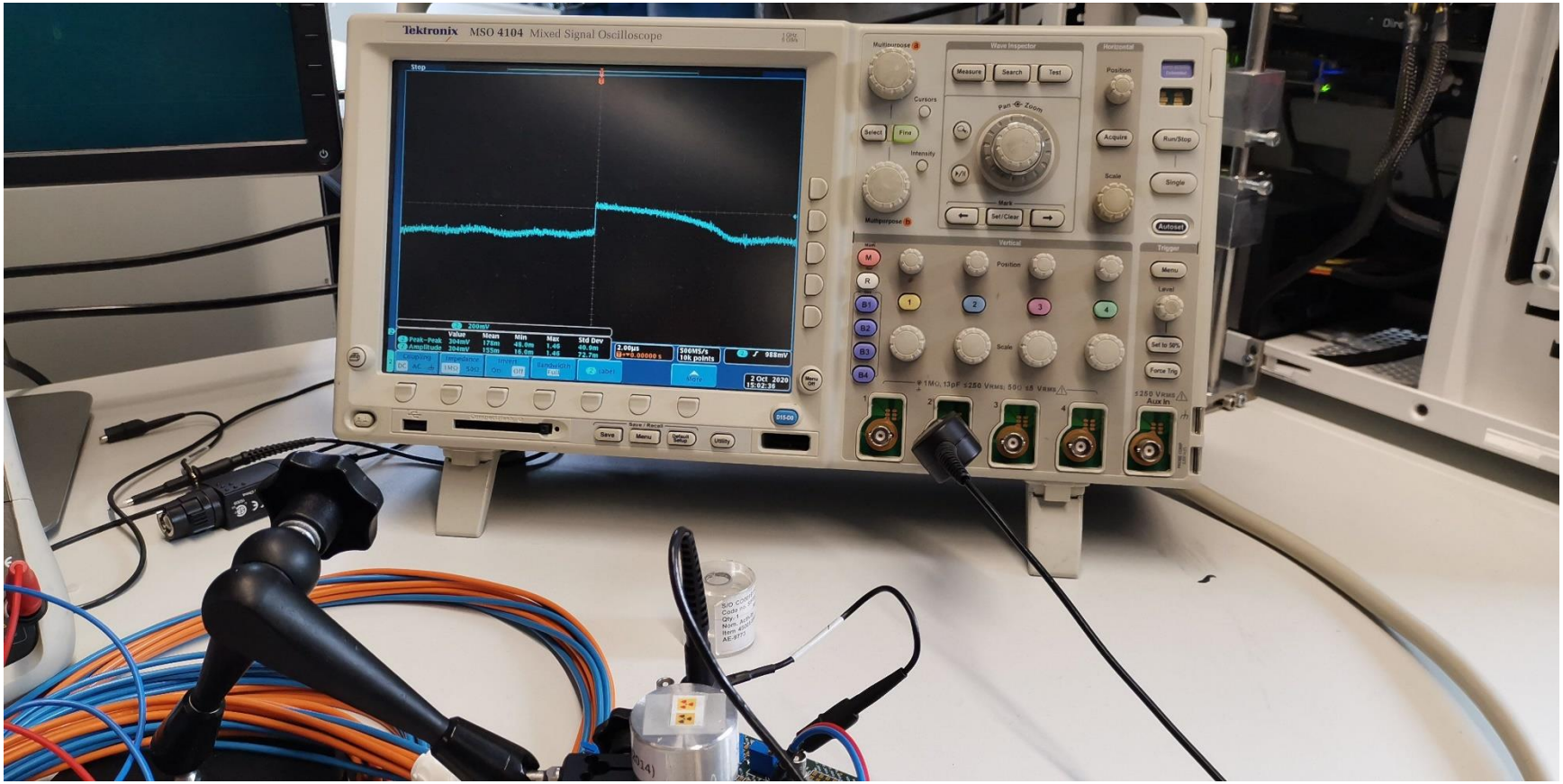
- Engineering run in TSI 180nm HVCMOS process with 16 designs, 5 of them for LHCb
- Submitted in April 2020
- Matrix1_cmos
  - Pixel size 25µm x 165µm
  - 124 x 29 pixels
  - CMOS and NMOS pixels
  - Option with TDAC in pixel or in periphery
  - NMOS comparator
- Matrix1_VarSize
  - Pixel size 1: 50µm x 165µm
  - Pixel size 2: 100µm x 165µm
  - PMOS pixels in different flavours
  - NMOS comparator, TDAC in periphery
- Matrix2
  - Pixel size 25µm x 165µm
  - 124 x 29 pixels
  - PMOS and NMOS pixels
  - Option with TDAC in pixel or in periphery
  - CMOS comparator
- Matrix2_VarSize
  - Pixel size 1: 50µm x 165µm
  - Pixel size 2: 100µm x 165µm
  - PMOS pixels in different flavours
  - CMOS comparator, TDAC in periphery



- Matrix2_hidr
  - Pixel size 1: 50µm x 165µm
  - Pixel size 2: 100µm x 165µm
  - PMOS pixels in different flavours
  - CMOS comparator, 2x in pixel, one slow for energy measurement one fast for time, TDAC in periphery
- Matrix3_VarSize
  - Pixel size 1: 50µm x 165µm
  - Pixel size 2: 100µm x 165µm
  - PMOS pixels in different flavours
  - Comparator in periphery
- Matrix3
  - Pixel size 25µm x 165µm
  - 124 x 29 pixels
  - NMOS pixels (low power)
  - Comparator in periphery
  - Daisy chain readout possible
- Matrix3_hidr
  - Pixel size 1: 50µm x 165µm
  - Pixel size 2: 100µm x 165µm
  - PMOS pixels in different flavours
  - Comparator in periphery, 2x per pixel, one slow for energy measurement one fast for time



- First signals from MPW1



Summary

- Our LHCb team:
- Richard Leys, Ivan Peric, Sigrid Scherl
- We plan to contribute on the sensor development for the upgrade and commissioning

- Thank you!