DEVELOPMENT OF THE CONFIGURATION, CALIBRATION AND MONITORING SYSTEM OF THE NEW SMALL WHEEL ELECTRONICS FOR THE ATLAS EXPERIMENT

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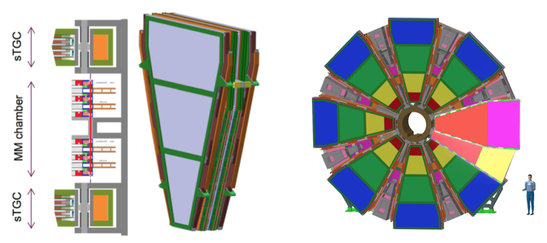
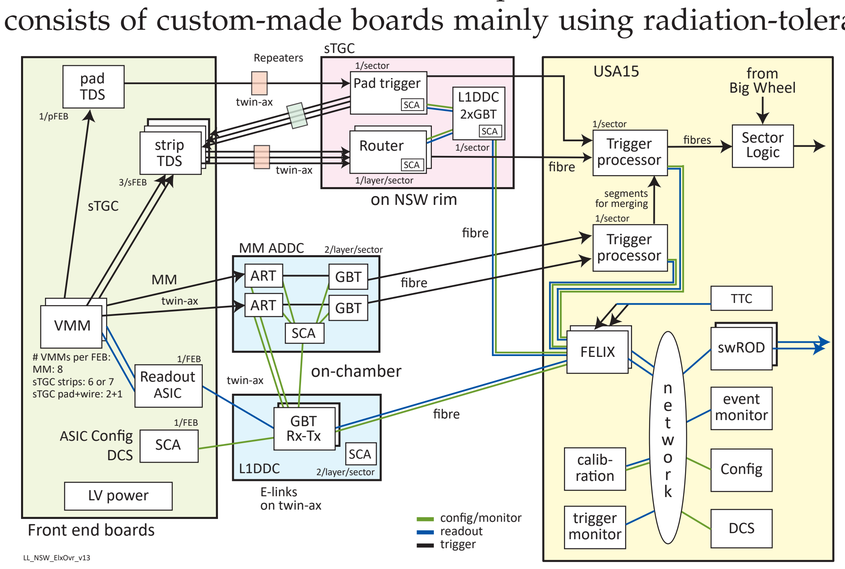
THE NEW SMALL WHEEL

The LHC accelerator will be upgraded to deliver an instantaneous luminosity up to $7.5 \times 10^{34} cm^{-2} s^{-1}$. The luminosity increase, drastically impacts the ATLAS trigger and readout data rates. The present ATLAS small wheel muon will be replaced with a New Small Wheel (NSW) which is expected to be installed in the ATLAS at the end of 2021. With the series-production of Micromegas (MM) and small-strip Thin Gap Chambers (sTGC) modules already produced the activities concerning the integration of the modules into the final fully equipped New Small Wheel sectors are currently in full swing at CERN.



ELECTRONICS OVERVIEW

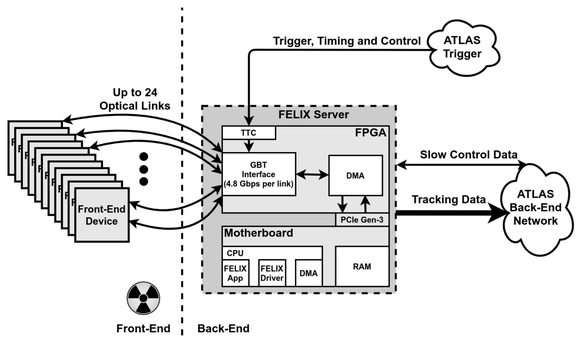
The NSW electronics for the trigger and Data Acquisition (DAQ) path of both detectors can be divided into two major categories, on-detector and off-detector electronics. The on-detector electronics Front-End boards, Level-1 Data Driver, ART Data Driver Card will be placed inside the cavern (detector area with radiation and magnetic fields) and consists of custom-made boards mainly using radiation-tolerant Application Specific Integrated Circuits (ASICs).

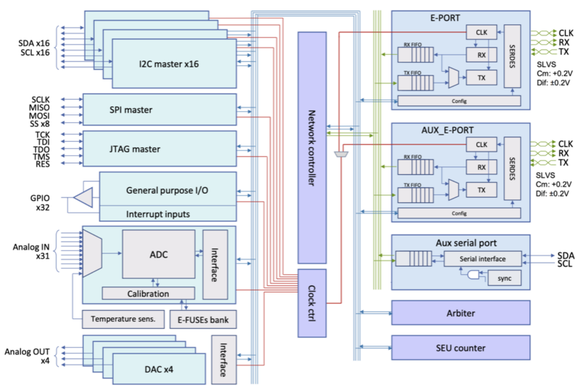


The communication between these boards will be established with the use of mini Serial Attached Small Computer System Interface cables. The off-detector electronics (Front End LInk eXchange (FELIX), trigger processor, sector logic and services running on commercial server computers like Read Out Drivers (ROD), Detector Control System (DCS), event monitoring, configuration, trigger monitor and calibration) will be placed outside the cavern in an area that is called USA15.

FELIX & GBT-SCA & SCA OPC UA SERVER

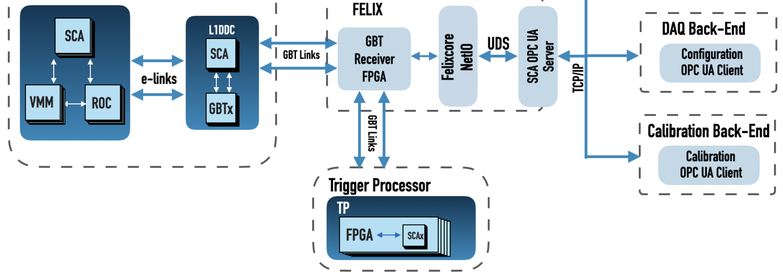
The keystone of the ATLAS DAQ system will be the Front-End Link eXchange or simply FELIX. FELIX will essentially be a bridge between the front-end electronics of all ATLAS detector subsystems, and their corresponding back-end components, which will mostly be software-based, whereas FELIX is an FPGA-based system housed by a commercial server. Situated in the USA15, FELIX connects to the front-end electronics of the ATLAS cavern via optical links, or GBT links, each one of which is running at 4.8 Gb/s. For the NSW case, FELIX will interface with the front-end nodes over 24 optical links. These links carry the GBT frame, which is 84-bit wide. The Giga-Bit Transceiver (GBT) protocol is a transmission scheme that involves radiation-tolerant ASICs, capable of handling the large amounts of data of high energy physics experiments.





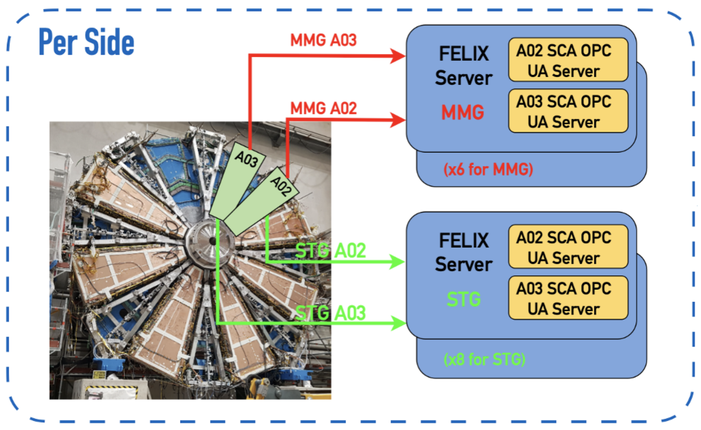
In this SCA-GBTx-FELIX communication chain, the last two components can be viewed as data mediators, so there is one piece missing: the back end logic that actually builds the packets-to-be-transmitted to the SCA, and handles the inbound traffic from the ASIC. This is a software suite, which is a dedicated Open Communications Platform Unified Automation (OPC UA) server.

The GBT-SCA ASIC (Giga-Bit Transceiver-Slow Control Adapter) is part of the GBT chipset and is usually connected both to a GBTx and to several front-end devices. It's purpose is to distribute control signals to the on-detector front-end electronics and perform monitoring operations of detector environmental parameters. In order to meet the requirements of different front-end ASICs used in high-energy physics experiments, it provides various user-configurable interfaces, such as SPI, I2C or JTAG, and is capable of performing simultaneous operations.



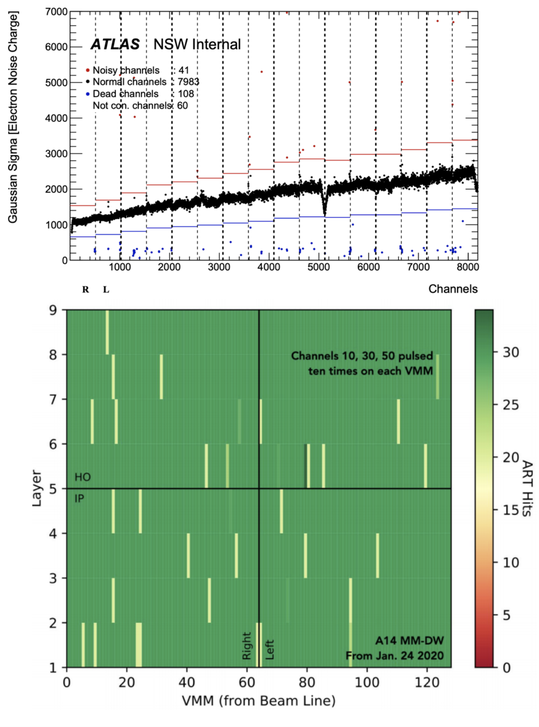
CONFIGURATION

The NSW is a fully autonomous trigger and tracking detector system, adequately supported by an advanced electronics scheme and ready to handle the challenges of increased instantaneous luminosity at the High Luminosity LHC. It includes more than 60k front-end ASICs and a few tens of FPGAs, which need to be configured before every run of the experiment. This process needs to be efficient and quick, since it needs to happen a few times per day. The main ASIC to be configured is the VMM, the front-end signal pre-processing chip which can read-out 64 channels. A few kbytes of configuration data include thresholds for each channel, but also global registers to define the gain, time-to-amplitude conversion and many others. For this procedure we need to use the SCA's SPI master to communicate with the 8 SCA's SPI slaves in the VMMs. Also the SCA's GPIO interface is required, to act as an enable signal. Moreover, a similar scheme using the SCA's I2C interface is used for configuration of the TDS chip, which is used for timing and trigger.



CALIBRATION

The calibration procedure consists of various timing and charge calibrations of the front-end electronics. Gain calibration is done by varying the signal input using the internal pulser of the chip. A specific configuration file needs to be loaded on the VMM chips, which is done with the SCA. Calibration of a time-to-amplitude converter is done by skewing the input clock, which is performed by re-configuring the specific on-board with different settings. Baseline and noise level is defined by reading out each channel output with the ADC when no collisions are happening.



MONITORING

Due to its complexity and long-term operation, the ATLAS detector requires the development of an advanced DCS for the electronics monitoring using the SCA chip which is already installed on the 8000 front-end boards of the NSW. The use of such a system is necessary for the safe operation of the detector as well as to act as a homogeneous interface to all the sub-detectors and the technical infrastructure of the experiment. This system gives us the ability to monitor all the power/temperature sensors, on-chip temperature and information which are connected to the SCA on all the fron-tend boards of the NSW.