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Development of the Configuration, Calibration and Monitoring System of the New Small Wheel Electronics for the ATLAS experiment

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A series of upgrades are planned for the LHC accelerator to increase its instantaneous luminosity to $7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. The luminosity increase drastically impacts the ATLAS trigger and readout data rates. The present ATLAS Small Wheel Muon detector will be replaced with a New Small Wheel (NSW) detector which is expected to be installed in the ATLAS underground cavern by the end of the Long Shutdown 2 of the LHC. One crucial part of the integration procedure concerns the installation, testing and validation of the on-detector electronics and readout chain for a very large system with a more than 2.1 M electronic channels in total. These include 7K Front-End Boards (MMFE8, SFEB, PFEB), custom printed circuit boards each one housing eight 64-channel VMM Application Specific Integrated Circuits (ASICs) that interface with the ATLAS Trigger and Data Acquisition (TDAQ) system through 1K data-driver cards. The readout chain is based on optical link technology (GigaBit Transceiver links) connecting the backend to the front-end electronics via the Front-End Lnk eXchange (FELIX), is a newly developed system that will serve as the next generation readout driver for ATLAS. For the configuration, calibration and monitoring path, the various electronics boards are supplied with the GBT-SCA ASIC (Giga-Bit Transceiver-Slow Control Adapter) which is part of the Gigabit Transceiver Link (GBT) chipset and its purpose is to distribute control and monitoring signals to the electronics embedded in the detectors and in the ATLAS service areas. Experience and performance results from the first large-scale electronics integration tests performed at CERN on final NSW sectors will be presented.

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