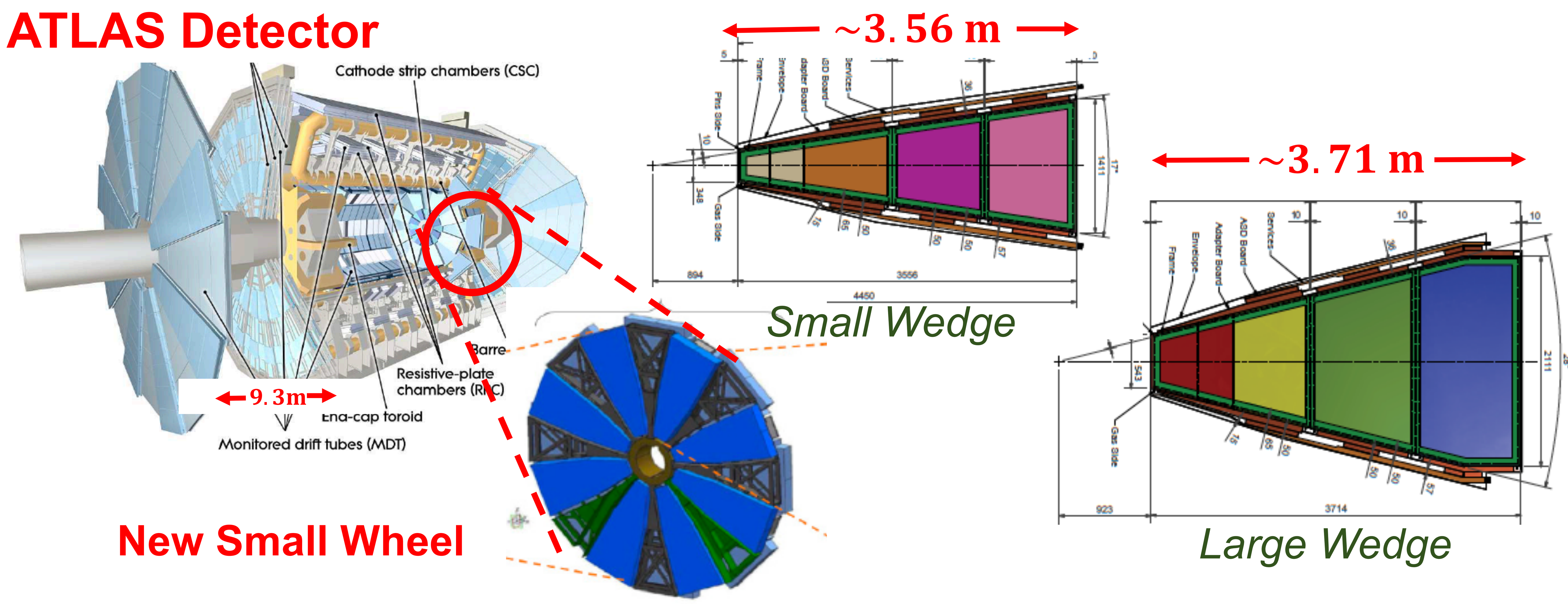
Integration and Commissioning of the Front-End Electronics of NSW ATLAS small-strip Thin Gap Chambers

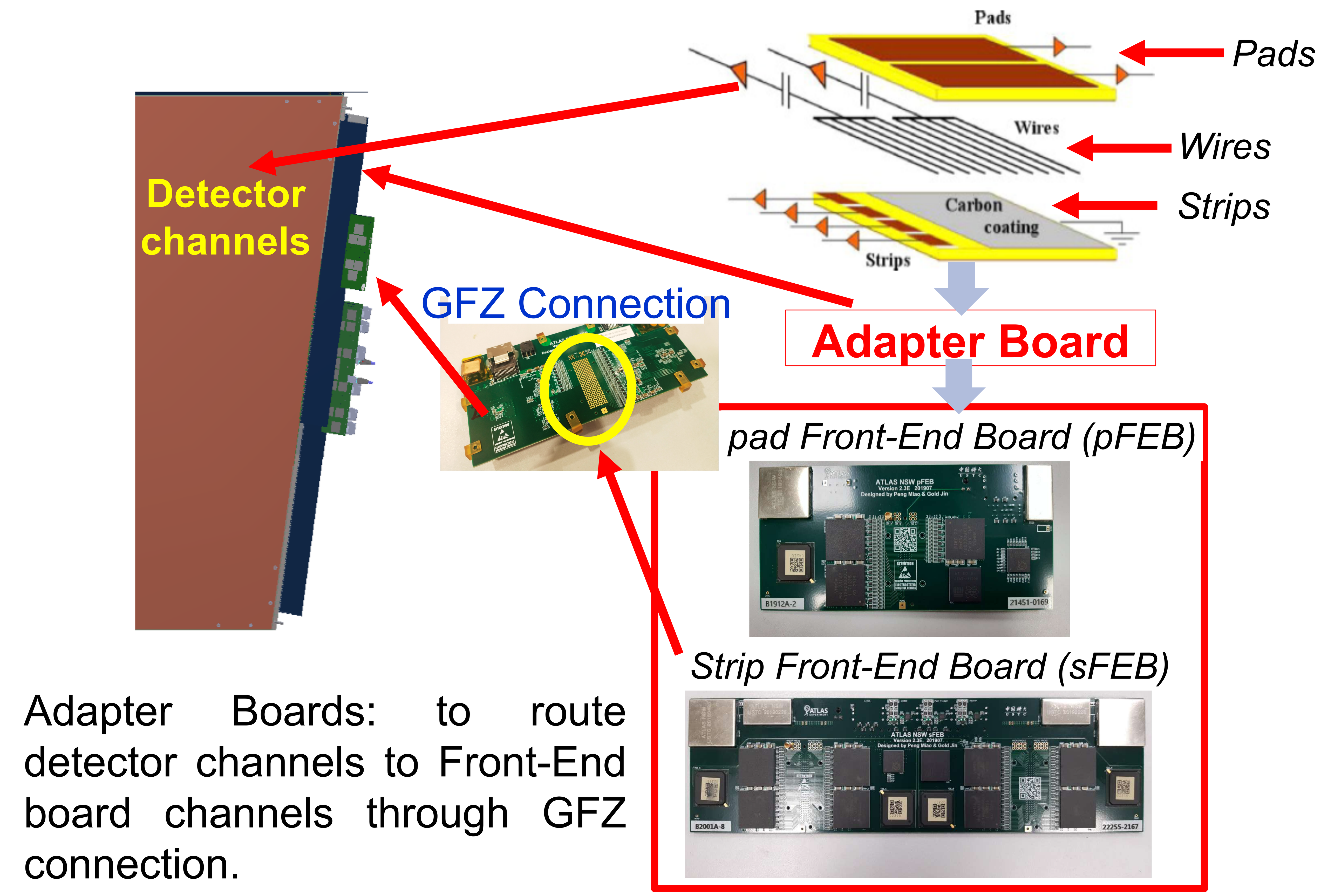
Prachi Arvind Atmasiddha, University of Michigan, Ann Arbor, USA
(On Behalf Of The ATLAS Muon Collaboration)

INTRODUCTION

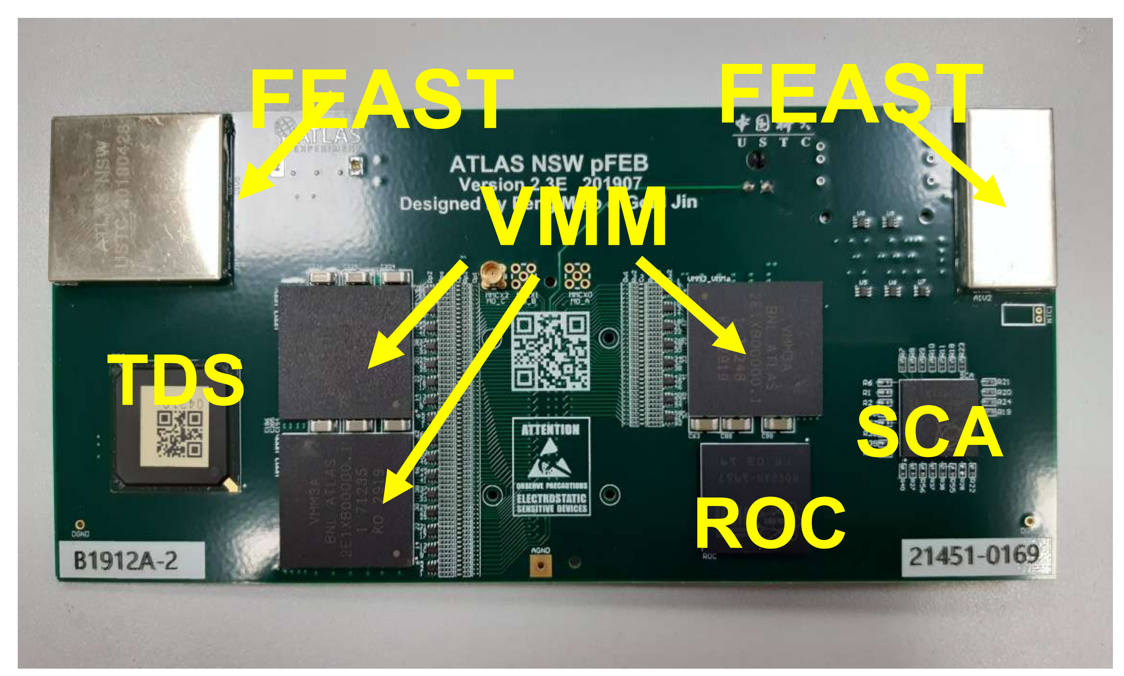


The Large Hadron Collider (LHC) will reach an instantaneous luminosity of $5-7.5\times10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$ (~2027 onward)[1]. This necessitates the upgrade of the ATLAS Muon Spectrometer. The innermost station of the muon end-cap system, the Small Wheel, will be replaced by the New Small Wheel (NSW). The NSW is required to improve the trigger selectivity in a high background environment (up to $20\ kHz\ cm^{-2}$). The small-strip Thin Gap Chambers (sTGC) sub-system will be the primary trigger detector for the NSW. The sTGC is expected to provide hardware-based online track segment measurements with a pointing accuracy of 1 mrad for the muon Level-1 trigger at the end-cap. The sTGC detector system is equipped with several types of radiation tolerant ASICs, electronics cards and FPGA based Back-End processors. Each sTGC wedge has 3 multilayered modules (quadruplets). Total 64 such wedges need to be commissioned. We present the status and the results from the Front-End electronics integration and commissioning of the sTGC sub-system at CERN.

FUNCTIONING OF THE FRONT-END ELECTRONICS



Adapter Boards: to route detector channels to Front-End board channels through GFZ connection.



FEAST – DC-DC converter powering the Front-End electronics.
VMM – primary readout ASIC.
TDS –Trigger Data Serializer
ROC – Readout Controller
SCA – For Slow Control

- Power consumption by one wedge: 372 W (pFEB: ~9W, sFEB: ~18 to 21W depending on the no. of VMMs.)
- Total number of Physical channels per wheel: ~178K (~5K/wedge)
- Total number of electronics channels per wheel: ~237K (~7.4K/wedge)

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STGC INTEGRATION AND COMMISSIONING

Preparatory Tasks

- Front-Ends Reception
- Data cables' bundling
- Manufacturing of the cooling pipes and plates.
- Etc

Mechanical Integration

Installation of low voltage distribution system, Front-Ends, Cables, Cooling, etc

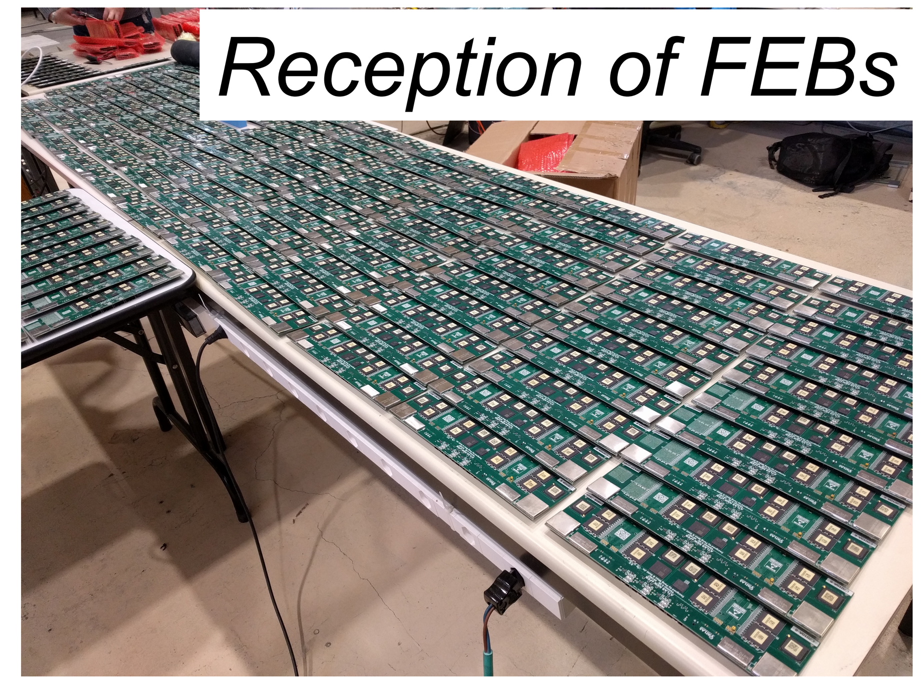
Electronics tests and validation of trigger and readout links

CHALLENGES

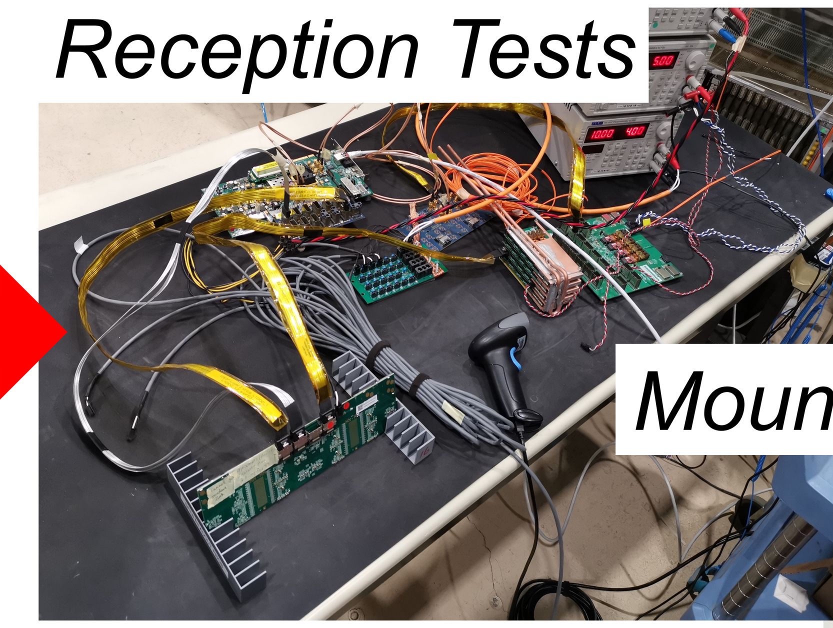
- Arrange active cooling system, data cables, Front-Ends and other electronics in a very tight space on the detector.
- Ground optimization and noise control for the large area detectors with high capacitance.
- Validation of the Front-End connectivity with complex readout & trigger data flow at high speed operated synchronously.

FRONT-ENDS AND SERVICE INSTALLATION

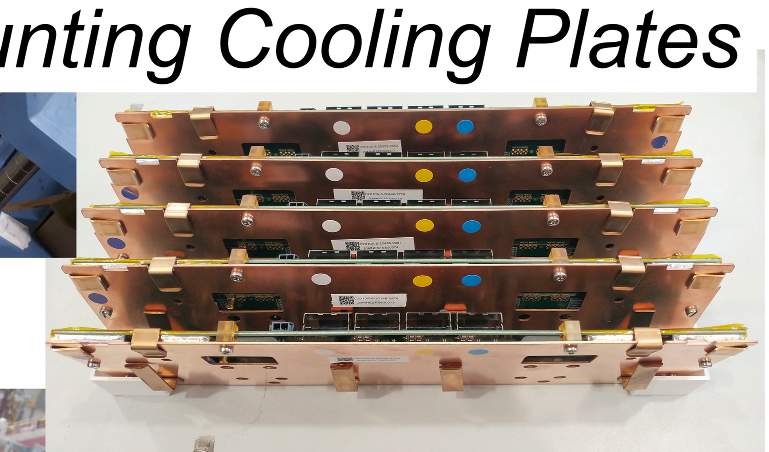
Reception Tests of the Front-End Boards:



Reception of FEBs



Reception Tests



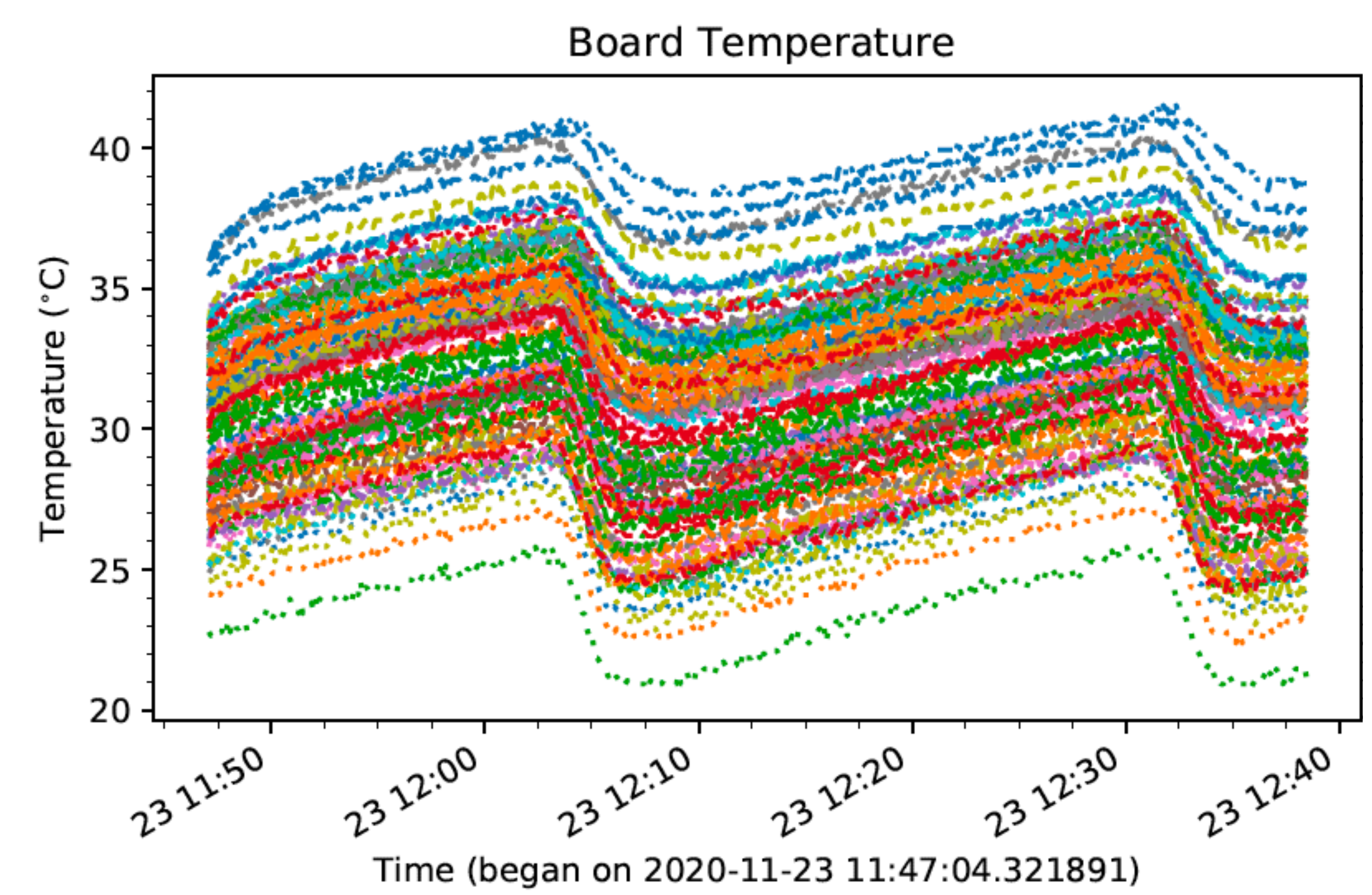
Mounting Cooling Plates

After installation of all the services on the sTGC wedge

Fitting all the services in a tight space (cooling system. Data cables, Front-Ends, LV power cables, etc)

The temperature of all the VMMs is monitored using the built-in temperature sensors inside the VMM.

Temperature should be < 50^0 C.



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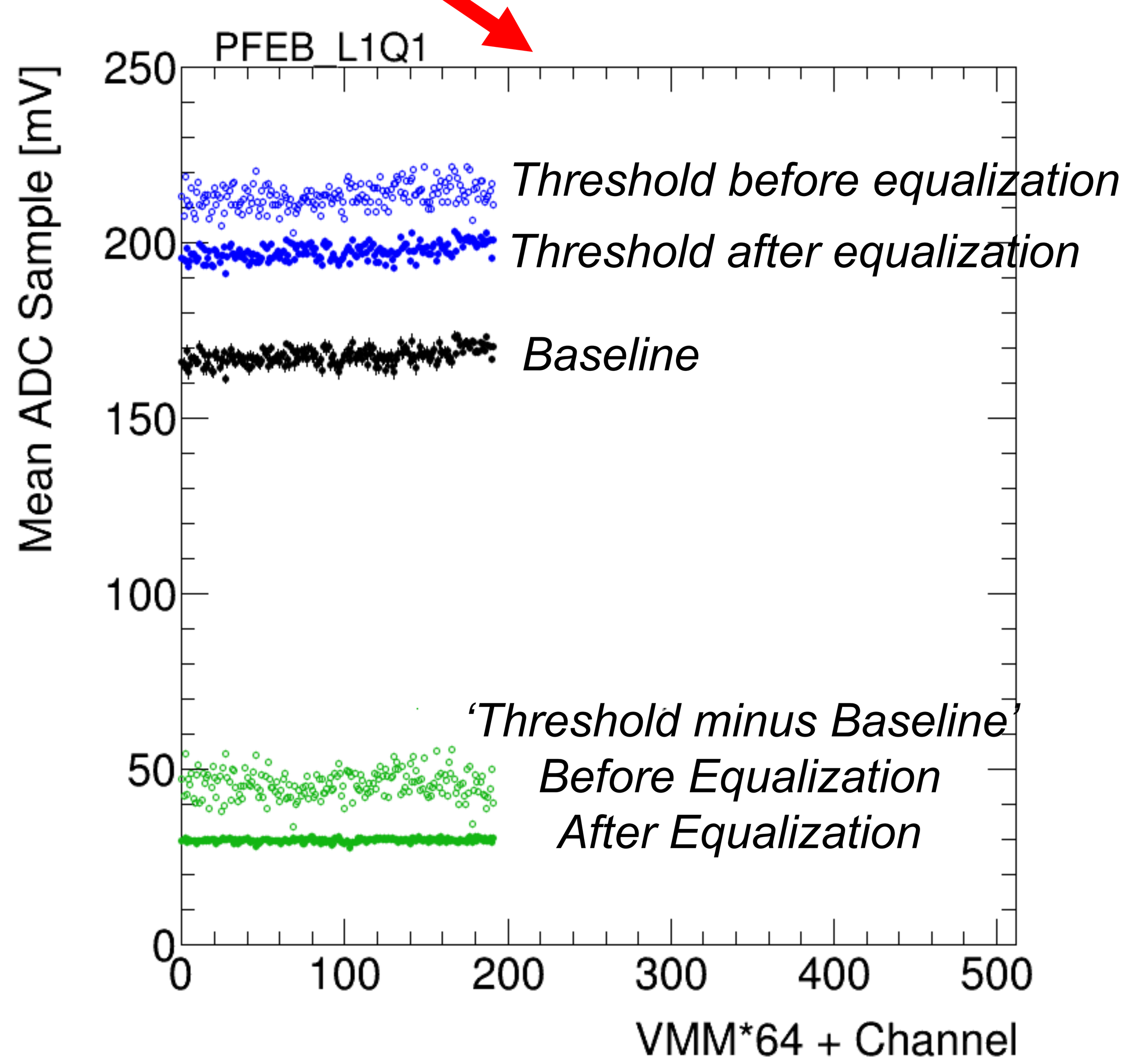
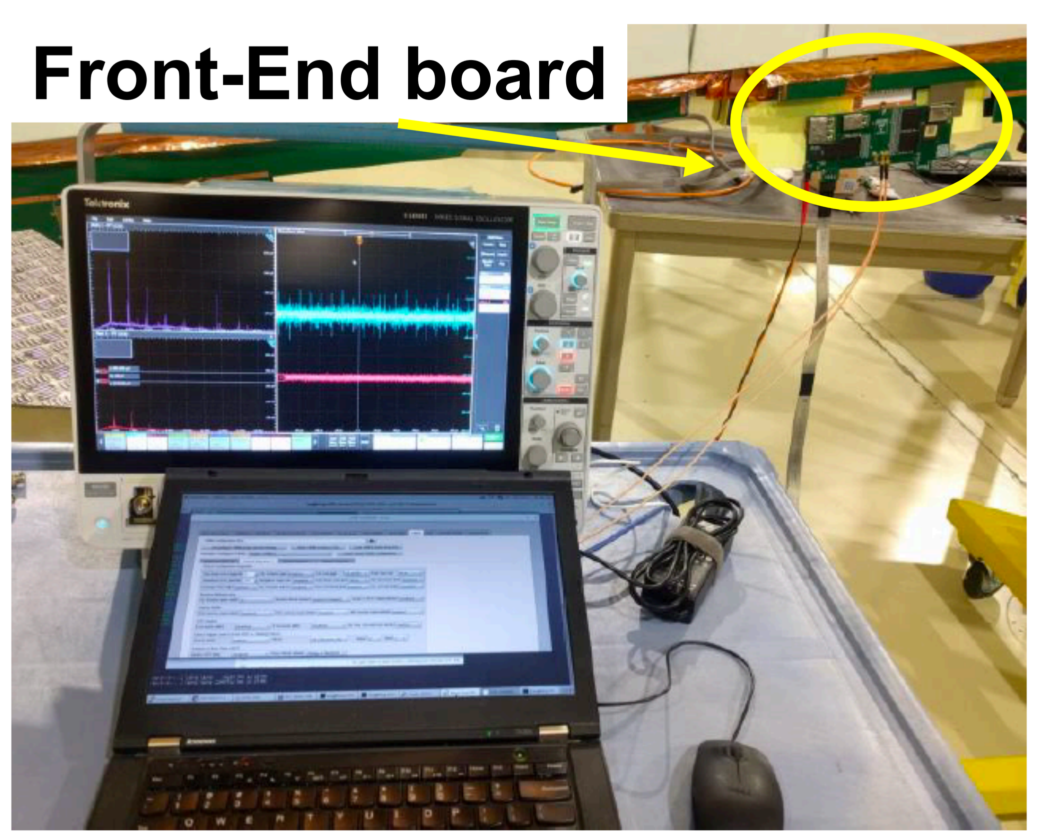
ON-WEDGE ELECTRONICS TESTS

Baseline, Noise and Connectivity Measurement:

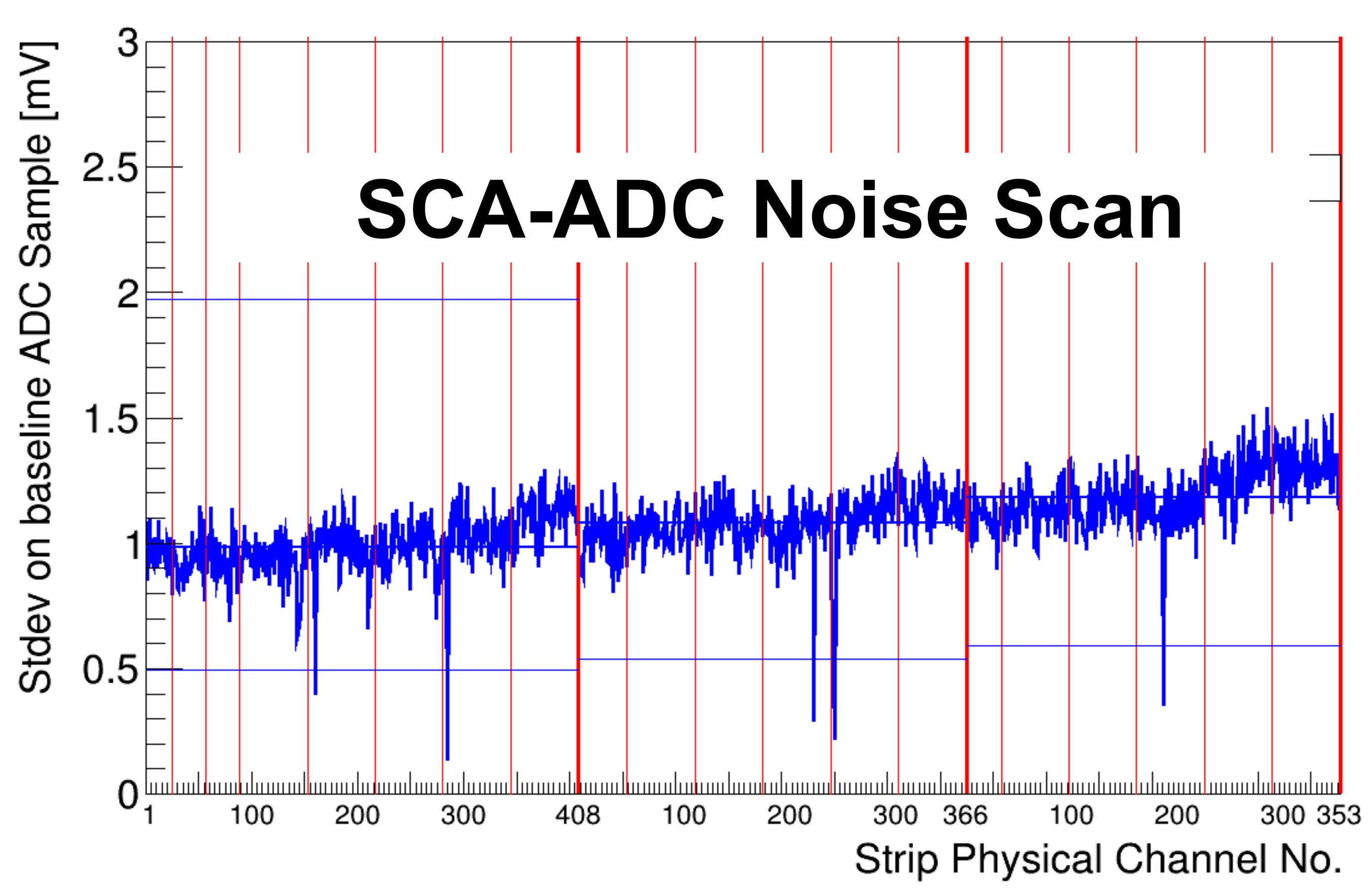
- Baseline and threshold equalization scans.
- Noise measurement is to:
  - Verify the connectivity between physical and electronics channels.
  - Validate the robustness of the system against any kind of noise propagated through conductive or radiative paths.
- Detailed studies have been performed to mitigate the sources of high noise by changing the grounding schemes or by eliminating the source if possible.



- Noise is measured using an oscilloscope and Analog-To-Digital Converter on the Front-Ends (SCA-ADC).

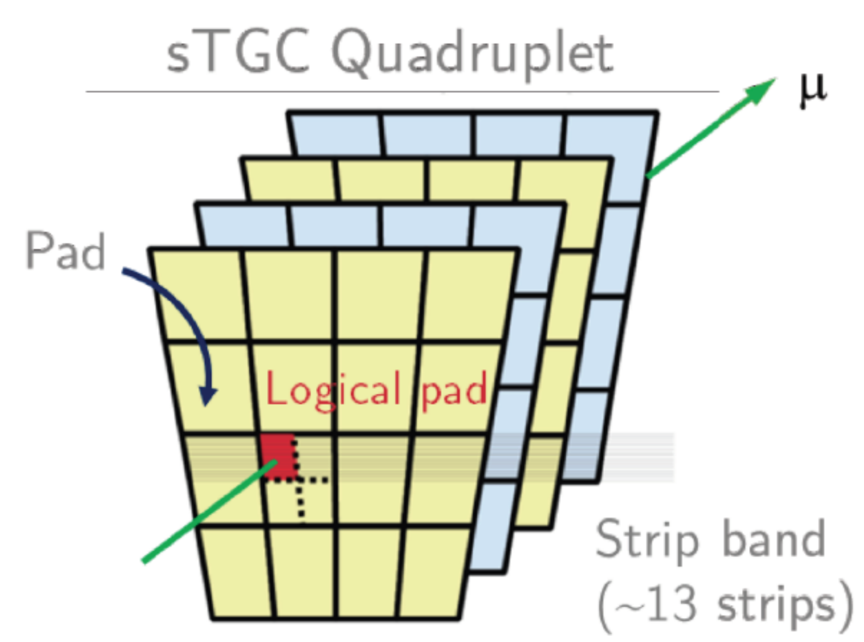


Noise measurement with oscilloscope

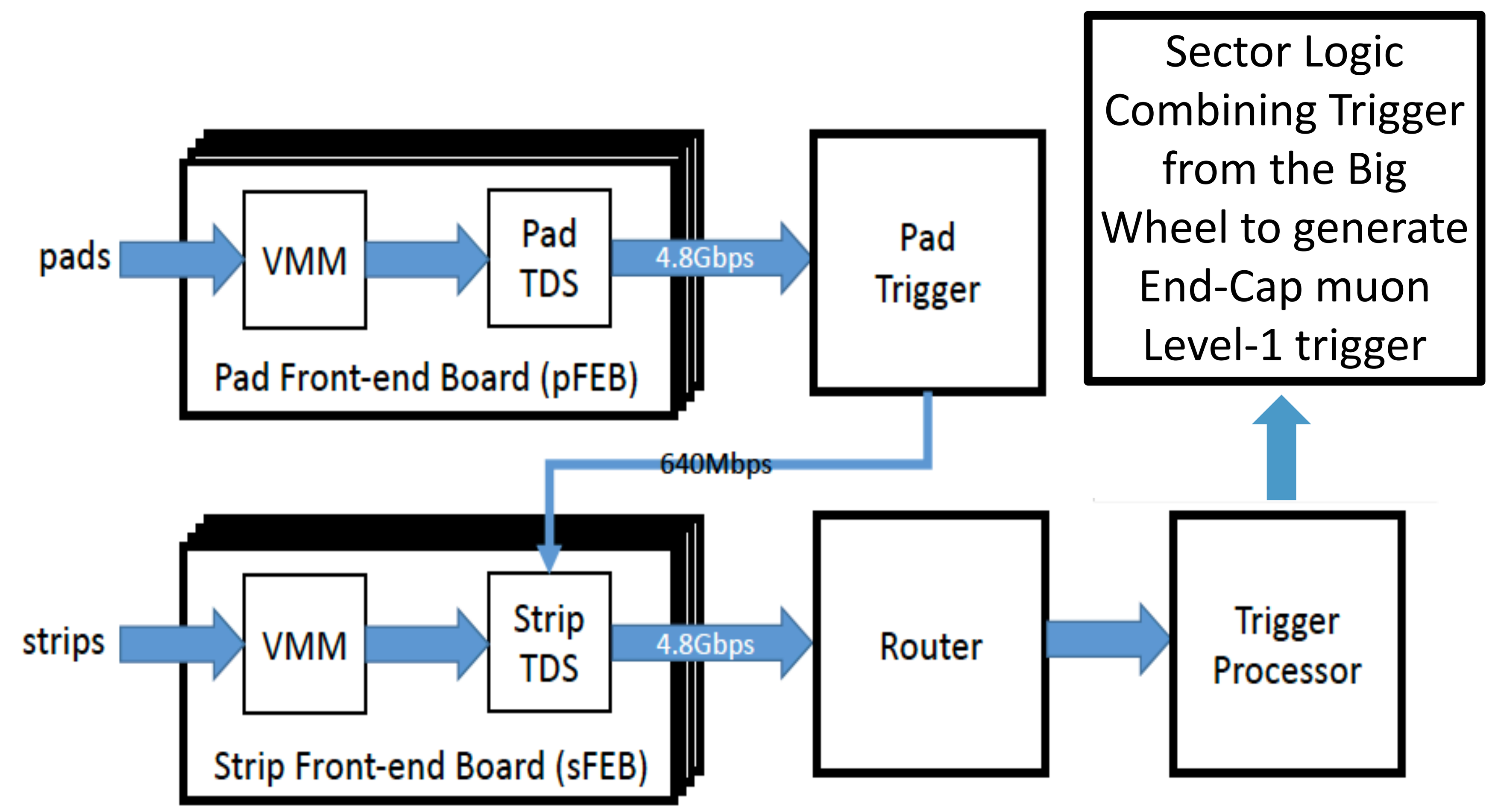


Noise ∝ Strip Length ∝ Capacitance

Trigger Chain Flow:

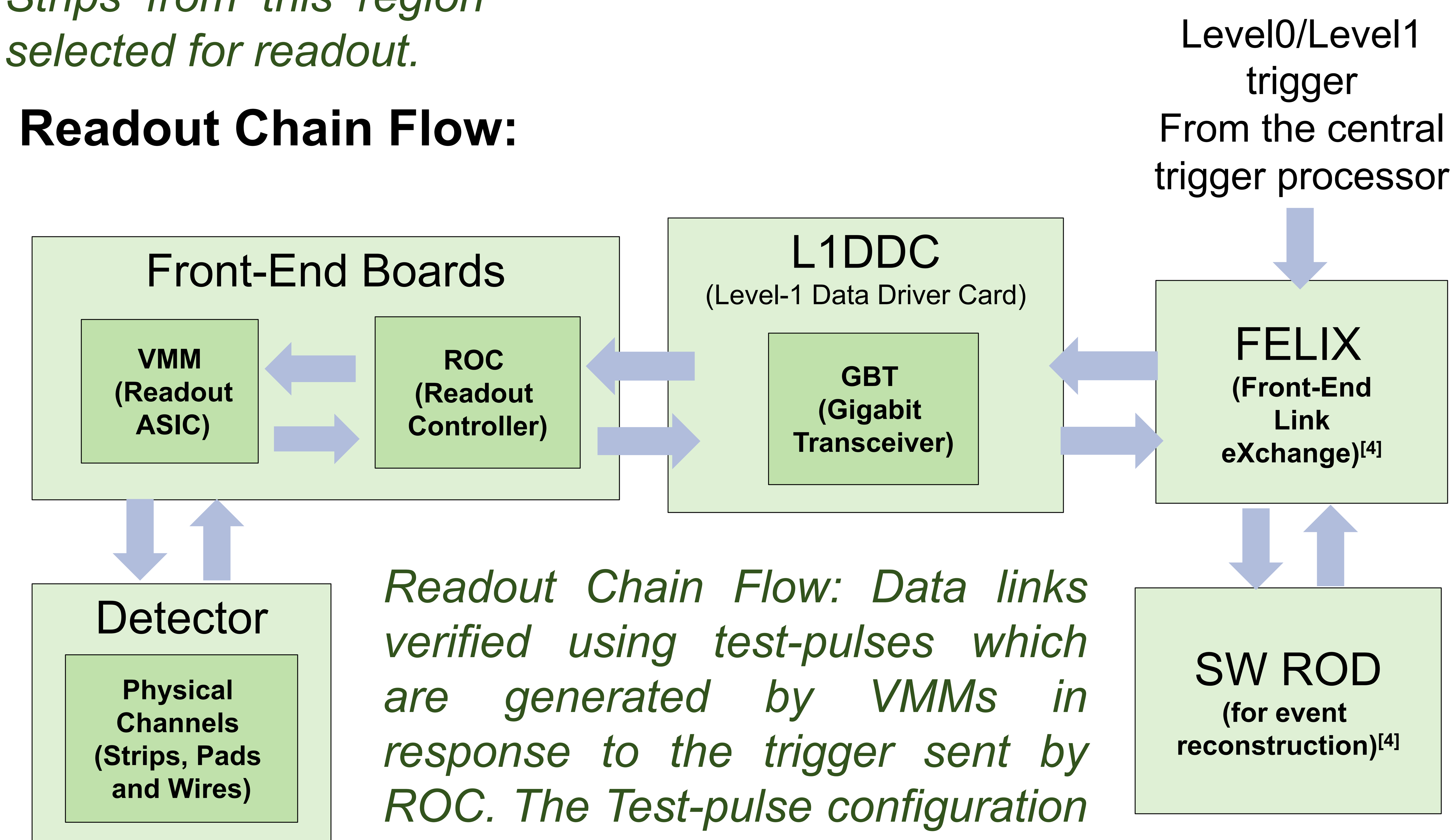


Region of interest determined using overlapping pads. Strips from this region selected for readout.



Trigger Chain Flow: Emulated trigger used to check all the data links.

Readout Chain Flow:



Readout Chain Flow: Data links verified using test-pulses which are generated by VMMs in response to the trigger sent by ROC. The Test-pulse configuration and Timing Trigger and Control is sent using FELIX via L1DDC.

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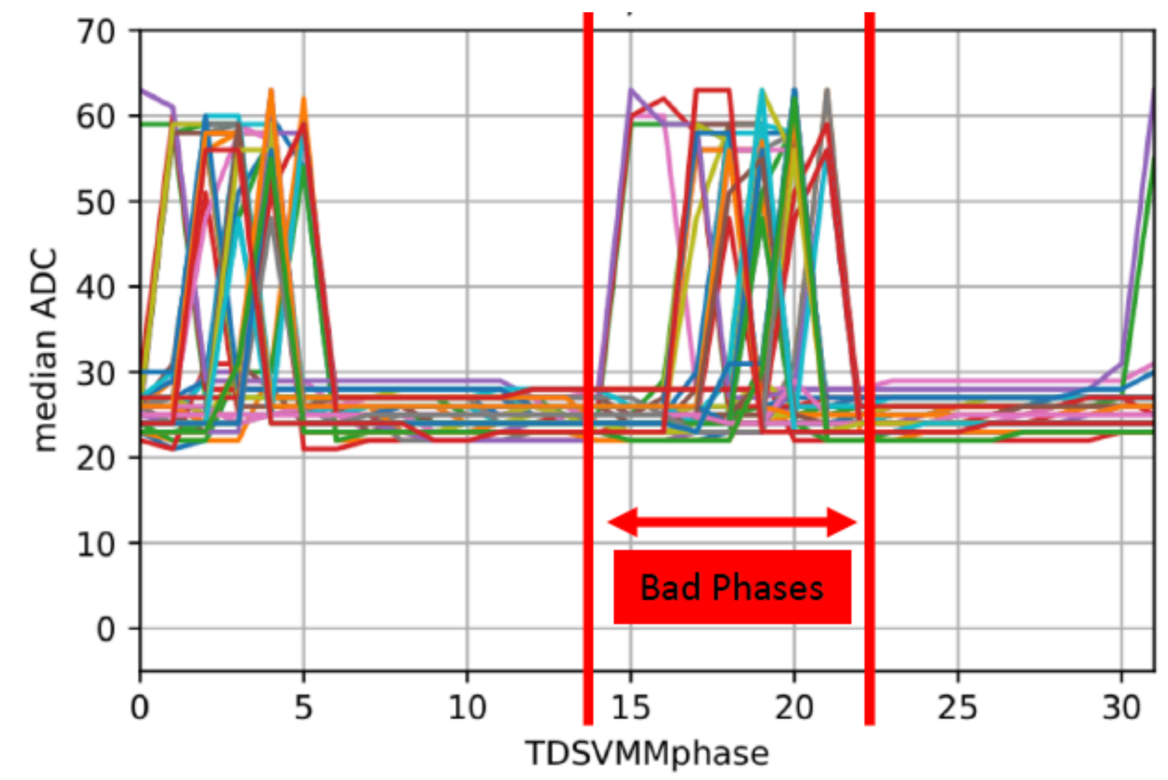
ON-WEDGE ELECTRONICS TESTS

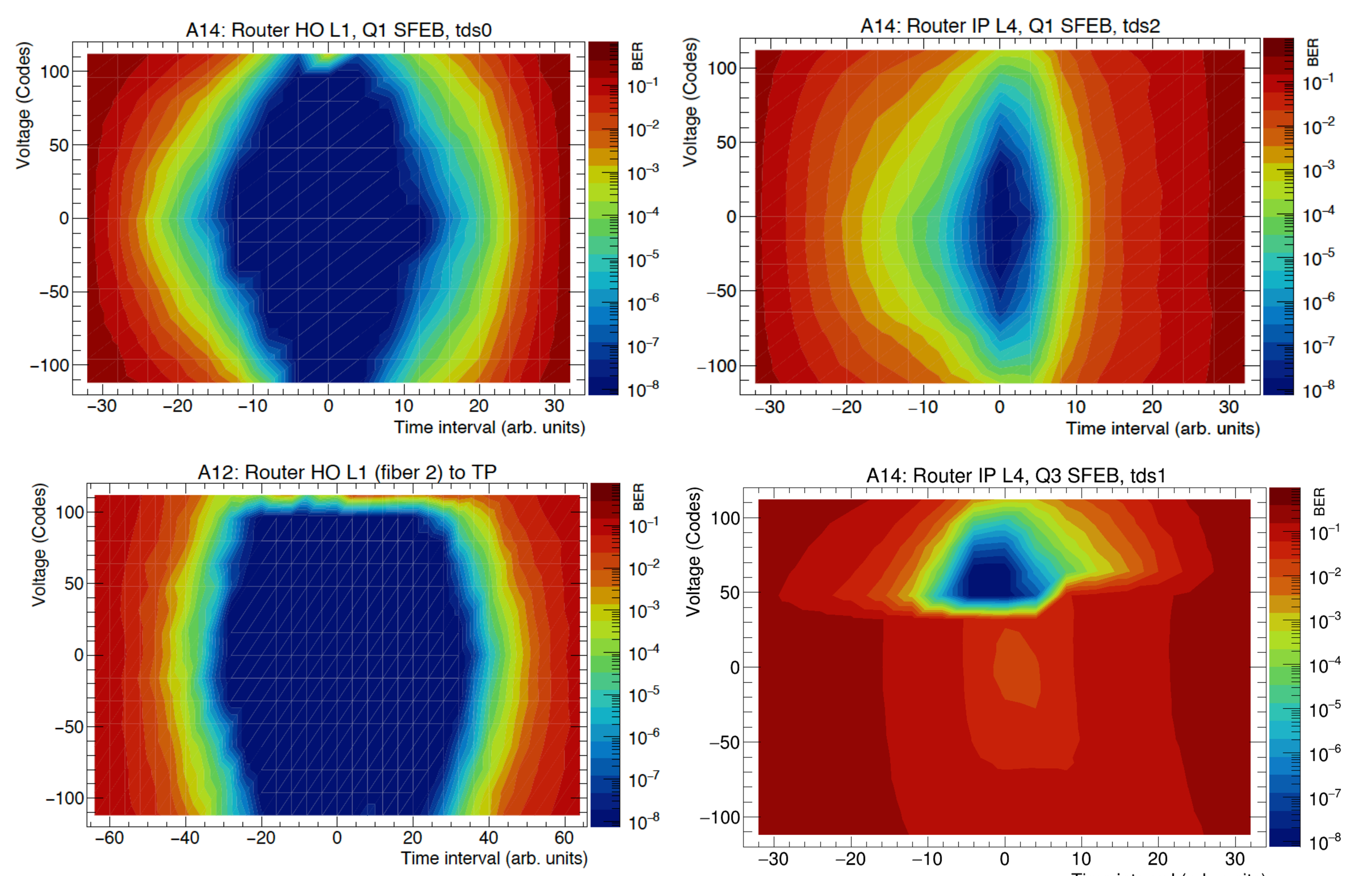
Data Quality Checks and synchronization:

- **The clock-phases** of VMM-TDS and ROC-TDS data links are tuned for synchronous trigger.
- **Readout parameters** which have to be tuned include: Bunch Crossing Offset, Time Trigger and Control (TTC) Phase, Clock phase for VMM to ROC data link, etc.
- **Eye-diagrams** – for checking the quality of the signal transmission, etc
- All separate data bits are superimposed together and the opening of the eye (*area in voltage-time space, where the measurement of the Bit Error Ratio (BER) is lower than a maximum acceptable value which is generally set to ~10^{-8} to 10^{-14}*) is measured.



VMM-TDS Phase

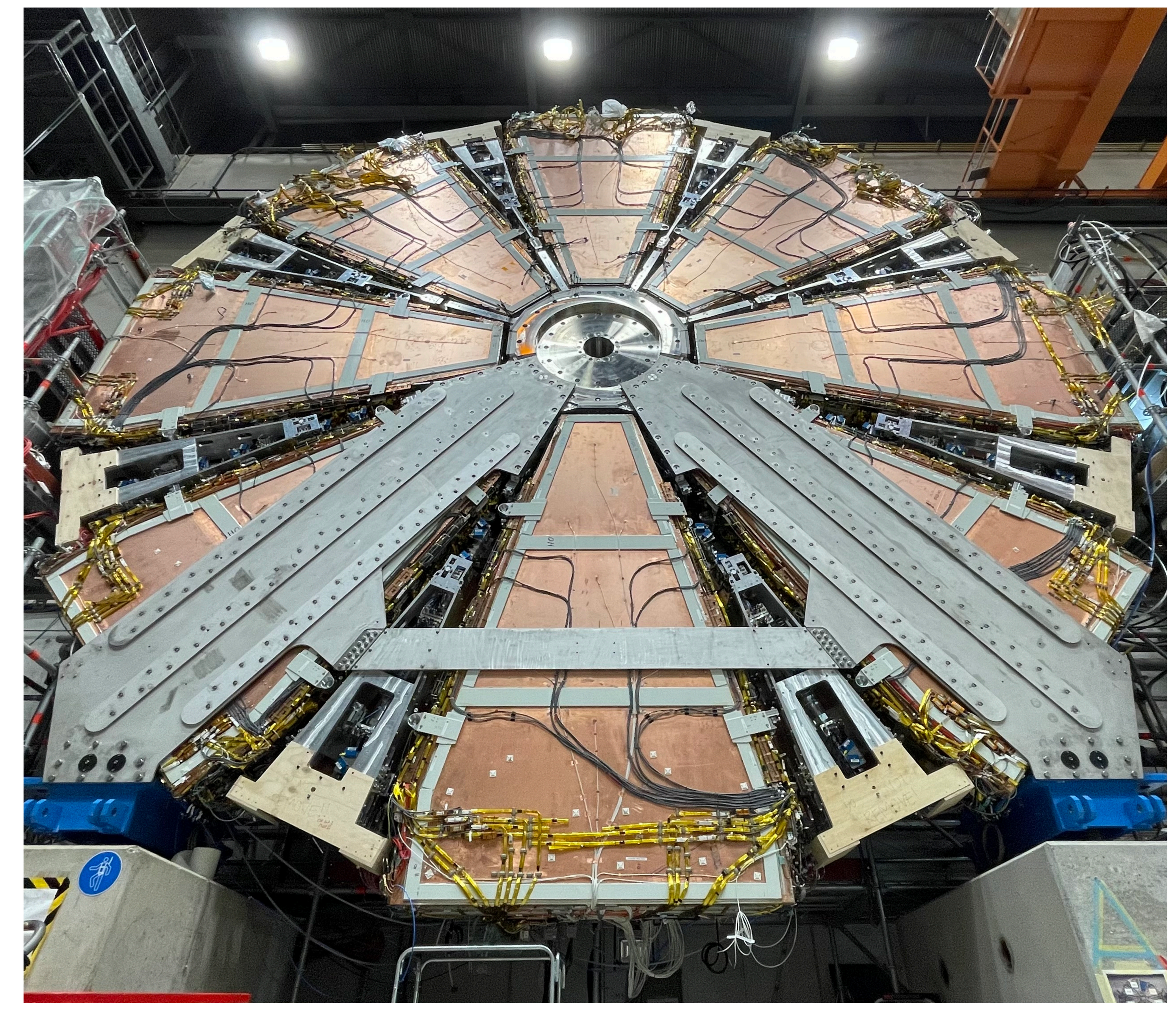
Good Eyes **Bad Eyes**



Eye-diagrams: for the signal transmission at 4.8 Gbps (Y-axis: voltage, X-axis: time) Smaller opening could be because of more time jitter, signal attenuation, etc.

CONCLUSION

For a typical sTGC Wedge	Problems
Strips	~ < 2%
Pads	~ <1%



NSW Side-A

- The Integration and Commissioning for sTGC detectors is ongoing at CERN for the installation during the LHC Long Shutdown 2 (LS2) period.
- Successful mounting and checking of the Front-Ends with trigger and data link tests are being done.
- The fully tested sTGC wedges are being mounted on the New Small Wheel along with the Micromegas detector wedges. All NSW Side-A Wedges have been mounted.

REFERENCES

[1] https://project-hl-lhc-industry.web.cern.ch/content/project-schedule **[2]** Kawamoto, T; ATLAS Collaboration (ATLAS-TDR-020). **[3]** P. Gkountoumis, JINST12, no.01, C01088(2017) **[4]** W. Wu, IEEE Transactions on Nuclear Science, vol. 66, no. 7, pp.986-992, July 2019. **[5]** Lefebvre, benoit , JINST 15 (2020) C07013