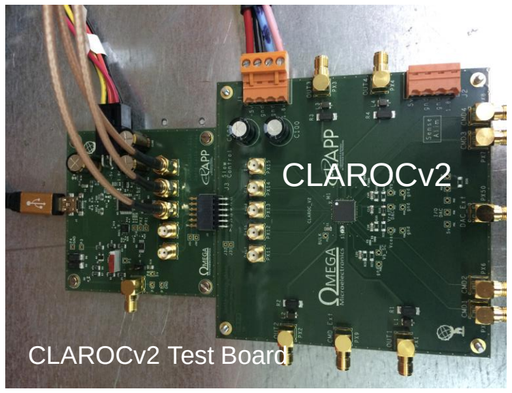
DEVELOPMENT OF THE ATLAS LIQUID ARGON CALORIMETER READOUT ELECTRONICS FOR THE HL-LHC

Mesut Unal
on behalf of the Liquid Argon Calorimeter Group

To meet new TDAQ buffering requirements and withstand the high expected radiation doses at the HL- LHC, the ATLAS LAr Calorimeter readout electronics will be upgraded.

Calibration Board



Injects accurately calibrated signals onto calorimeter cells

Requirements:

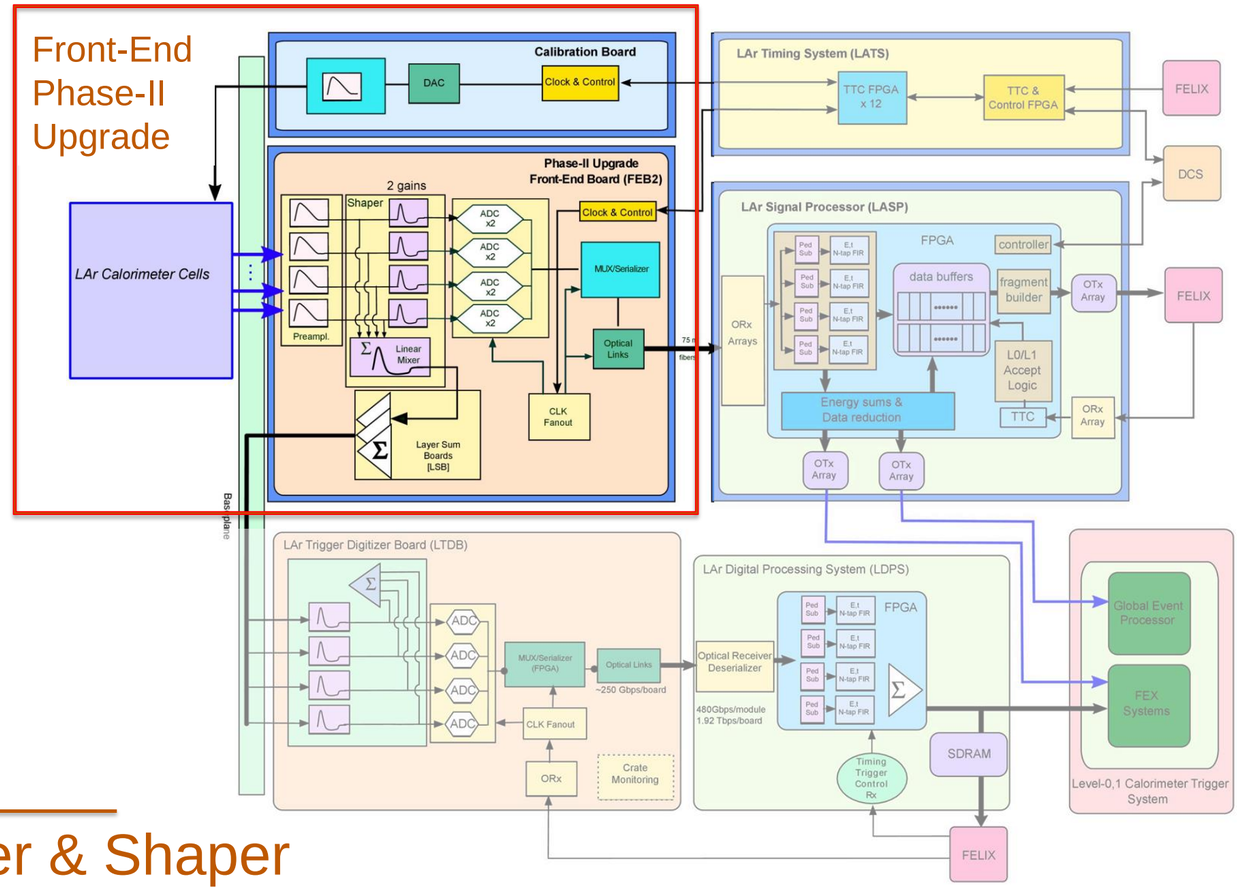
- 16-bit dynamic range
- Integral non-linearity (INL) < 0.1%
- Pulse rise time < 1ns
- Stable under irradiations until 1.4 kGy
- lpGBT integration

CLAROC

- Pulser ASIC, HV SOI CMOS Technology: XFAB 180 nm
- Dynamic range up to 320 mA, output up to -7.5V
- Each ASIC contains 4 calibration channels
- Two large transistors (PMOS, NMOS) of size 3mm/500nm

LADOC

- Radiation hard DAC
- TSMC 130 nm

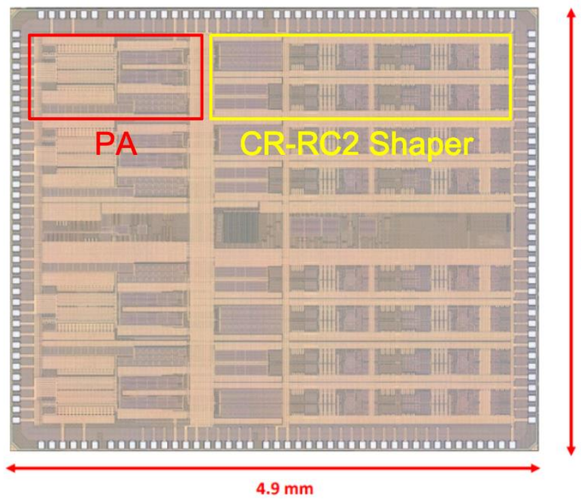


Pre-Amplifier & Shaper

Amplification and bipolar CR-$(RC)^2$ shaping of signal

ATLAS Liquid Argon Front End (ALFE)

- Baseline PA/Shaper
- Fully-differential pre-amplifier with two-gain shaper with differential outputs to the ADC
- 16-bit dynamic range, gain ratio ~23, 130nm TSMC
- Highly configurable via I2C

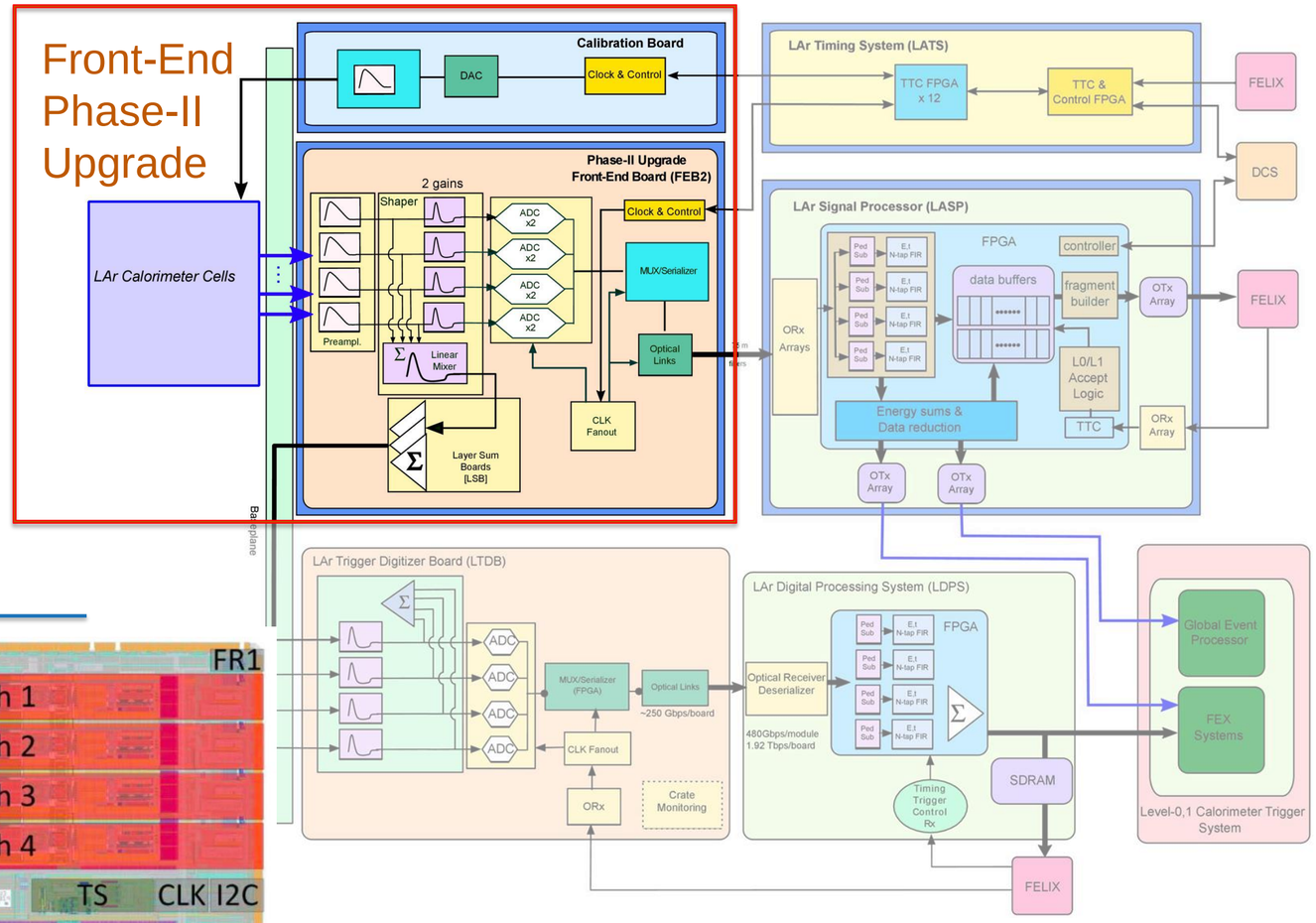


Pre-Amplifier & Shaper

Liquid Argon Upgrade Read Out Chip (LAUROC)

- Single-ended pre-amplifier with two-gain shaper with differential outputs to ADC
- Meets the requirements:
  - Dynamic range: 10 mA for 25 Ω channels, 2 mA for 50 Ω channels
  - Preamplifier noise: 350 nA for 10 mA channels, 120 nA for 2 mA channels
  - INL < 0.2%; sum of four channels sent to Level-0 Trigger

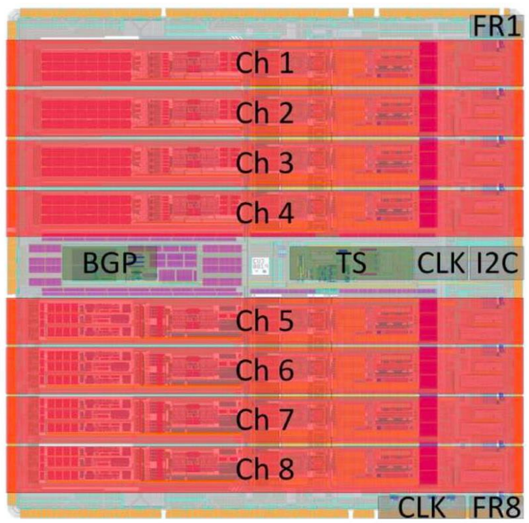
*Not retained because ALFE has a better performance



Analog-to-Digital Converter (ADC)

COLUTA

- Design ASIC for FEB2
- Baseline option
- Eight channel, 15-bit ADC
- Multiplying DAC + 12-bit pipeline SAR



- Performance measured by injecting a sine wave at different carrier frequencies
- Achieve precision of 11.7 and 11.3 bits at 1 & 8 MHz
- DNL < ±1.0 15-bit LSB, no missing codes
- INL < 0.03%
- Digital Data Processing Unit (DDPU) block computes ADC codes and outputs data to optical links at 640 MHz

Meets design requirements:

- Digitize both gains of 4 calorimeter channels per ADC ASIC (ie. 8 ADC/ASIC)
- Digitize at 40 MSPS
- 14-bit dynamic range, > 11-bit precision
- Radiation hardness

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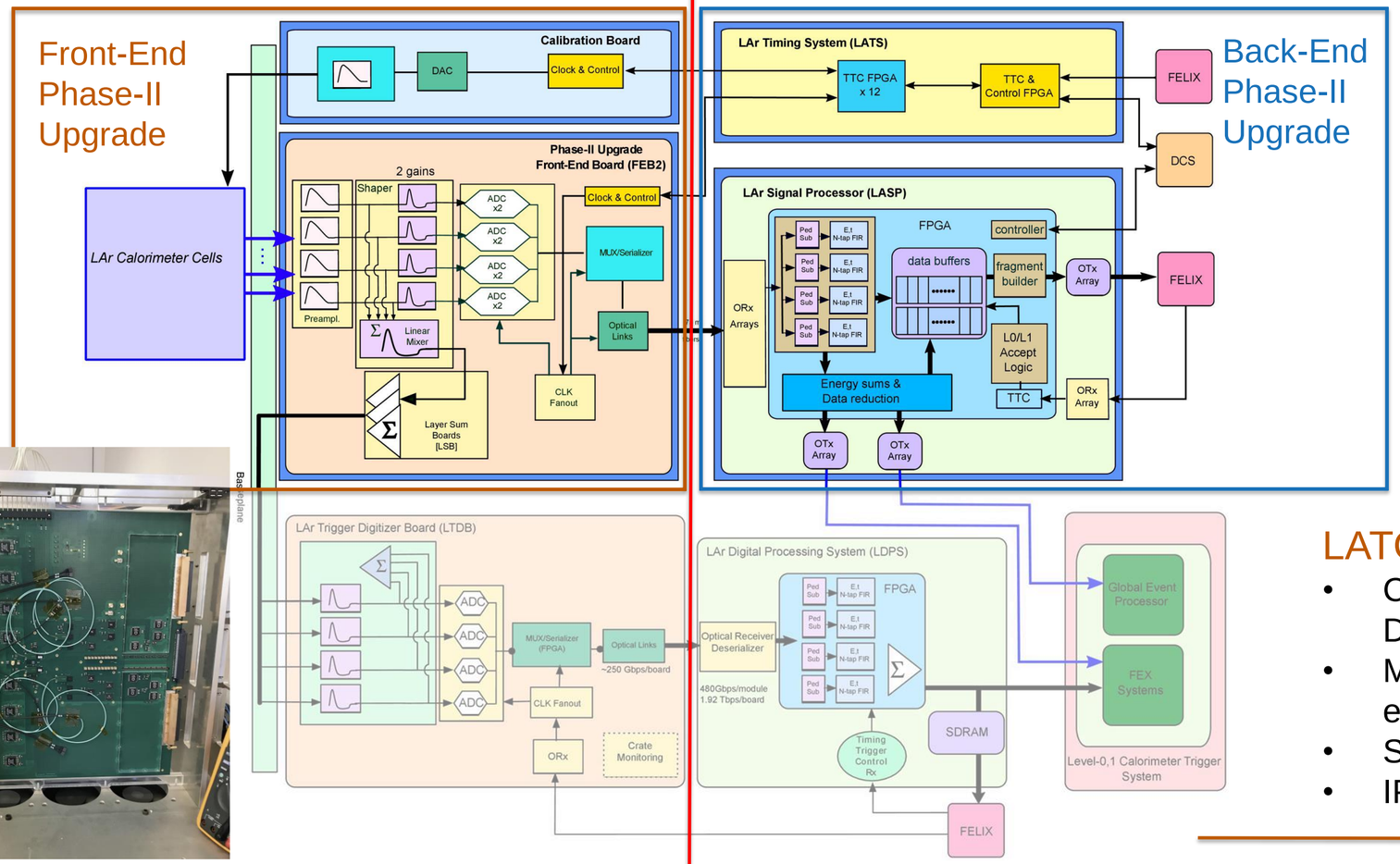
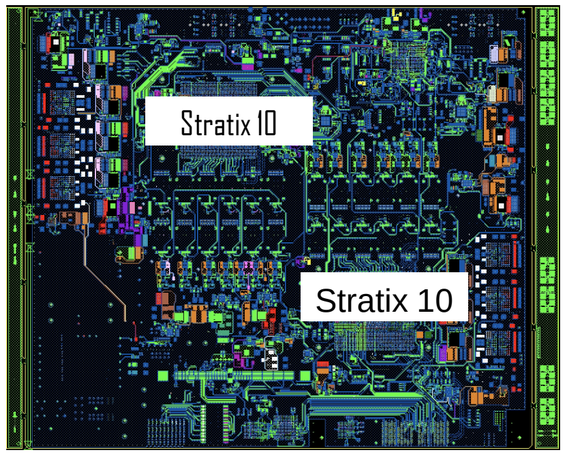


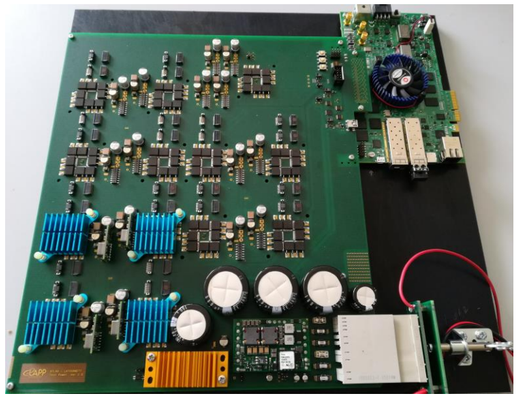
Front-End Board 2 Slice Testboard

- Can contain pre-prototype versions of preamplifier-shaper and ADC, layer sum boards, radiation-tolerant power distribution, optical links for data and control
- 32-channel readout
- Full readout chain working



LATS

TTC distribution, configuration and monitoring of FEBs and calibration boards



LATOURNETT

- Central FPGA (Cyclone 10 GX): connections to FELIX, DCS/Run Control
- Matrix FPGAs (Cyclone 10 GX): connections to FE electronics
- System on Module: Embeds OPC UA, Linux distribution
- IPMC: read critical sensors

LASP

- Apply digital filtering to data from FEB2 (512 channels)
- Digital filtering, buffer and output data to TDAQ at 25 Gbps
- Testboard design is complete
- Firmware development (Intel Stratix 10) in progress

References:
- ATLAS-TDR-027
- ATL-COM-LARG-2020-001
- AT2-AL-CD-0001 v.1.1