Firmware of the ATLAS Level-0 Endcap Muon Trigger for HL-LHC

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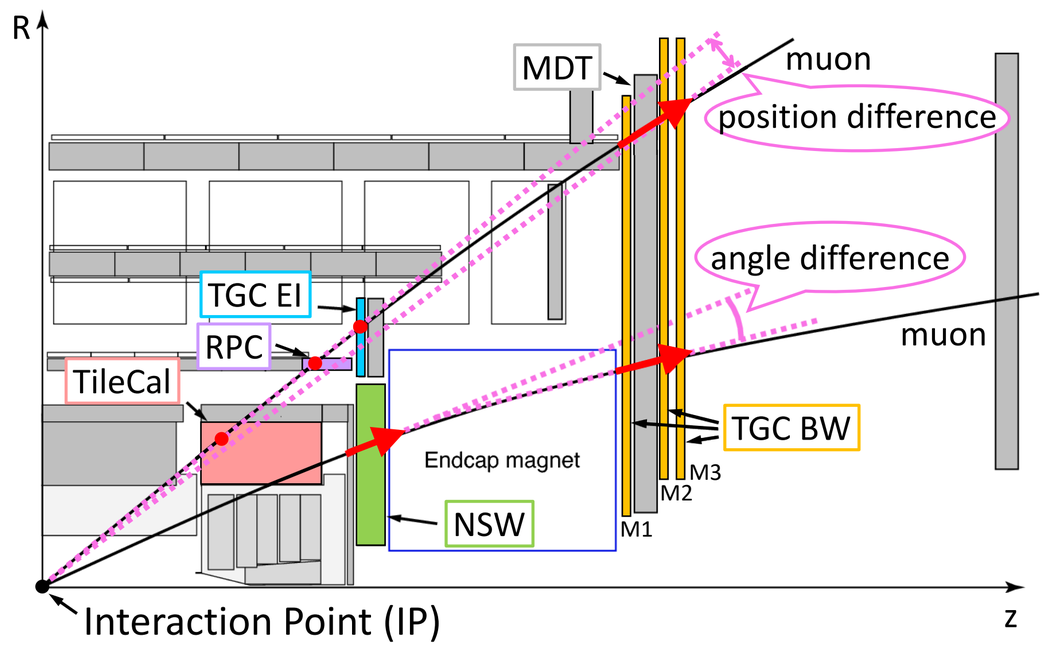
Introduction

High-Luminosity LHC (HL-LHC) is planned to start its operation in 2027 with an instantaneous luminosity of $7.5 \times 10^{34}\ \mathrm{cm^{-2}s^{-1}}$. To cope with the increase of luminosity, the ATLAS trigger and readout system will be upgraded [1]. The new system triggeris based on a single-level hardware trigger (Level-0) with a maximum rate of 1 MHz and 10 μs latency. Overview of the Level-0 endcap muon firmware for HL-LHC and the status of the development are presented.

Level-0 endcap muon trigger at HL-LHC

- Primary outer detector: Thin Gap Chamber on Big Wheel (TGC BW) consisting of three stations (M1, M2 and M3)
  - Multiwire proportional chamber at endcap (pseudorapidity $|\eta|$ = 1.05 − 2.4)
  - Two-dimensional position measurement using signals from wires and strips orthogonal to each other
- Original trigger scheme
  - Simple coincidence on signals from TGC BW
  - Transverse momentum (p_{T}) evaluation with look-up tables
- New trigger scheme for HL-LHC
  - Track segment reconstruction outside the magnetic field with all hit information from TGC BW
  - p_{T} determination based on position and angle difference for TGC BW track segment and signals from inner detectors: New Small Wheel (NSW), TGC in Endcap Inner (EI) station, Resistive Plate Chamber (RPC) in barrel inner station, and Tile hadronic calorimeter (TileCal)
  - More precise p_{T} evaluation with Monitored Drift Tube (MDT)

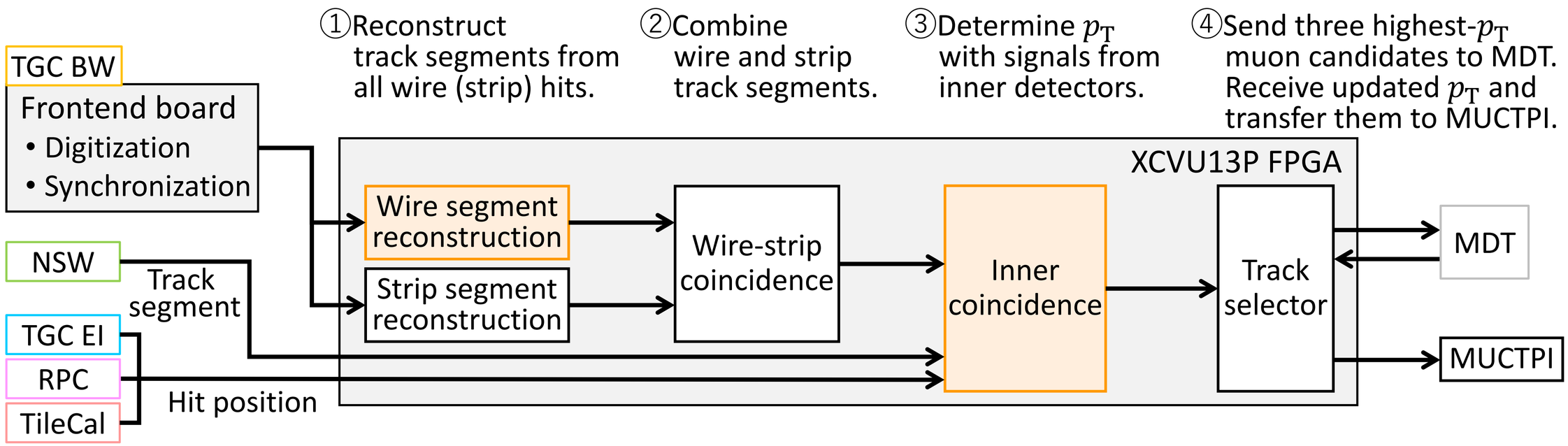


R-z view of ATLAS muon detectors (reference [1])

Firmware overview

- Trigger and readout algorithm implemented on a high-end large scale FPGA (Xilinx XCVU13P [2]). Firmware development ongoing with requiring resource utilization $\lesssim$ 50 % to avoid timing violations.
- Trigger firmware (see the bottom figure)
  - ➢Target: muon reconstruction efficiency > 90 %
  - ➢Method: reconstruct muons from hit information of all channels of TGC BW and sending them to "Muon to Central Trigger Processor Interface" (MUCTPI)
- Readout firmware: readout of TGC hits and trigger firmware data for the events accepted by the Level-0 trigger
- The wire segment reconstruction and the inner coincidence focused on

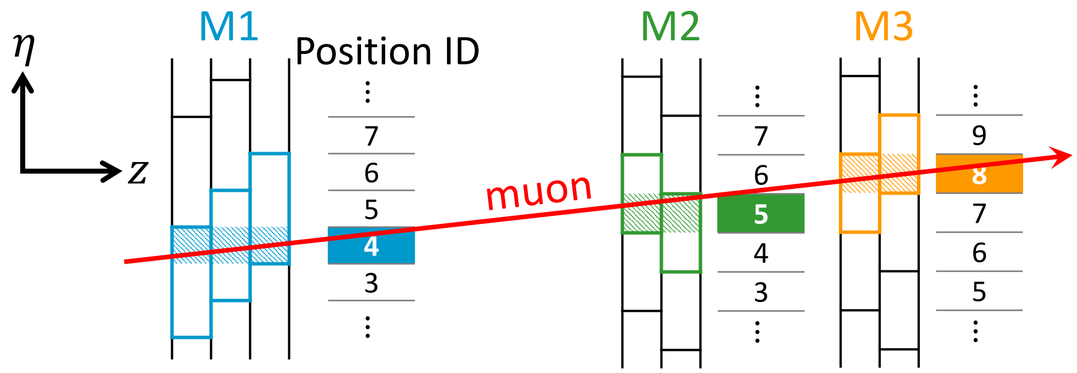
x-y view of the TGC BW (reference [3])



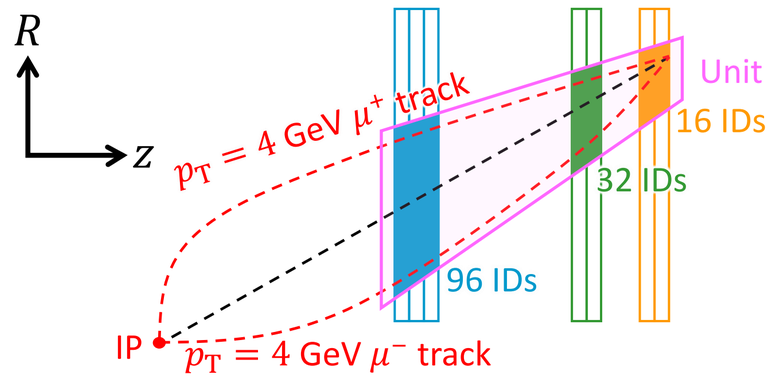
Wire segment reconstruction method

- TGC BW consisting of three stations;
  M1 (3 layers), M2 (2 layers) and M3 (2 layers)
- Segment reconstruction strategy:
  - ➢Hit position IDs determined by station coincidence
  - ➢Angle of track segment obtained by “pattern-matching”;
    Hit position IDs on three stations compared with
    a hit-pattern list predefined in FPGA RAM
- TGC BW divided into units of segment reconstruction
  - ➢Units defined as sets of position IDs to cover
    muon tracks with p_{T} > 4 GeV, with 16 IDs on M3
  - ➢Parallel segment reconstruction for small regions on TGC BW
    in a realistic circuit scale achieved by unit division
- Similar logic implemented for strip segment reconstruction

Station coincidence

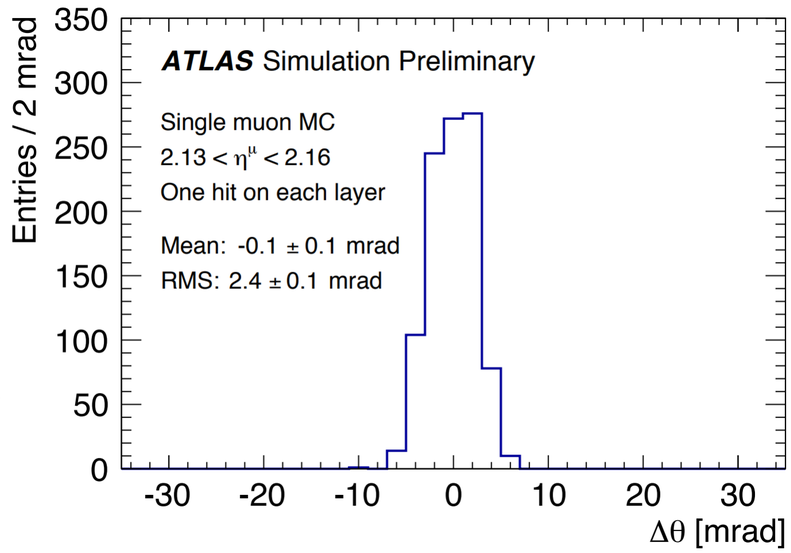


Unit of segment reconstruction



Implementation of wire segment reconstruction

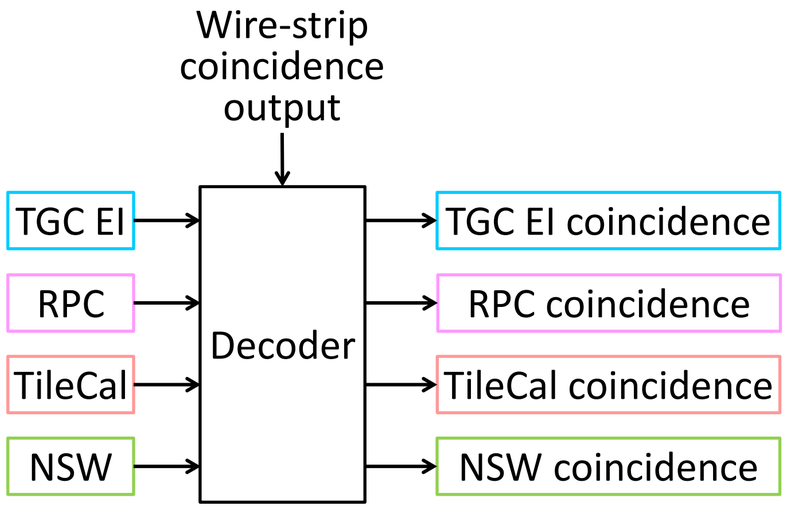
- Firmware for a specific unit developed and validated
  on FPGA with an evaluation board VCU118
  - ➢Angular resolution of 2.4 mrad obtained
    in the region with 2.13 < η < 2.16 [4]
- Expansion of the firmware to a whole sector (1/24 of TGC BW) in progress
  - ➢The firmware expanded successfully without timing violations
  - ➢Next step: validation for the full η range (1.05 − 2.4)

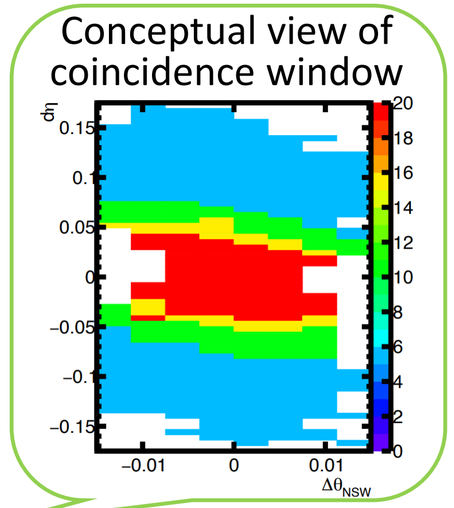


Comparison of track angles between TGC BW and offline reconstruction (reference [4])

Inner coincidence method

- TGC EI, RPC and TileCal for $|\eta|$ = 1.05 − 1.3
  - ➢Two-dimensional position information from the inner detectors used
  - ➢p_{T} evaluation with position difference between the TGC BW track segment and hits in the inner detectors
- NSW for $|\eta|$ = 1.3 − 2.4
  - ➢p_{T} evaluation with angular difference between the NSW track segment and the vector from IP to the NSW track segment ($\Delta\theta_{\mathrm{NSW}}$) and position difference between the track segments in TGC BW and NSW ($d\eta$)





TGC EI, RPC, TileCal and NSW data transferred to the coincidence blocks after decoding
Coincidence logic implemented in FPGA RAM
Decoder output: RAM address, Coincidence output: RAM data

Conclusions

The new ATLAS Level-0 endcap muon trigger is under development for HL-LHC. The new trigger reconstructs muon track segments from several detectors' signals. The TGC wire segment reconstruction is essential for initial muon candidates. The firmware for the wire segment reconstruction was validated in a specific region. Expansion of the firmware to the full range and the firmware for the inner coincidence with the other detectors are in progress.

Reference

[1] The ATLAS Collaboration, *Technical Design Report for the Phase-II Upgrade of the ATLAS TDAQ System*, CERN-LHCC-2017-020
[2] Xilinx Inc., https://www.xilinx.com/
[3] The ATLAS Collaboration, *Installation of the first of the big wheels of the ATLAS muon spectrometer, a thin gap chamber (TGC) wheel*, https://cds.cern.ch/record/986163
[4] The ATLAS Collaboration, *L0 Muon Trigger Public Results*, https://twiki.cern.ch/twiki/bin/view/AtlasPublic/L0MuonTriggerPublicResults