Institute for Collider Particle Physics
University of the Witwatersrand

Upgrade of ATLAS Hadronic Tile Calorimeter for the High Luminosity LHC

ATLAS EXPERIMENT

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on behalf of the Tile Calorimeter System

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TileCal in Context

- The Tile Calorimeter (TileCal) is a sampling calorimeter which forms the central section of the Hadronic calorimeter of the ATLAS experiment.
- TileCal performs several critical functions within ATLAS such as: the measurement and reconstruction of hadrons, jets, hadronic decays of τ-leptons and missing transverse energy. It also participates in muon identification and provides inputs to the Level 1 calorimeter trigger system.
- The detector is located within the region $\eta <|1.7|$ and is partitioned into four barrel regions. Each barrel region consists of 64 wedge shaped modules which cover $\Delta\varphi \sim 0.1$ and are composed of plastic scintillator tiles, functioning as the active media, inter-spaced by steel absorber plates.

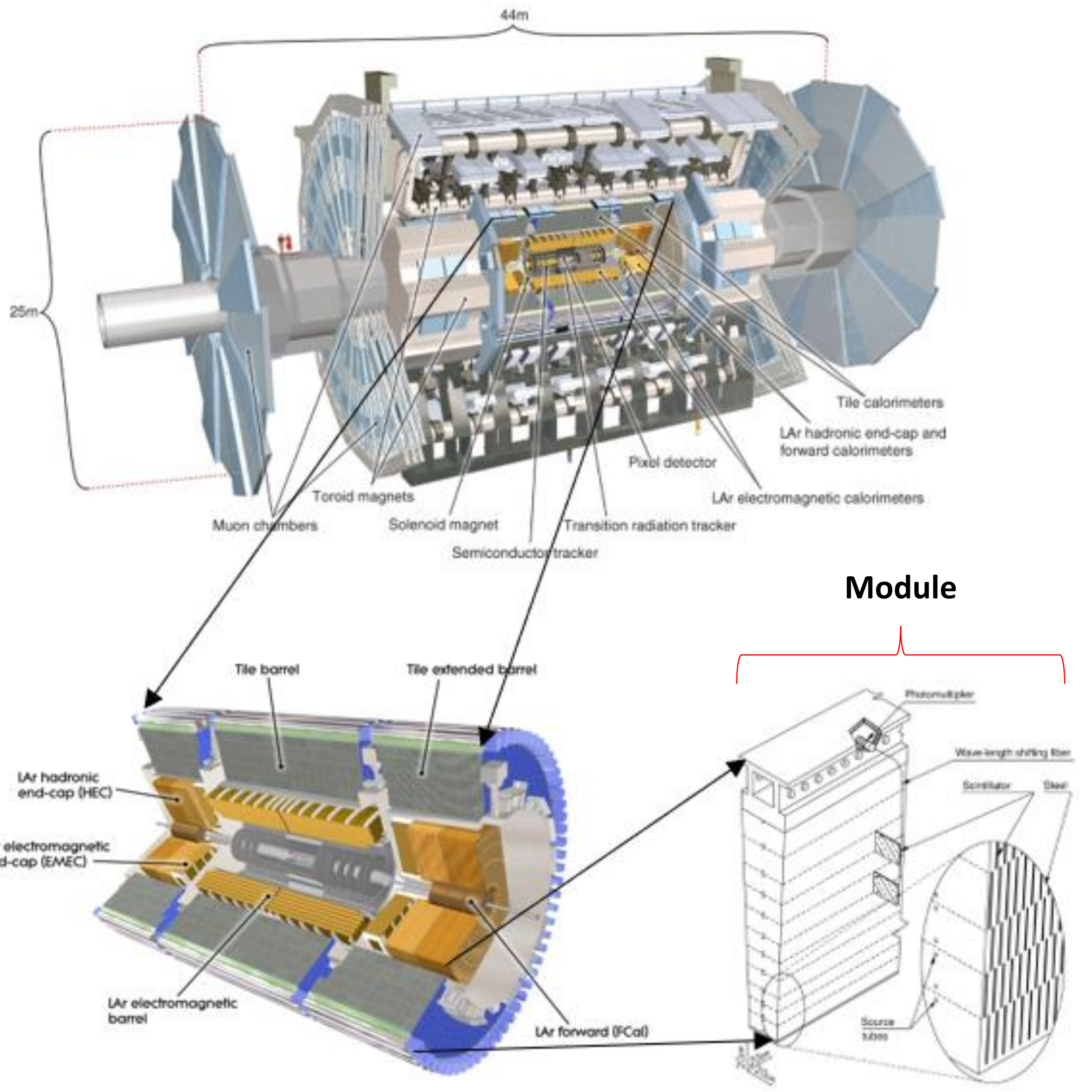

Fig. 1 Top - The ATLAS detector, Bottom left - The inner Barrel, Bottom right - A TileCal module*. J. Pequenao, Computer Generated image of the ATLAS calorimeter,(2008), https: // cds. cern. ch/ record/ 1095927*

TileCal Phase-II upgrade motivation

- In the year 2027 the start of the operation of the High-luminosity Large Hadron Collider(HL-LHC) is planned with a foreseen peak luminosity of $5 \times 10^{34} cm^{-2} s^{-1}$.
- The resulting HL-LHC environment has necessitated the development of new electronics, both on and off detector, in order to ensure the continued peak performance of TileCal.
- The new electronics need to meet the requirements of a 1 MHz trigger for the Level 1 trigger system, higher resistance to ambient radiation exposure and improved performance under pileup conditions.
- A total of 768 PMTs located in the most exposed regions will be replaced due to aging.

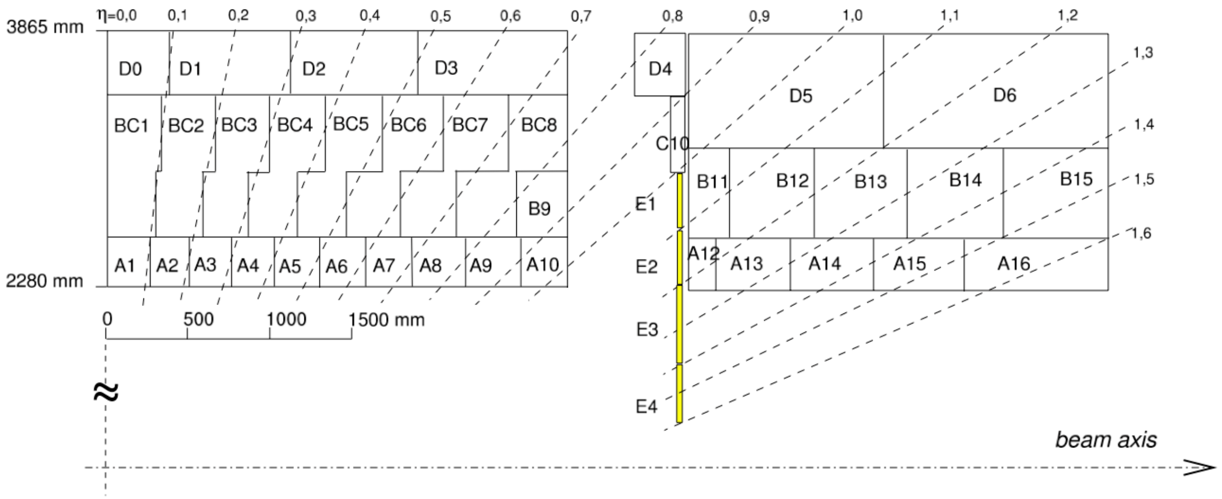

***Fig. 2 Schematic showing the TileCal cell and scintillator structure**, including E-cells (E1-E4) which are highlighted in yellow.* ApprovedDetectorReferenceFiguresAndSchematics < AtlasPublic < TWiki (cern.ch)

	30 fb⁻¹		150 fb⁻¹		300 fb⁻¹		3000 fb⁻¹ integrated luminosity	
Most exposed cell per layer	**PMT integrated anode charge (C)**	**Measured PMT response loss (%)**	**PMT integrated anode charge (C)**	**Measured PMT response loss (%)**	**PMT integrated anode charge (C)**	**Measured PMT response loss (%)**	**PMT integrated anode charge (C)**	**Measured PMT response loss (%)**
A13	5	-5	25	-15	50	-20	500	-50
B11/C10	1.5	>-3	8	-5	15	-7	150	-15
D4	1	>-2	5	-2.5	10	-6	100	-9

Fig. 3 Estimation of the PMT response loss at HL-LHC era.

Time evolution of the PMT response shows a fairly exponential decay shape both for measurements of on-detector sample and for test bench measurements. Assuming that the PMT response degrades exponentially and estimating the decay constant from the available measurement at the end of run I ad after 20 and 35 fb-1 in run II, it is possible to estimate PMT response loss. At the end of HL-LHC era, more exposed PMTs will have lost 50% of their response.

https://twiki.cern.ch/twiki/bin/view/AtlasPublic/ApprovedDetectorReferenceFiguresAndSchematics

TileCal Phase-II Upgrade power distribution

High Voltage (HV) Distribution System

- The HV distribution system provides regulated high voltage to individual HVADs. It consists of HVremote boards that provide primary HV which is distributed to the HVADs via passive HVbus boards located within the Minidrawers.
- The upgrade removes the radiation hardness requirements of the HV regulators as regulation is now implemented off-detector

Low Voltage Distribution, Control and Monitoring System (LVDCMS)

- This system provides low voltage power to the front-end electronics of the Superdrawers. The off detector Auxiliary boards (AUXboards) operate as 200 VDC power supplies as well as perform control and monitoring functions via the Embedded Local Monitoring Board (ELMB) of the Low Voltage Power Supplies (LVPS), of which there is one per TileCal module. The new on detector LVPS is radiation hard and is comprised of eight Bricks which function to step-down the 200 VDC received from the AUX boards to the 10 VDC required by the Point-of-load regulators located on the MBs as well as an ELMB.

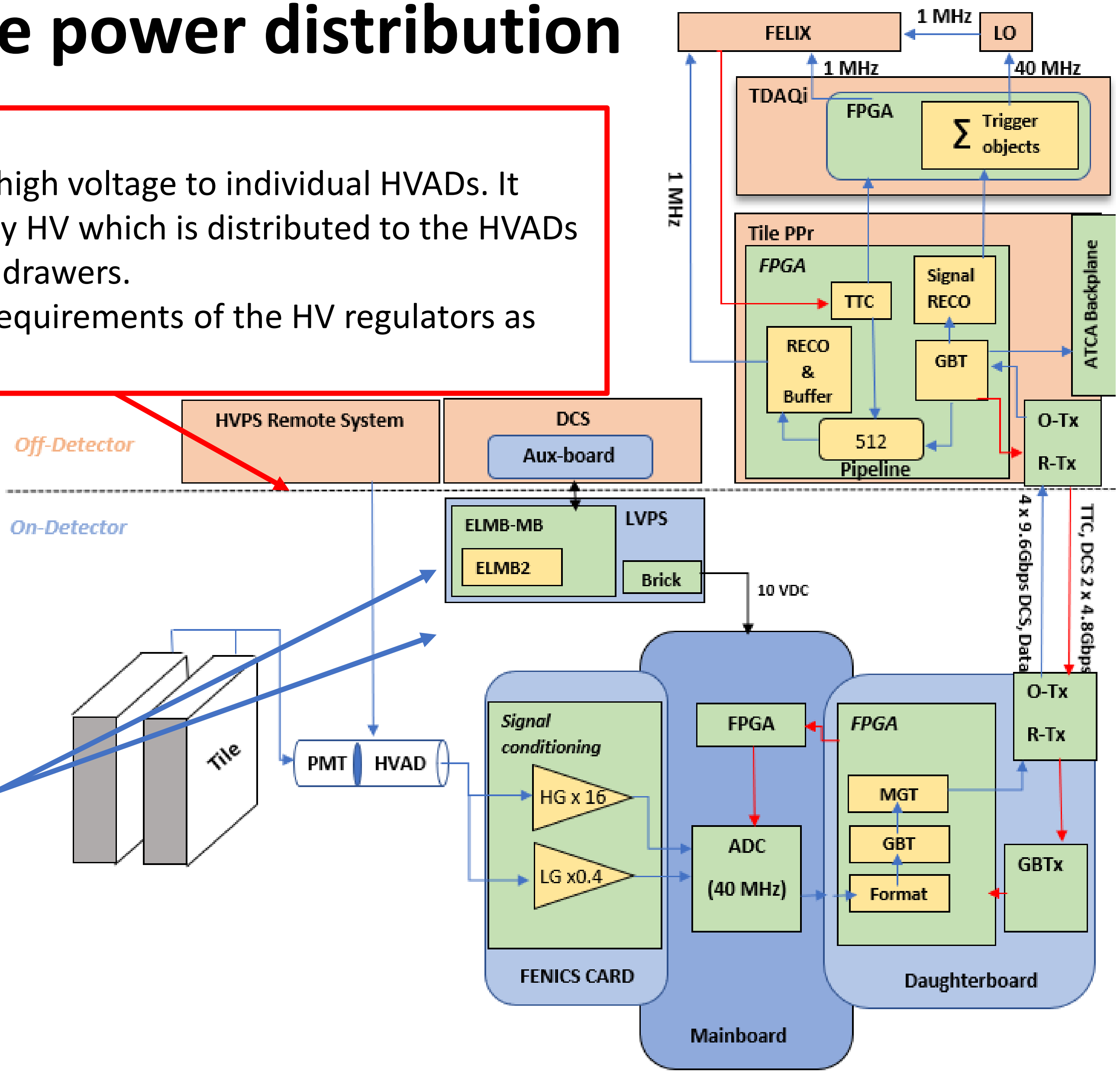

Fig. 4 The upgraded readout chain and power distribution of TileCal.

MD: Mini Drawer
SD: Super Drawer
PMT: Photo multiplier Tube
FELIX: Front-End Link eXchange
TDAQi: Trigger and Data Acquisition Interface
FPGA: Field Programmable Gate Array
PPr: Pre Processor
ADC: Analog To Digital Converter
HVAD: High Voltage Active Divider
DCS: Detector Control System
ELMB: Embedded Local Monitoring Board
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TileCal Phase-II Upgrade mechanics

- The On-detector electronics are housed in a new modular configuration in which one drawer (Superdrawer) is composed of 4 functionally independent Minidrawers (MD).
- The new configuration simplifies installation and manipulation creating better conditions for servicing within the high radiation environment.

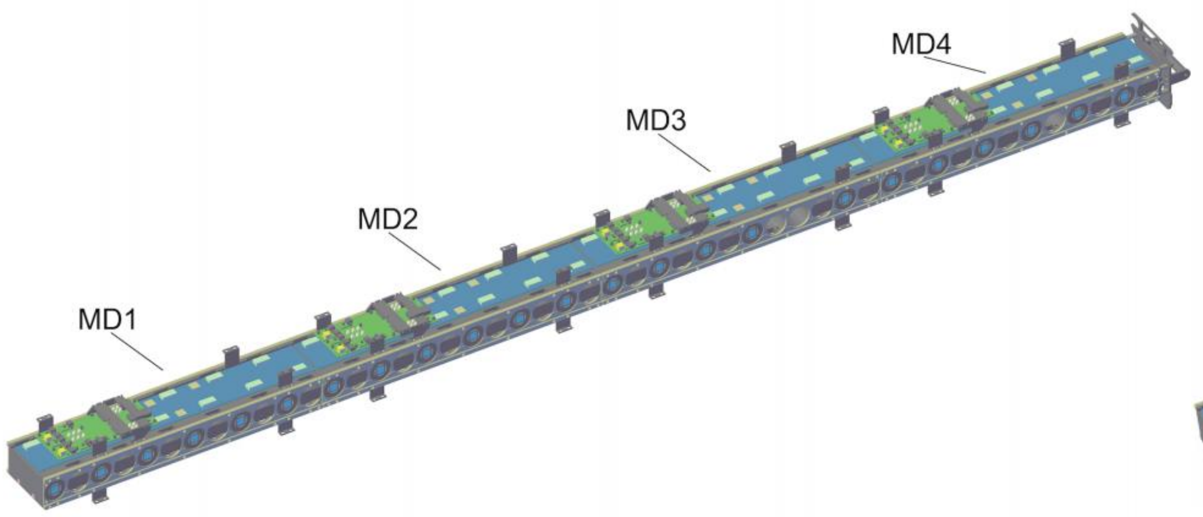


Fig.5 Tile new super-drawer architecture, ATL-TDR-028 · LHCC-2017-019, pg 69

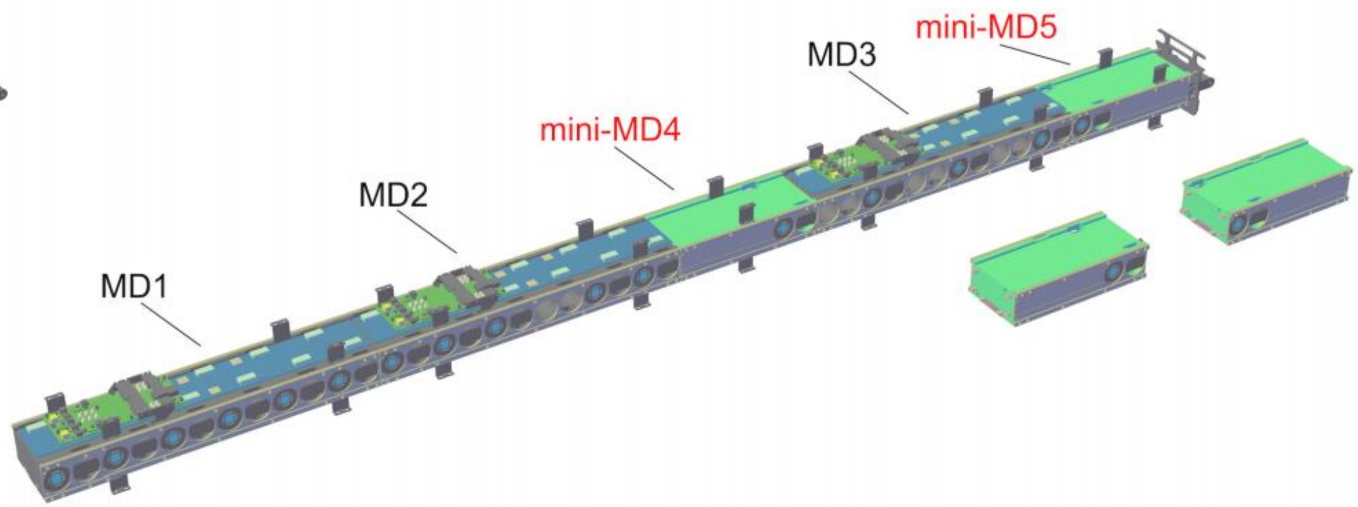
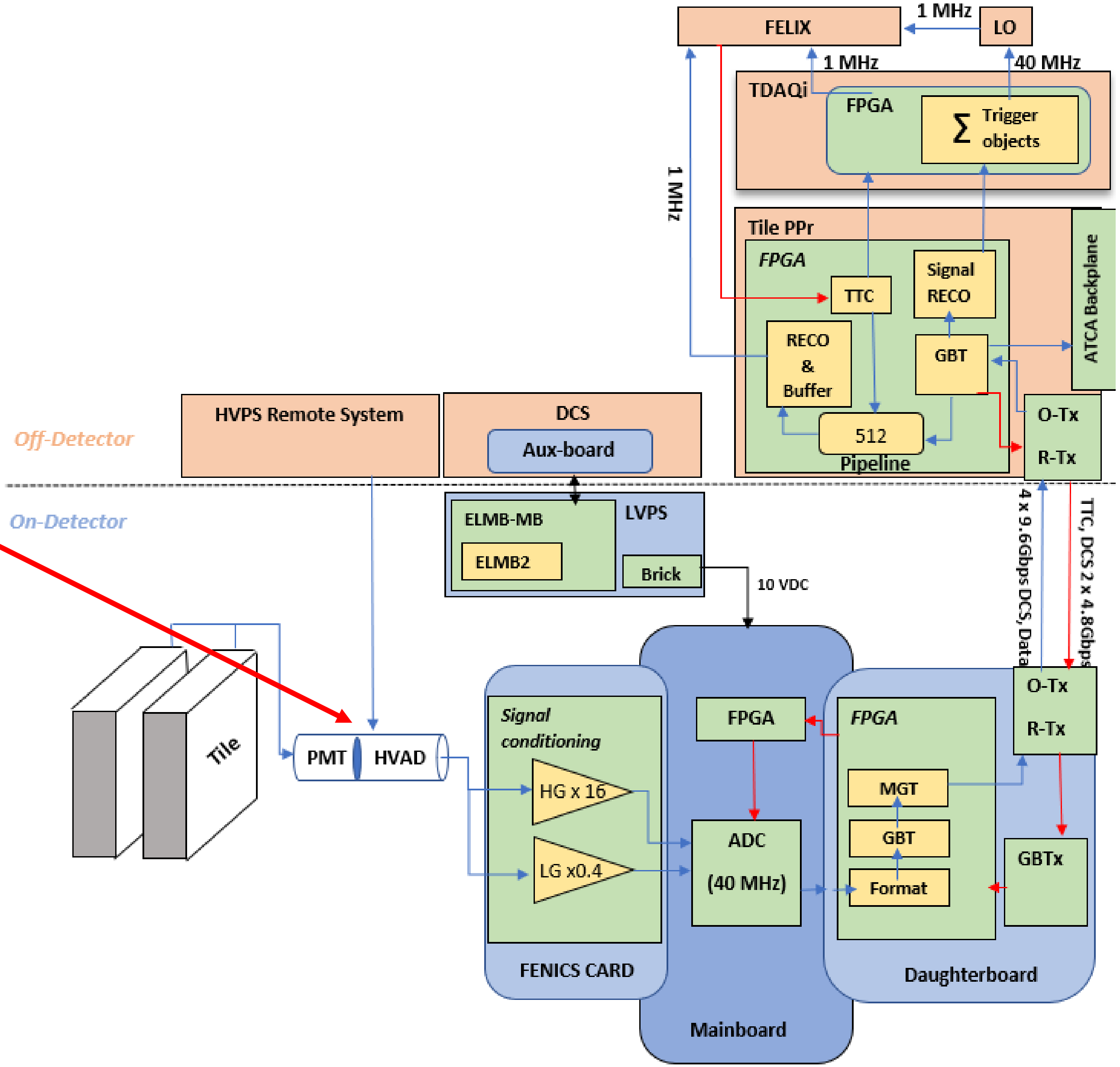


Fig.6 Super-drawer architecture designed explicitly for Extended Barrels modules, ATL-TDR-028 · LHCC-2017-019, pg 70

PMTs and High Voltage Active Dividers(HVADs)

- PMTs receive scintillation light via wavelength-shifting fibres. This light is then converted into electrical signals.
- A total of 768 PMTs located in the most exposed regions will be replaced due to aging.
- The HVADs make use of transistors and diodes in addition to passive components. They are responsible for dividing the received high voltage power between the individual dynodes of a PMT.
- The Upgrade ensures that the calorimeter performance, in terms of linearity and energy resolution for the measurement of highly energetic jets is maintained.



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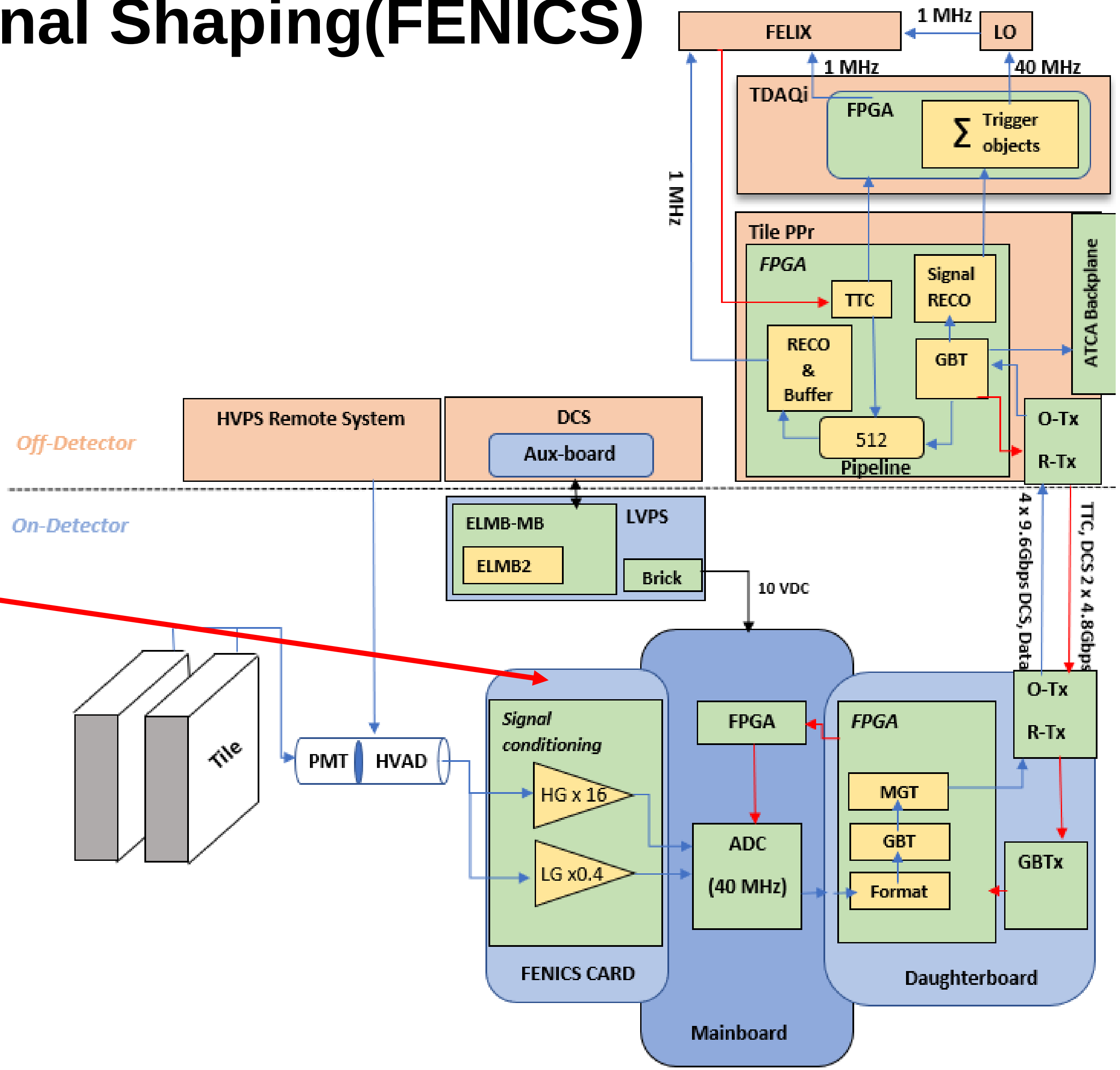
Front End board for the New Infrastructure with Calibration and signal Shaping(FENICS)

- A readout board responsible for the amplification and shaping of current received from a single PMT that is also involved in calibration as it contains the Charge injection system.
- FENICS reads the fast signals (full width at half maximum 25 ns) using two gains (x32, x1) and reads the averaged current (integration time 10ms) using six gains (0.3, 25, 25.3, 50.3, 125.3,150.3V/µA)



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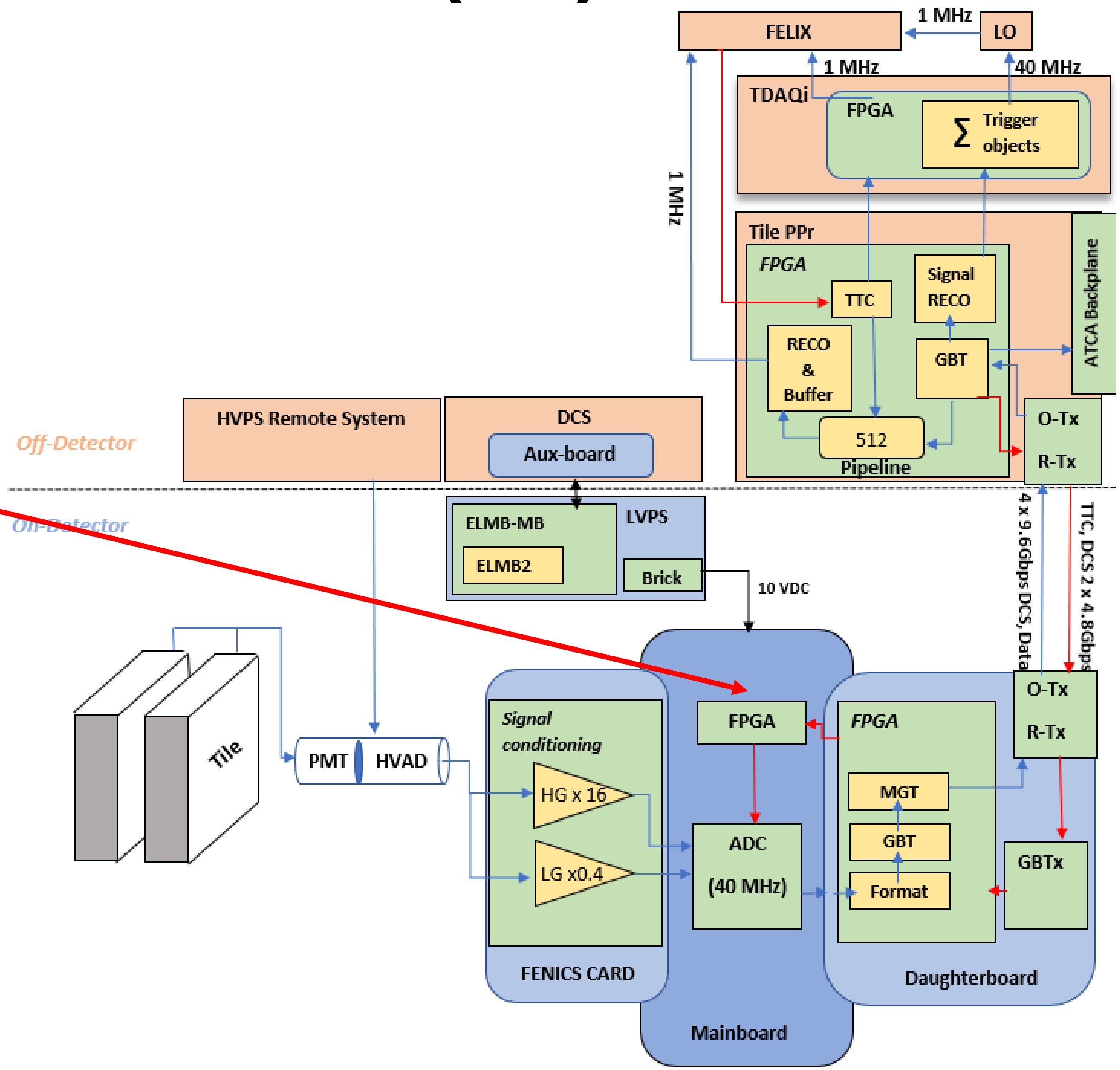
Mainboard (MB)

- There is an MB located in each Mini-drawer of TileCal. A single MB interfaces with twelve FEN-ICS and one DB. A MB digitizes the low and highgain signals received from the FENICS which arethen sent to its associated DB.
- An Upgraded MB is functionally divided into two halves for redundancy, provides digital control of the front end boards using Field-Programmable Gate Arrays (FPGAs), and features voltage and current monitoring.



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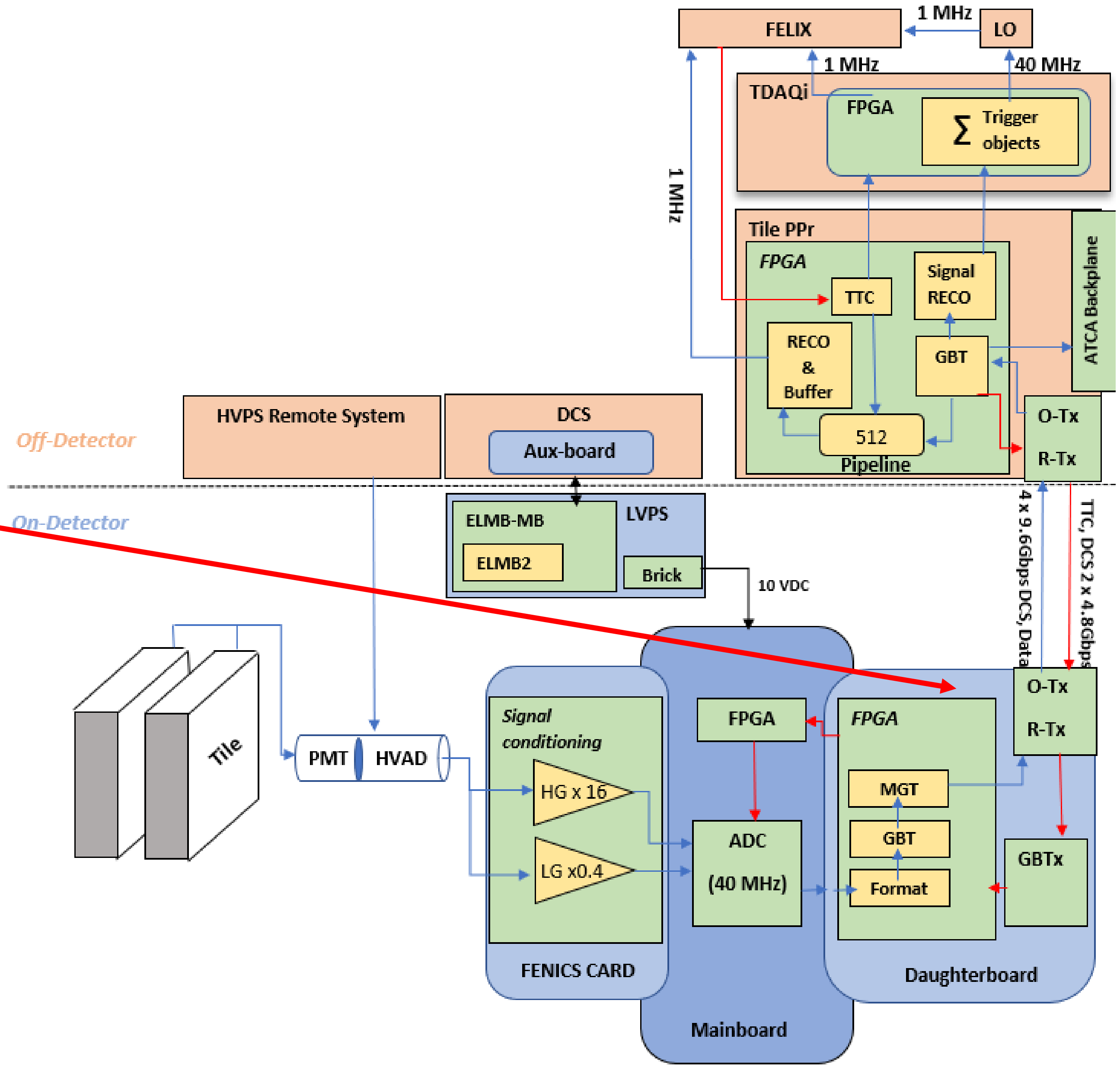
Daughterboard (DB)

- The DB is the primary interface between the on and off detector electronics of TileCal and is mounted on an MB. A DB sends detector data to the off-detector electronics, receives and distributes LHC clocks, configurations and slow-control commands.
- Major changes to the DB include using FPGAs with improved power sequencing as well as im-proved routing from the MB Analogue to Digital Converters (ADCs) to achieve better readout timing performance.



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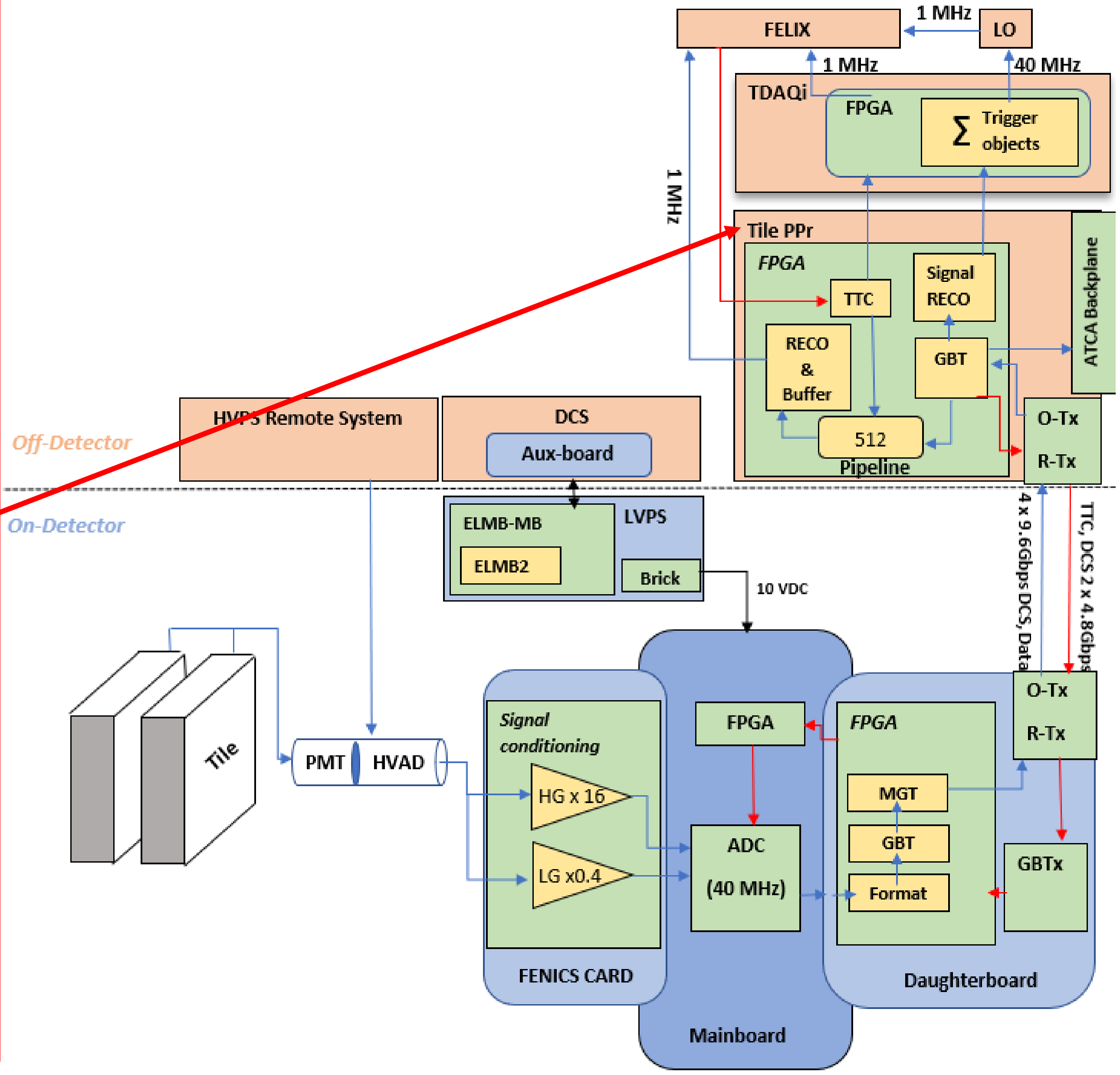
PreProcessor (PPr)

- A PPr is composed of four Compact Processing Modules(CPMs) and an Advanced Telecommunications Computing Architecture (ATCA) carrier board. Each CPM will read out and operate up to two TileCal SDs via high-speed optical links.
- A CPM implements a bi-directional GigaBit Transceiver communication with four 9.6 Gbps uplinks and two 4.8 Gbps downlinks per mini-drawer. The uplinks transmit detector and monitoring data to the CPMs. The downlinks provide Detector Control System (DCS) commands and Timing, Trigger, and Control information to the on-detector electronics, as well as the LHC clock for the sampling of the PMT signals.
- Deposited energy is reconstructed and calibrated in real-time using the received digitized samples. The CPM transmits this data to the TDAQi via the ATCA carrier board at the LHC frequency via four 9.6 Gbps optical links



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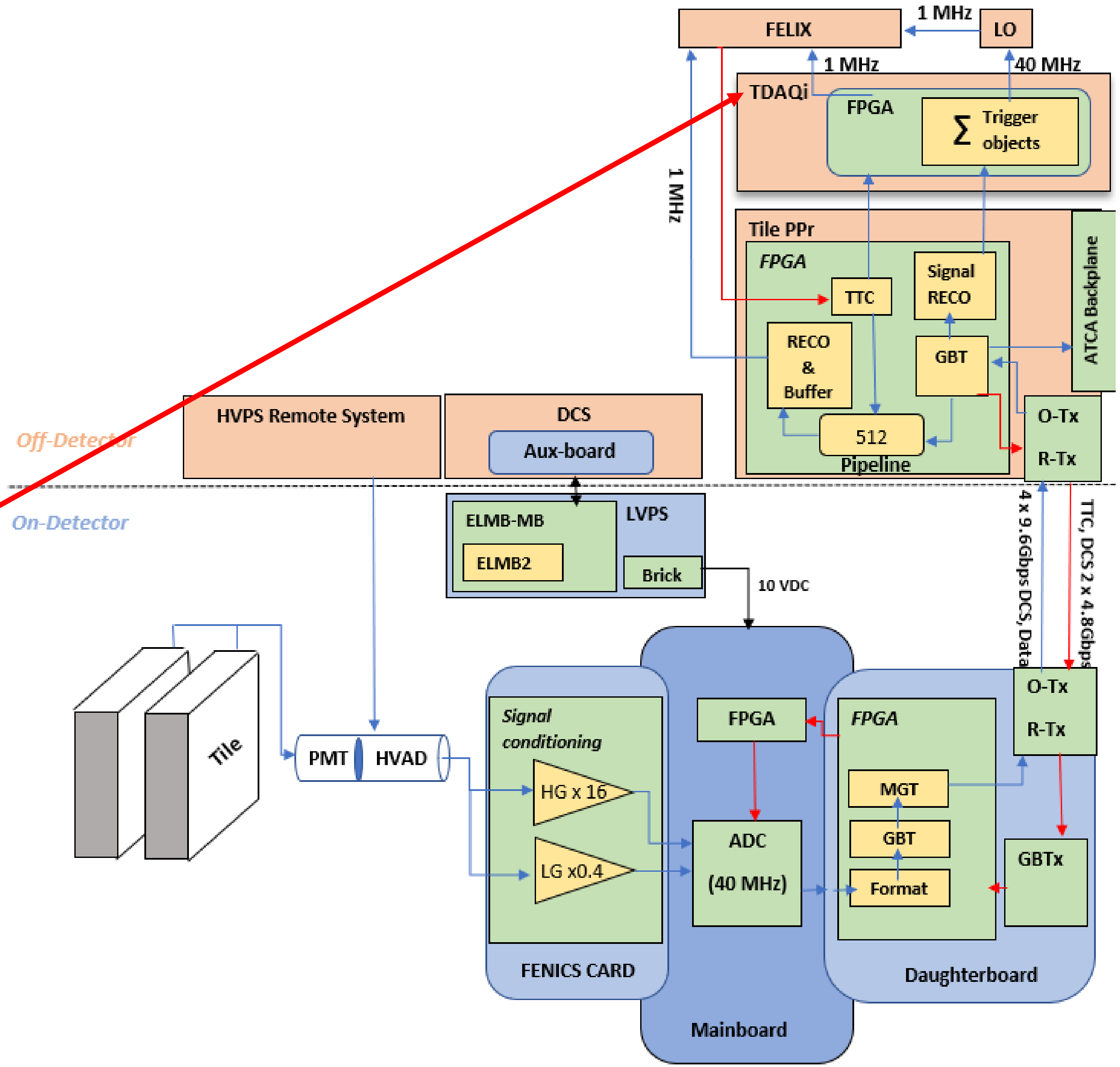
Trigger and Data AcQuisition Interface(TDAQi)

- All interfaces between the TileCal and TDAQ are implemented in the TDAQi module.
- The TDAQi constructs the trigger primitives and interfaces with the trigger and FELIX systems.
- The Trigger FPGAs compute trigger objects for electrons, jet, global, and muon triggers and the results are transmitted through low latency high-speed optical links to the L0 trigger.
- Trigger sums changing from analog to digital.



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Upgraded calibration systems

TileCal is equipped with calibration systems that allow for monitoring and calibration of the responses of the different components of the detector.

Cesium System:

- To calibrate and monitor the full optical path of TileCal a system ofCs137gamma sources, driven by a liquid flowthrough all the scintillating tiles, is used.
- New highly radiation-tolerant control boards oftheCs137system to be implemented as well as a new optical link interface with the DCS.

Laser System:

- A laser source is installed off-detector which provides light to the PMTs through 400 optical fibres.
- A new control and interface board with TDAQ and DCS is being introduced. The light mixer will also be replaced by an integrating sphere to add a controlled source of DC light to simulate underlying minimum bias events during calibration.

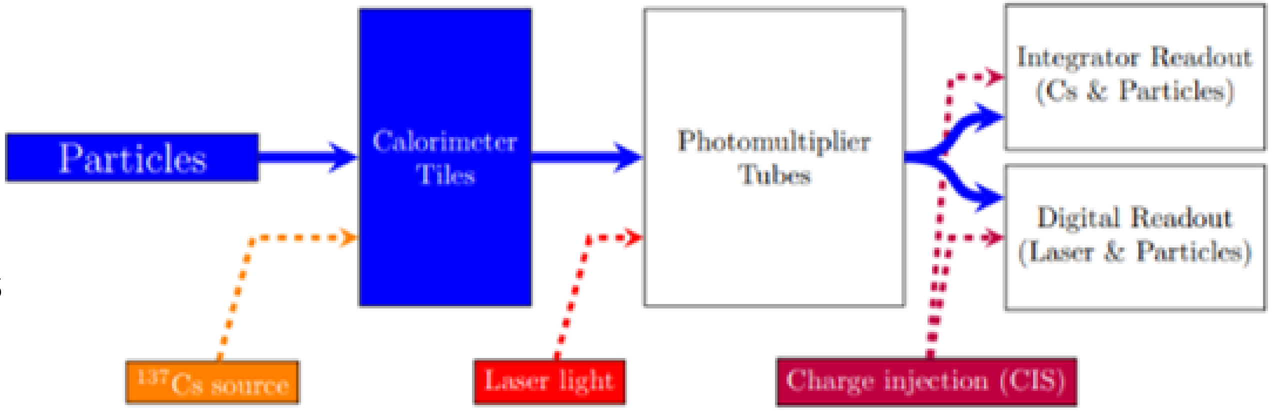

Fig. 7 TileCal Calibration systems along the signal chain.

2021 Test Beam Campaigns

- The calorimeter setup in the H8 beam of the CERN SPS consists of two fully functional long-barrels and one extended-barrel module allowing for the testing of any upgrade electronics without the need to install them within TileCal.
- Building upon past successful test beams, two new test beams will be undertaken in September and November of 2021.
- The primary goal is to test the response of the HL-LHC module readout.
- The following electronics will be installed: Up-grade HV Distribution System, Upgrade LVPS-DCS, Upgrade V4 MBs, Upgrade V6 DBs, Up-grade FENICS2, Upgrade PPr and CPM.

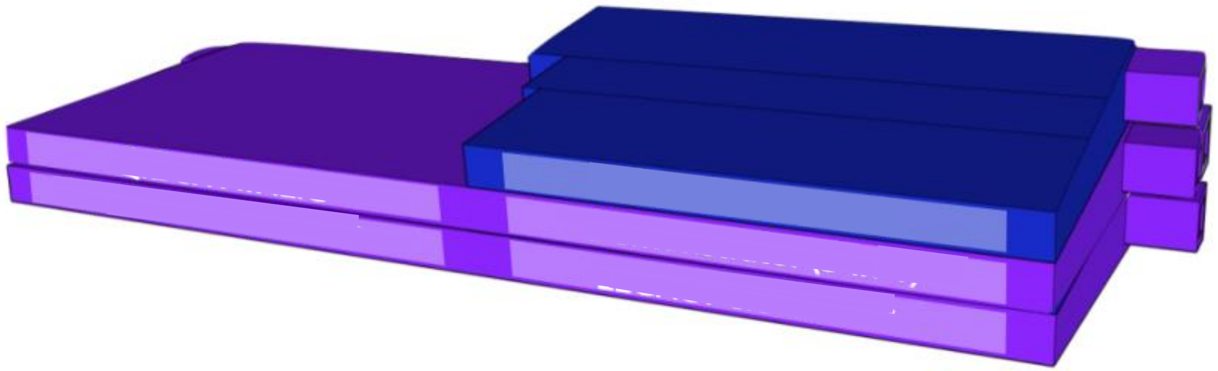

Fig. 8 Test beam module composition.

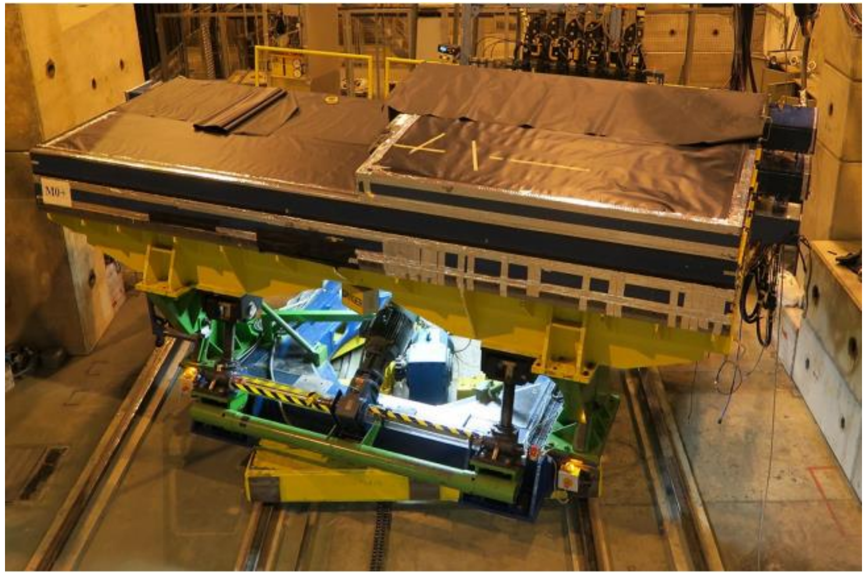

Fig. 9 Picture of the test beam modules and the mobile table, ATLAS-TDR-028 pg 169.

The END