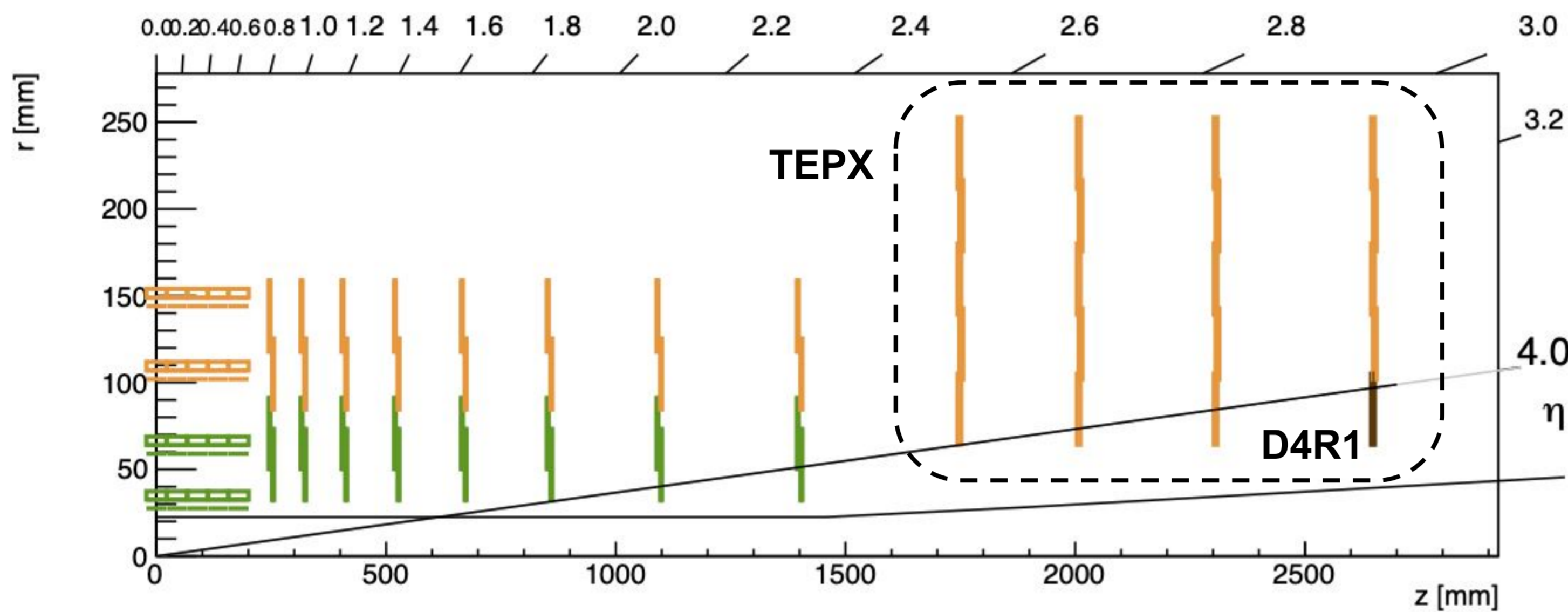


Overview

The Tracker Endcap Pixel Extension (TEPX) will be located in the very forward extremity of the CMS inner tracker volume. It will extend from 1750 mm to 2650 mm in longitudinal, and from 63 mm to 255 mm in radial direction. It will consist of 4 discs on both ends of the CMS Interaction Point (IP), each having 5 rings with varying number of pixel modules.



TEPX is planned to be used by BRIL as an independent luminosity and Beam-Induced Background (BIB) detector in LHC Phase 2, with the following properties:

- More than 800 million individual pixels distributed over a sensor area of 2 m²
- |z| position enabling good time separation (~17 ns) of collision products and BIB
- Low occupancy relative to other parts of the inner tracker allowing for high precision luminosity measurements

TEPX Front-End

- CMS Readout Chip (CROC): RD53B, a 65 nm radiation hard hybrid pixel detector chip
- Continuous operation during stable beams is required, independent of global physics DAQ and LHC beam mode
- Due to low occupancy from collisions, the readout bandwidth is planned to be split between physics and luminosity data
- Measured observables of TEPX will be pixel hits, clusters and coincidences between overlapping pixel modules

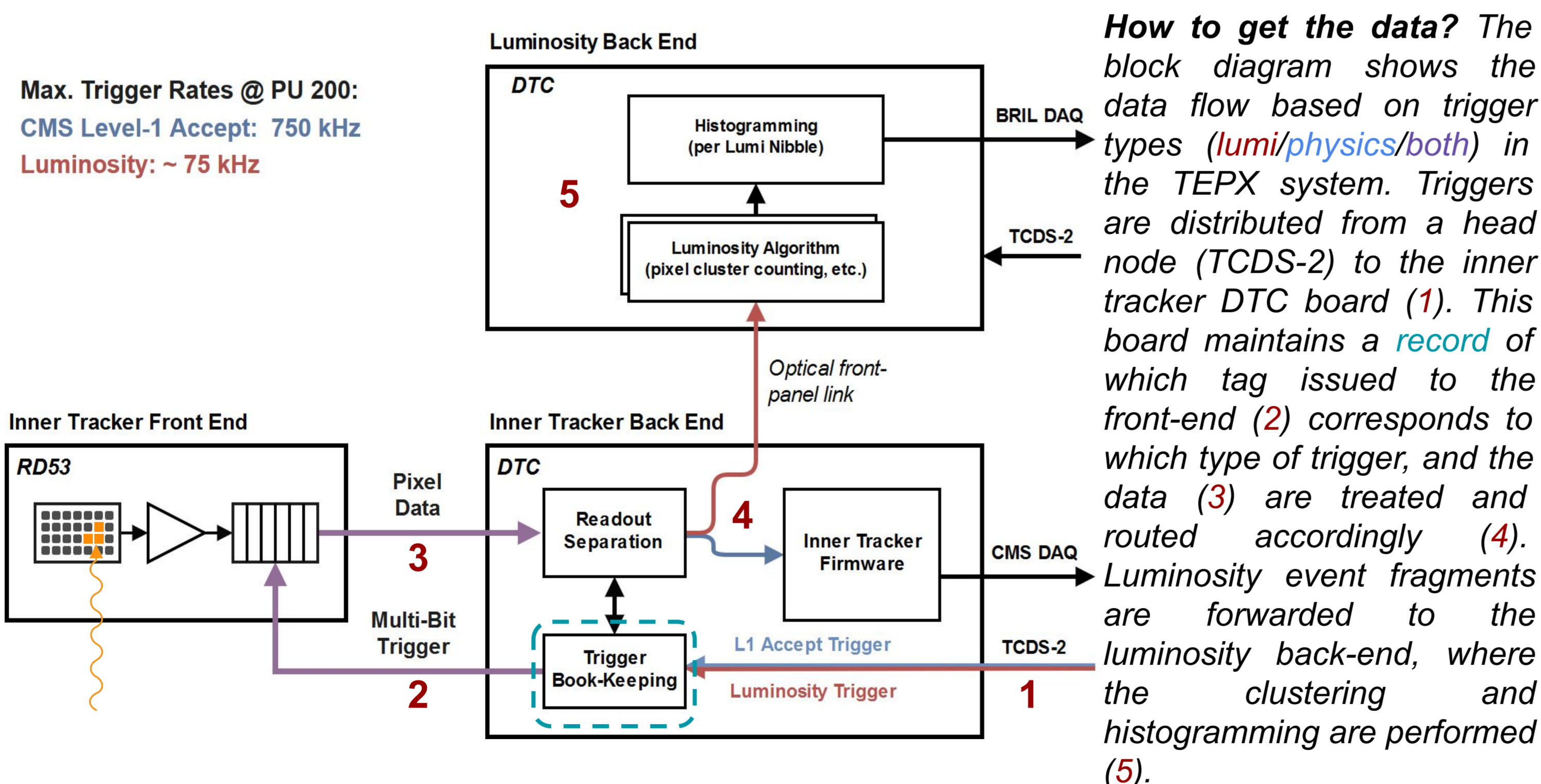
Trigger and Back-End

TEPX will use two different triggers, managed by the Data, Trigger and Control board (DTC) back-end, which steers configuration and data taking for all inner tracker detectors:

- Physics data taking with 750 kHz trigger rate
- Luminosity:
 - Under nominal physics conditions: up to 75 kHz trigger rate at pileup 200
 - During Van der Meer scans: up to 1 MHz trigger rate at pileup 0.5

Luminosity triggered data will be processed online via a cluster merging and histogramming algorithm running on FPGAs and housed on a dedicated DTC.

- Output: histograms of the number of clusters per bunch crossing per a specified detector granularity per time unit

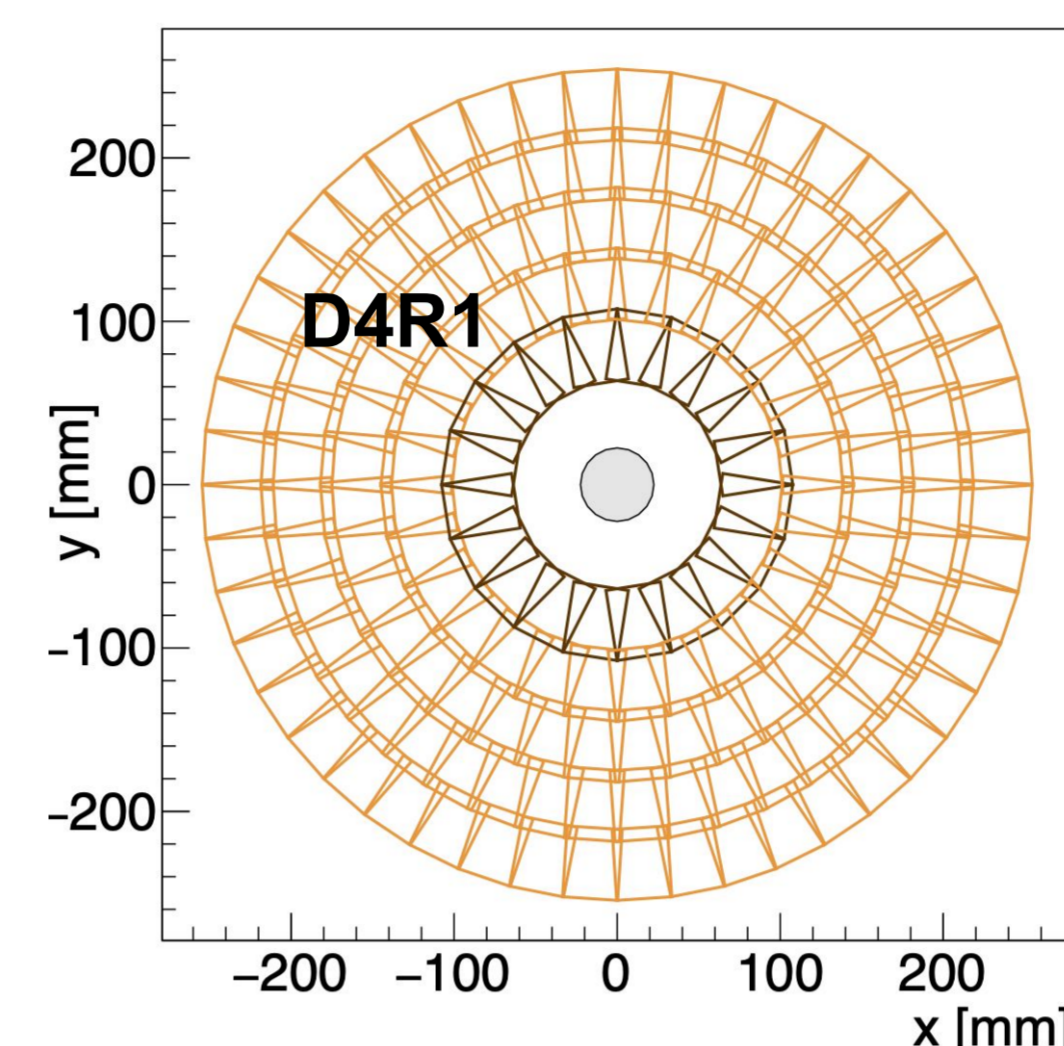


Expected Performance of the Clustering Algorithm

- Relatively low count mismatch rate: ~0.021%
- Data processing possible up to a trigger rate of 1 MHz
- FPGA resource utilization is less than 50%
- Nonlinearity less than 1% across relevant pileup range
- Identification of a cluster crossing multiple chips as a single cluster not possible
- No charge, cluster size and position information
- Out-of-time hits: ~6-12% due to time walk

TEPX Disc 4 Ring 1

Disc 4 Ring 1 (D4R1) of TEPX is not planned to be used for tracking due to its position at high pseudorapidity ($\eta > 4$). This enables BRIL to exploit it as an independent luminosity and BIB device for LHC Phase 2, making use of the full available readout bandwidth and trigger rate. In addition to the rest of TEPX, D4R1 will thus become a second source of luminosity measurements, with higher expected statistical precision.



D4R1 is foreseen to operate under the exclusive control of BRIL, which allows to:

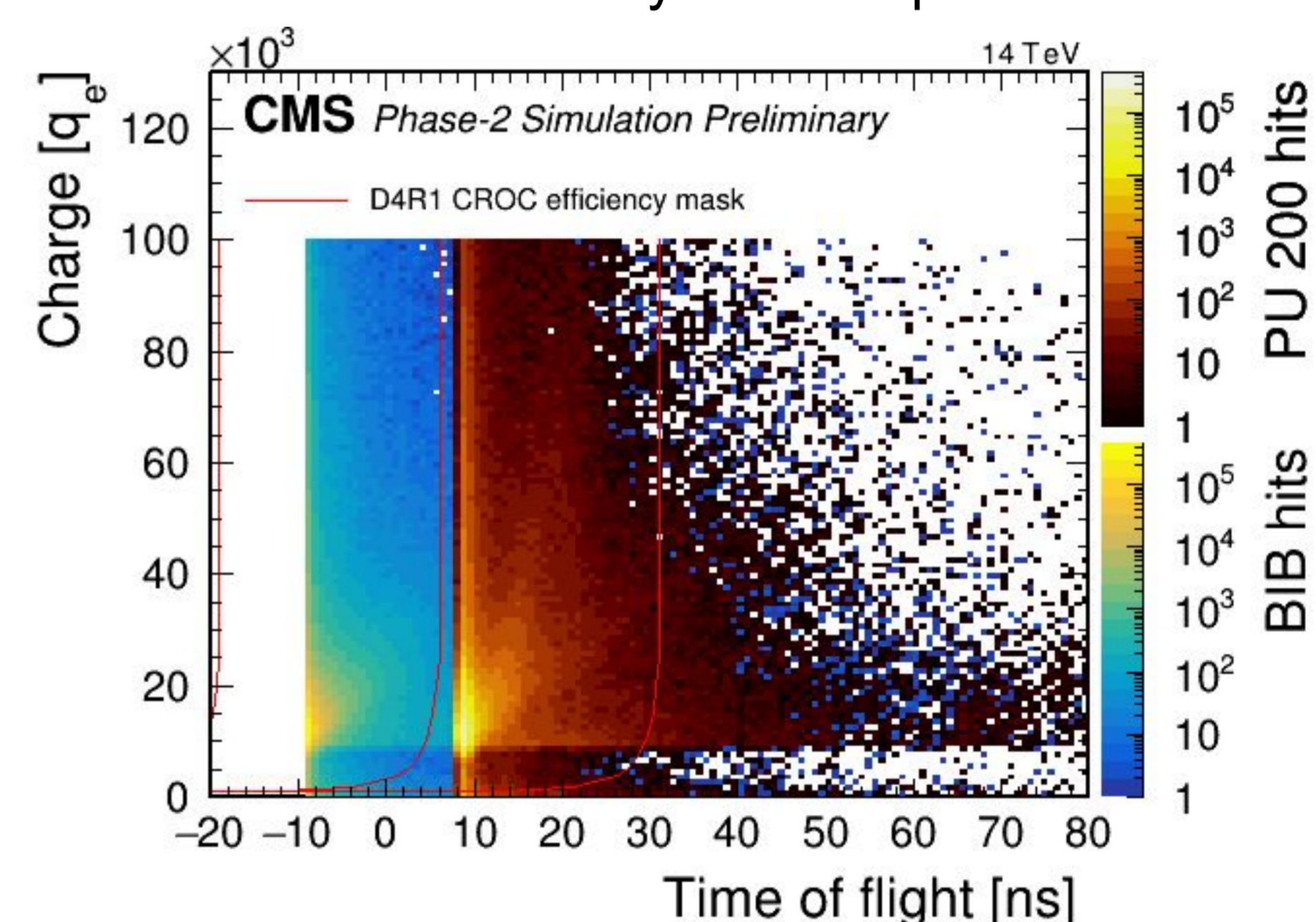
- Exploit the full available trigger rate (up to several MHz) and bandwidth, thus providing an excellent statistical precision (~1%)
- Provide measurements outside of stable beams, notably during energy ramps to measure BIB with a special clocking scheme
- Design and cable the detector such that all services, including the back-end are independent of the rest of TEPX

Baseline luminosity triggers:

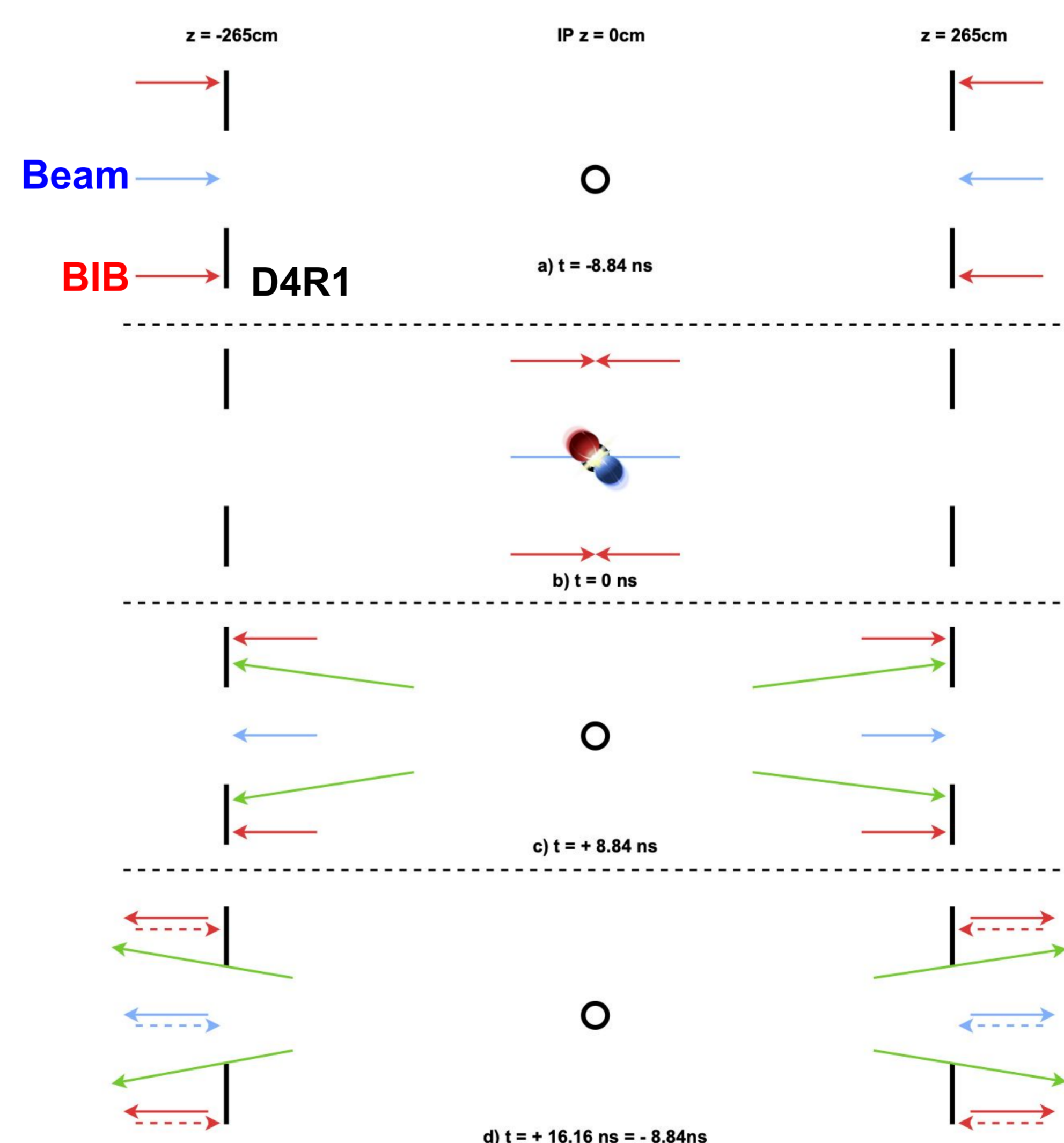
- Under nominal physics conditions: 825 (750+75) kHz trigger rate at pileup 200
- During Van der Meer scans: 2 MHz trigger rate at pileup 0.5

Measuring Beam-Induced Background with D4R1

D4R1 lies at an ideal location to measure luminosity from *outgoing collision products* and *incoming BIB* with a very good time separation of ~17 ns. The timing settings of the CROC front-end can therefore be configured such that the incoming BIB can be sampled in one clock cycle before the collision products, as shown in the figure below. The expected occupancy of BIB is nevertheless orders of magnitude lower than that caused by collision products.



When to sample? The plot shows the simulated time of flight versus deposited charge distribution for hits in D4R1 caused by BIB and pileup 200. The distribution is overlaid with the efficiency model of the front-end chip (red curves) for two consecutive clock-cycles: the one where the collision products are expected (right) and the previous one where the BIB is expected to be sampled. Maximum efficiency was estimated with the rising edge of optimal bunch clock being about 6 ns after the nominal collision time. The plot contains 1.04 million simulated BIB events (beam gas and beam halo) and 930 pileup 200 events that cause a similar number of hits. Since beam background events are much less intense, the different statistics help to visualise the time distribution.



Why incoming beam background? The sketch illustrates the measurement of beam-induced background with TEPX D4R1 at the beginning of the bunch train. The incoming bunch (blue) and beam background (red) traverse the D4R1 sensors at $t = -8.8$ ns (a) to collide at $t = 0$ ns (b) at the interaction region. The outgoing background and collision products (green) then traverse D4R1 again at $t = 8.8$ ns (c). Since the collision products are not very well localised in time (out-of-time pileup) and due to albedo, the incoming background arriving about 7.3 ns later with the next bunch at $t = 16.16$ ns (d) cannot be distinguished in the detector signal.