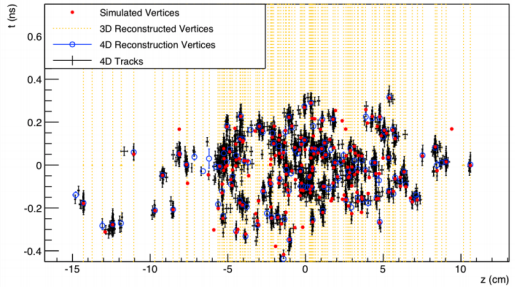
The CMS MTD Endcap Timing Layer: Precision Timing with Low Gain Avalanche Detectors

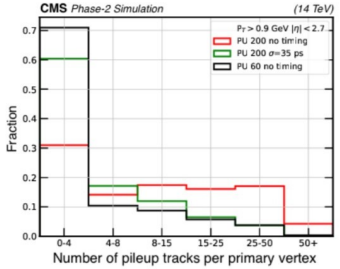
Chris McMahon (Boston University)
on behalf of the CMS Collaboration

Introduction

The unprecedented instantaneous and integrated luminosity provided by the HL-LHC will allow us to search for rare processes that will help us understand the nature of the Higgs boson and shed light on new physics. However, with the expected O(5000) charged particles produced per bunch crossing, efficient and robust track reconstruction will become extremely challenging.

- tracks coming from nearby vertices make it difficult to do object reconstruction and identification
- planned upgrades in tracker and other detectors will not be sufficient
- we need new detector capabilities: track timing information
  - collisions can happen at same position along the beam axis, but at different times

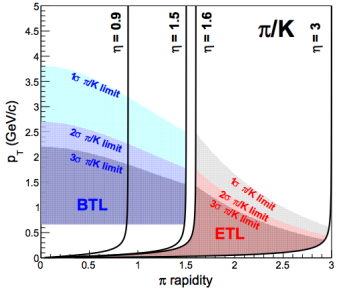


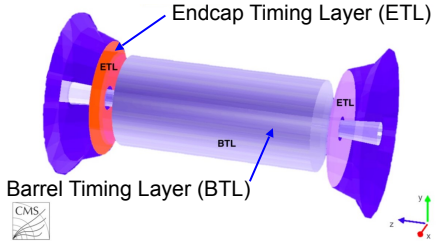


MIP Timing Detector

The Minimum Ionizing Particle (MIP) timing detector will be composed of two different detector technologies: the barrel ($\eta < 1.6$) uses LYSO bars with SiPM readout and the endcap ($1.6 < \eta < 3.0$) uses a silicon sensor with internal gain. MTD will improve reconstruction by:

- collecting timing information on charged particles
- combining tracking with timing
- track hits vary by an rms of 180-200 ps, so we need timing information more precise than that
  - with 40 ps precision, we can mitigate the effect of pileup from HL-LHC





Barrel covers low eta region, endcap covers $1.6 < \eta < 3.0$

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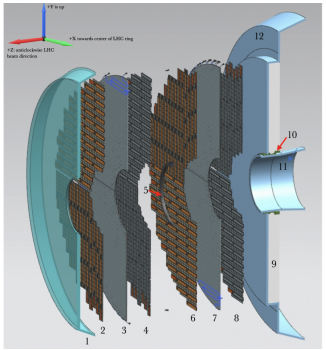
Endcap Timing Layer Design

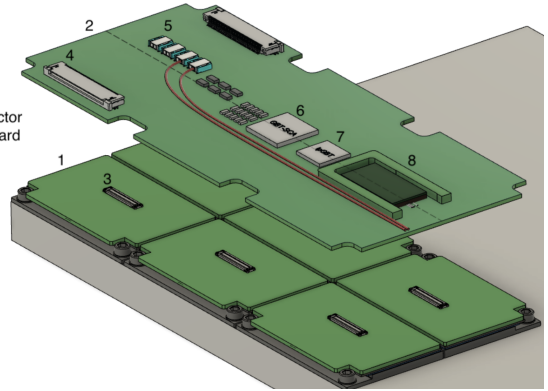
Disk design

- Two disks per endcap
- each disk covered in silicon sensors on each side
- disk separation of 20mm: average 1.7 hits per track
- modules serviced in groups of 3, 6, and 7 by service hybrids that are arranged around the disk to minimize dead areas on each disk



Service hybrid prototype

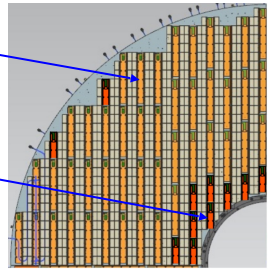
1: Flipped module
2: Readout board
3: Board-to-board connector
4: Connector to powerboard
5: BV connector
6: GBT-SCA
7: lpGBT
8: VTRx+



Service hybrid arrangement in disk

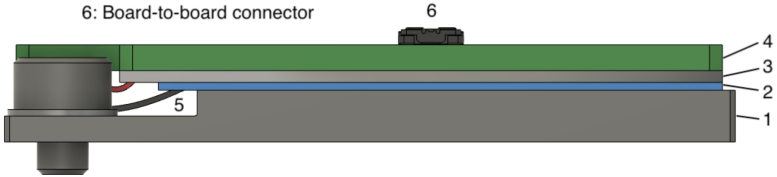
Full-sized: 12 modules

half-sized: 6 modules



Module prototype

1: Base plate (AIN)
2: LGAD
3: ETROC
4: PCB
5: Wire bonds
6: Board-to-board connector



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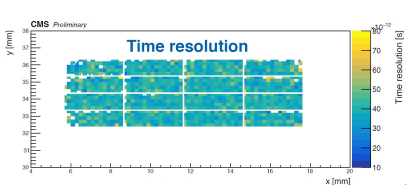
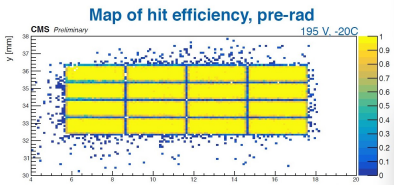
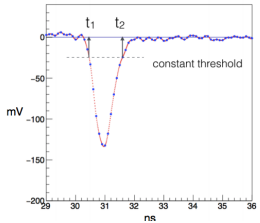
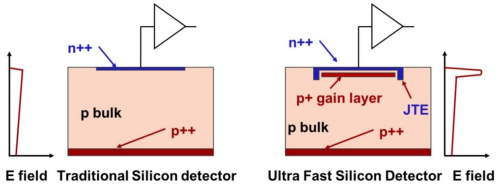
Low Gain Avalanche Detector (LGAD)

- ultra fast silicon avalanche detector
- thin gain layer to meet threshold for charge multiplication
- gain of 10-30
- only used in Endcap Timing Layer (ETL)
- Barrel Timing Layer (BTL) uses crystal scintillators with silicon photomultipliers instead.
- these are less radiation tolerant, but fit the BTL design and schedule better





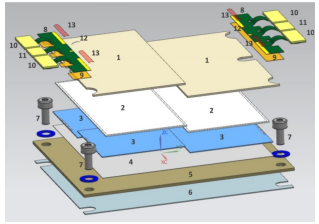




ETROC

- Endcap Timing Readout Chip
- one ETROC per 16x16 pixel LGAD sensor
- ~1600 per endcap
- reads charge deposits from LGADs and stores them in memory, along with timing information collected from an external clock
- multiple ETROCs are then connected to one service hybrid

Prototypes

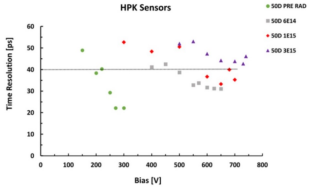


ETROC0: 1x1 (2018)
- beam test: ~30 ps resolution

ETROC1: 4x4 (2019)
- beam test: ~46 ps resolution

ETROC2: 16x16 (2021)
- still in development currently
- use ETROC emulator to prepare our test equipment for when development finishes

ETROC3: 16x16 (2022)
- final prototype using what we will learn from ETROC2



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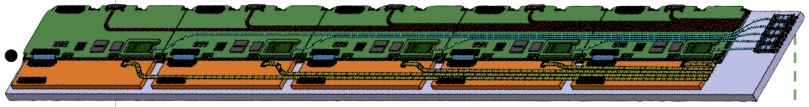
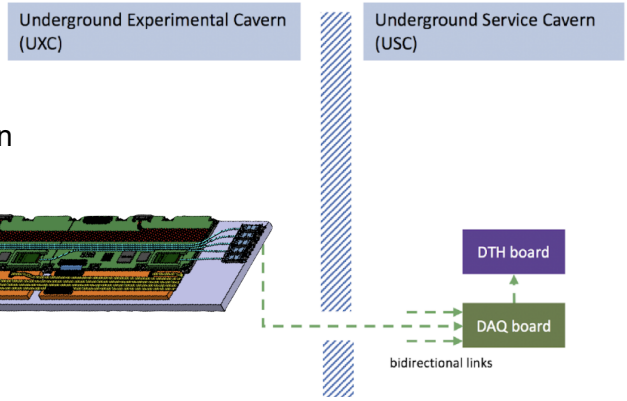
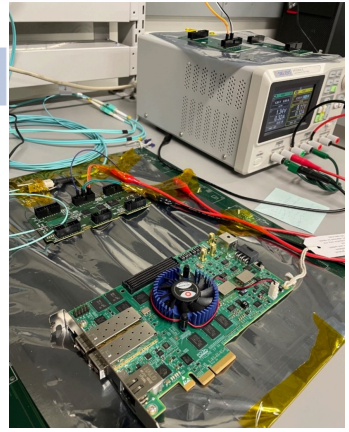
Testing data flow

- read hits and clock measurements on the detector
- package all the timing data through optical link on VTRx to the underground service cavern (USC)
- need to maintain radiation resistance in a fluence of up to 1.6x10^15 neq/cm^2





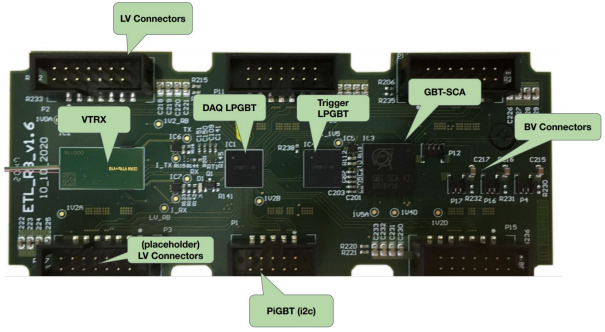
Boston test stand



Setup to help evaluate different module prototypes and developed module testing

- developments with ETROC2 emulator
- lay the ground work for future system testing

Readout Board



1-2 LPGBTs: Collect data from ETROCs
1 VTRX+

- versatile transceiver: sends collected hits & timing data through an optical link
- also receives clock information, which is distributed to ETROCs

1 GBT-SCA

- slow control system for LPGBT & ETROC
- manages bias voltages, monitors temperature

Summary

- High-Luminosity LHC will provide new insights into BSM physics
- MIP timing detector with 40 ps precision will help maintain our current reconstruction effieciency
- Module prototyping and preliminary system tests beginning at BU