The ATLAS Level-1 Calorimeter Trigger Upgrade

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HighRR BiWeekly

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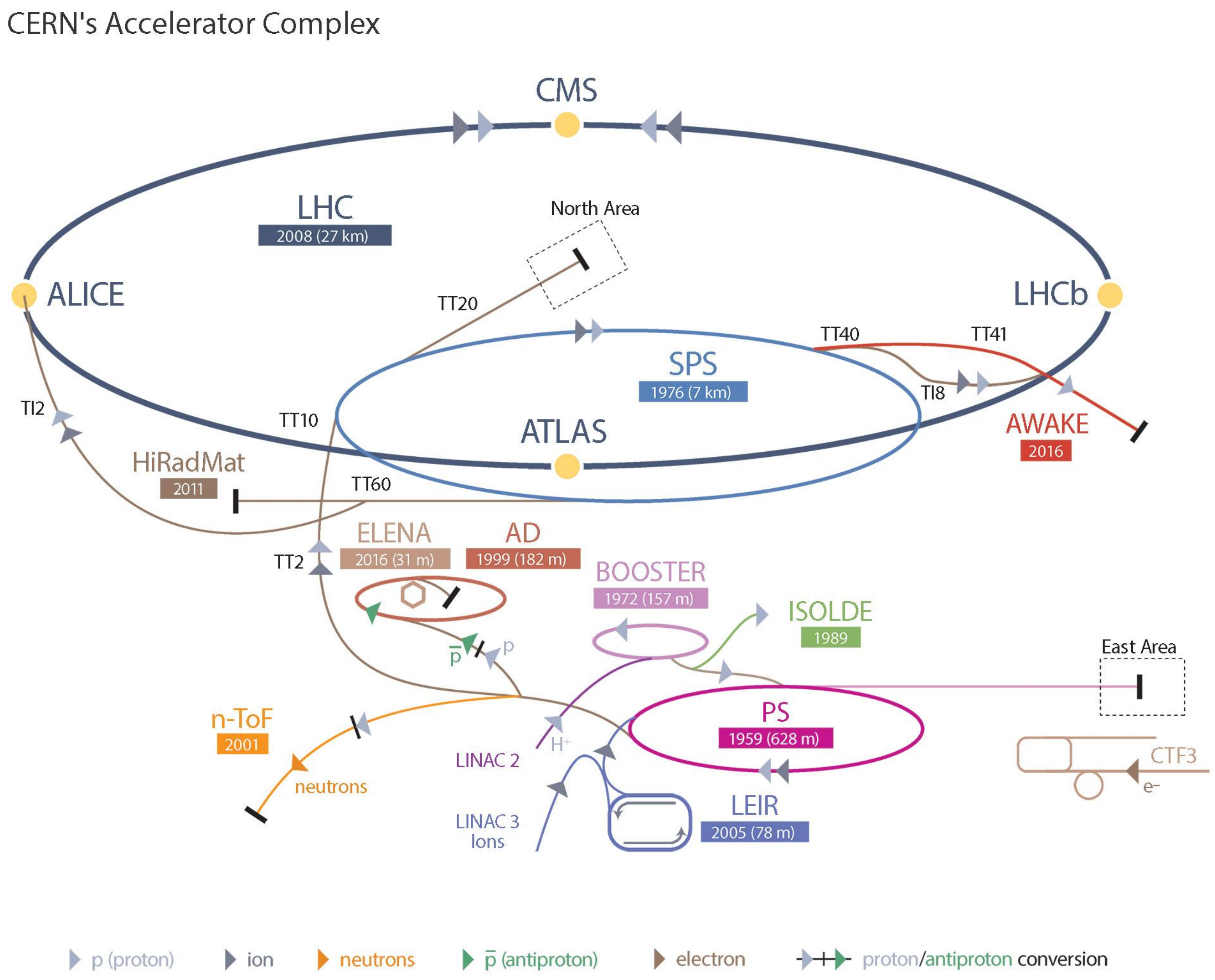
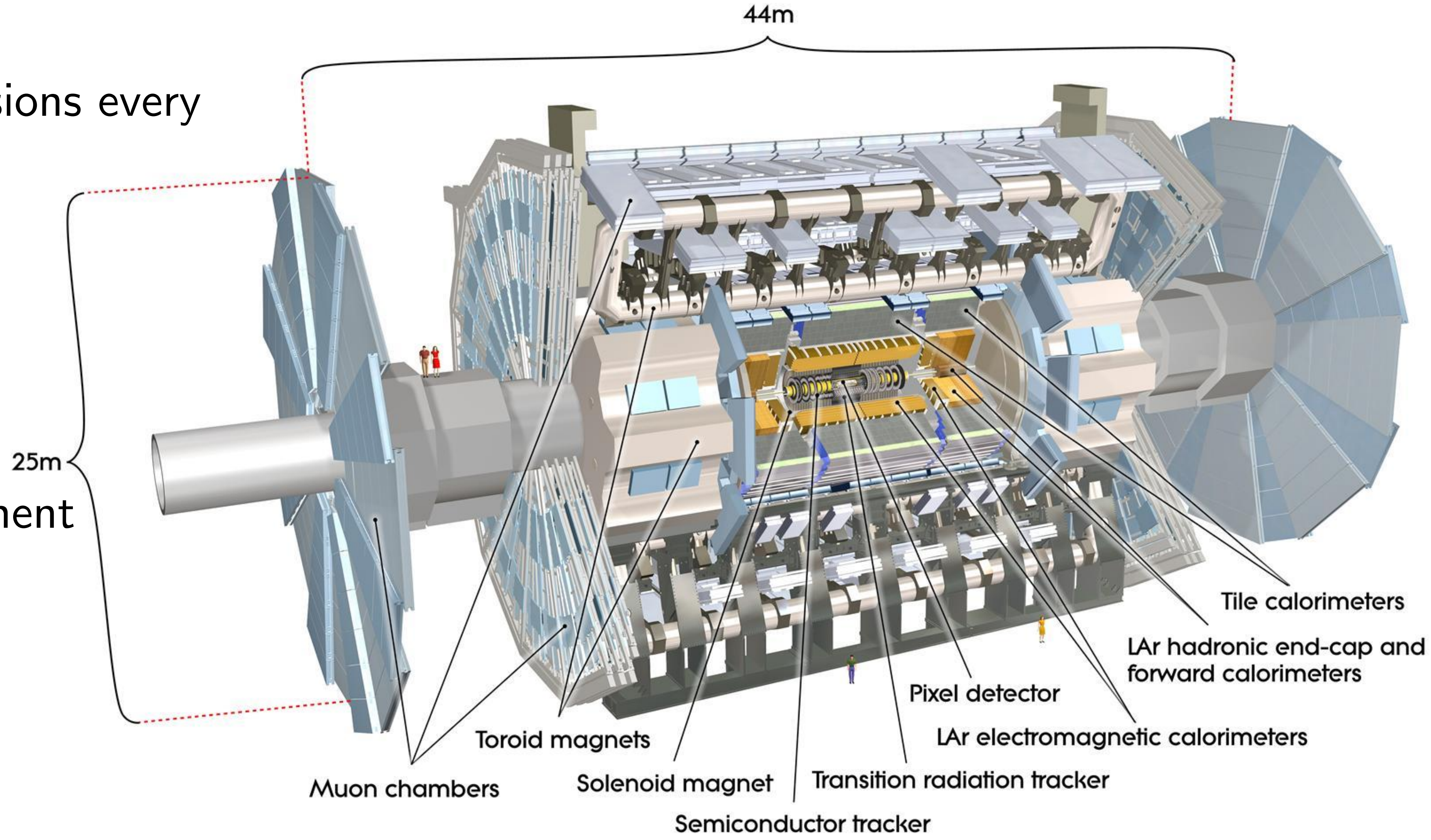
The ATLAS detector at the LHC



The ATLAS detector

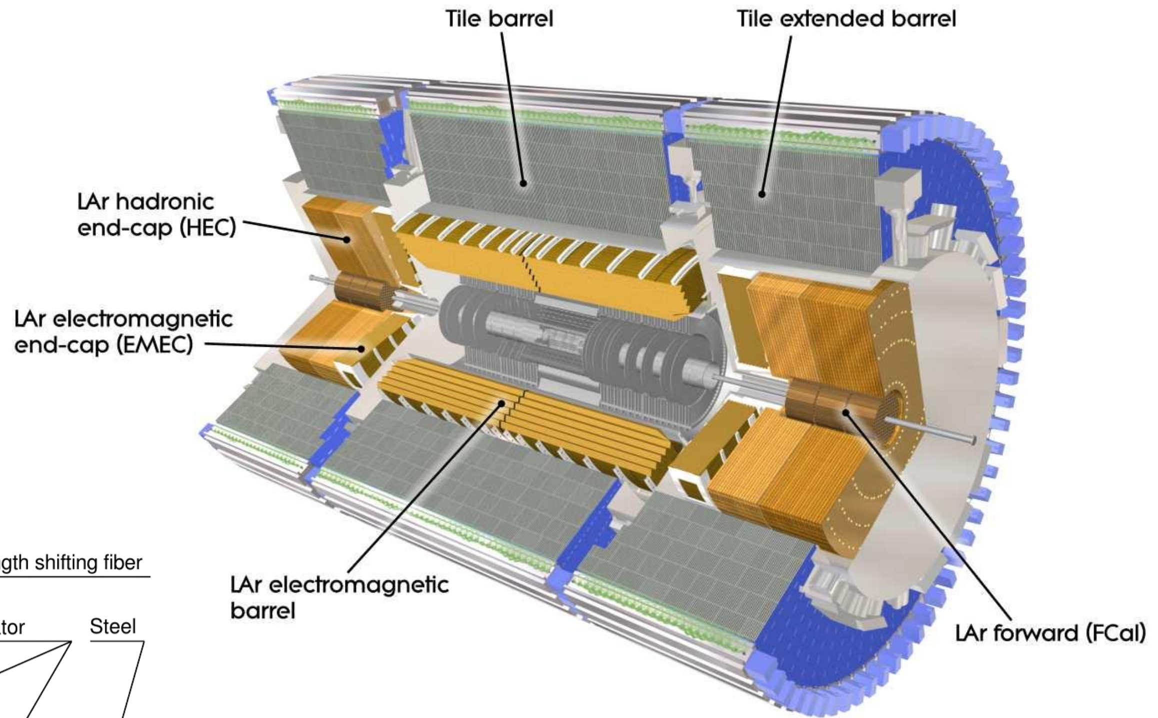
- **A T**orodia**l L**HC **A**pparatu**S**
  - 7000 tons
- $\sqrt{s} = 13$ TeV pp collisions every 25 ns



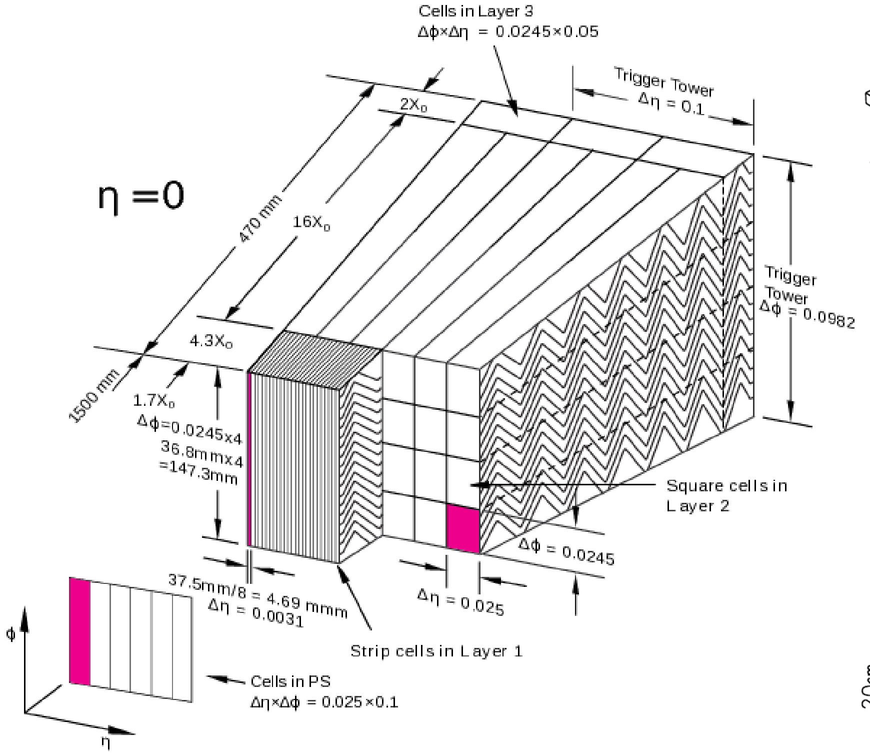
- Multi-purpose experiment
- Higgs Physics
- BSM searches
- SM measurements
- SUSY

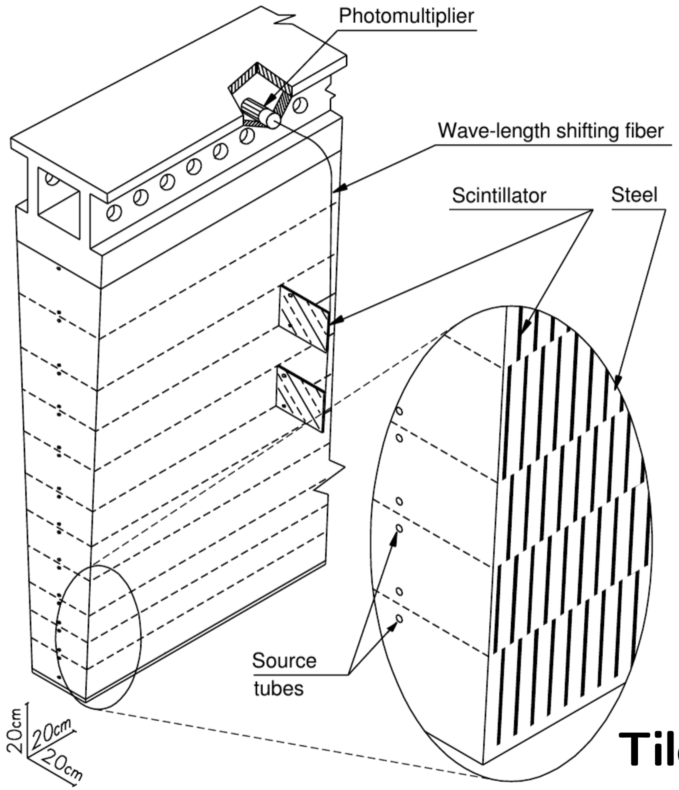
ATLAS Calorimeters

- **Sampling calorimeters**
- **LAr: lead and liquid argon**
- **Tile: steel and plastic scintillators**

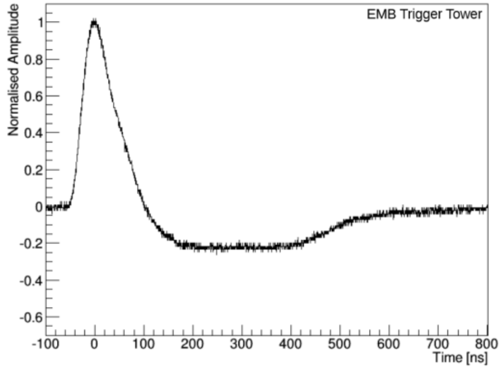


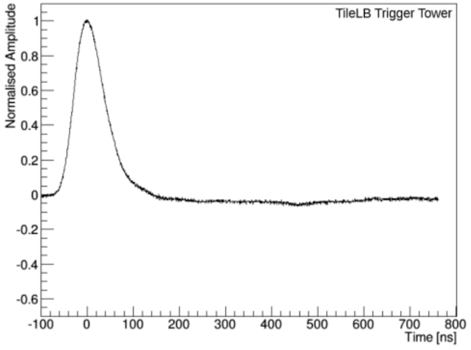
Liquid Argon (LAr)





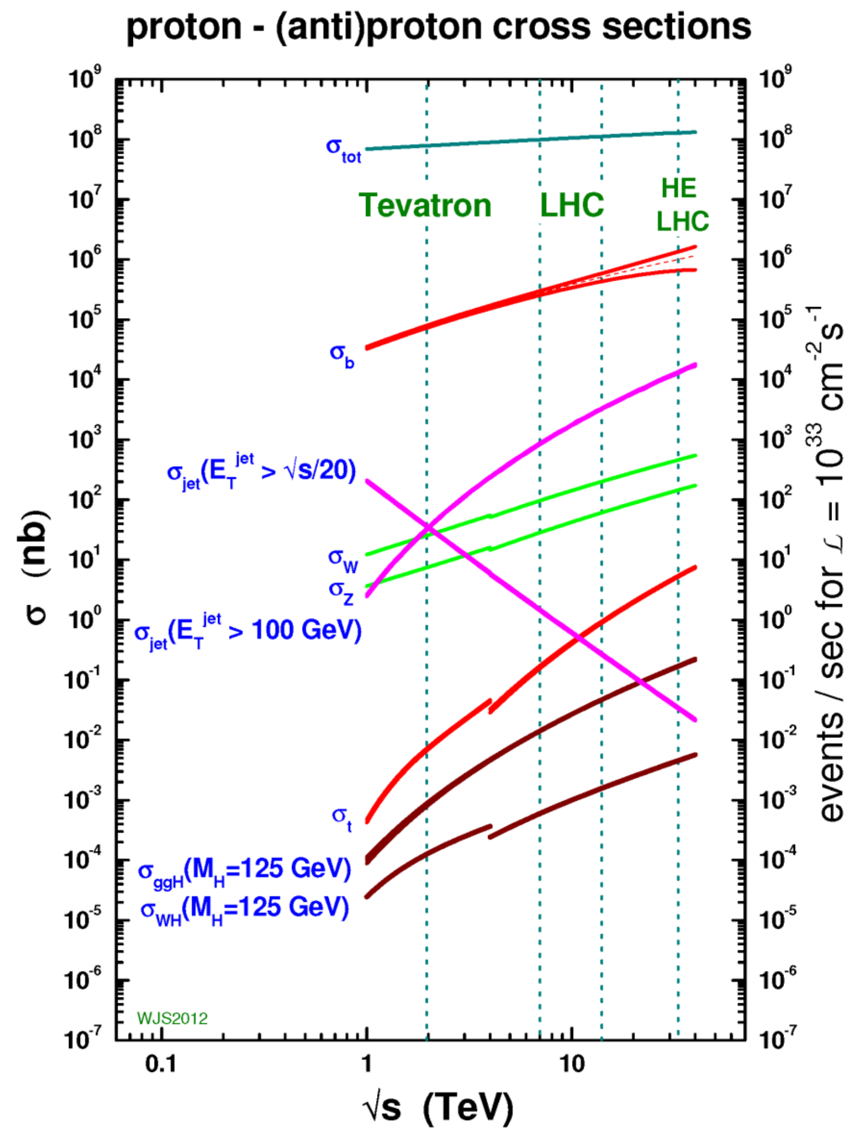
Tile Calorimeter





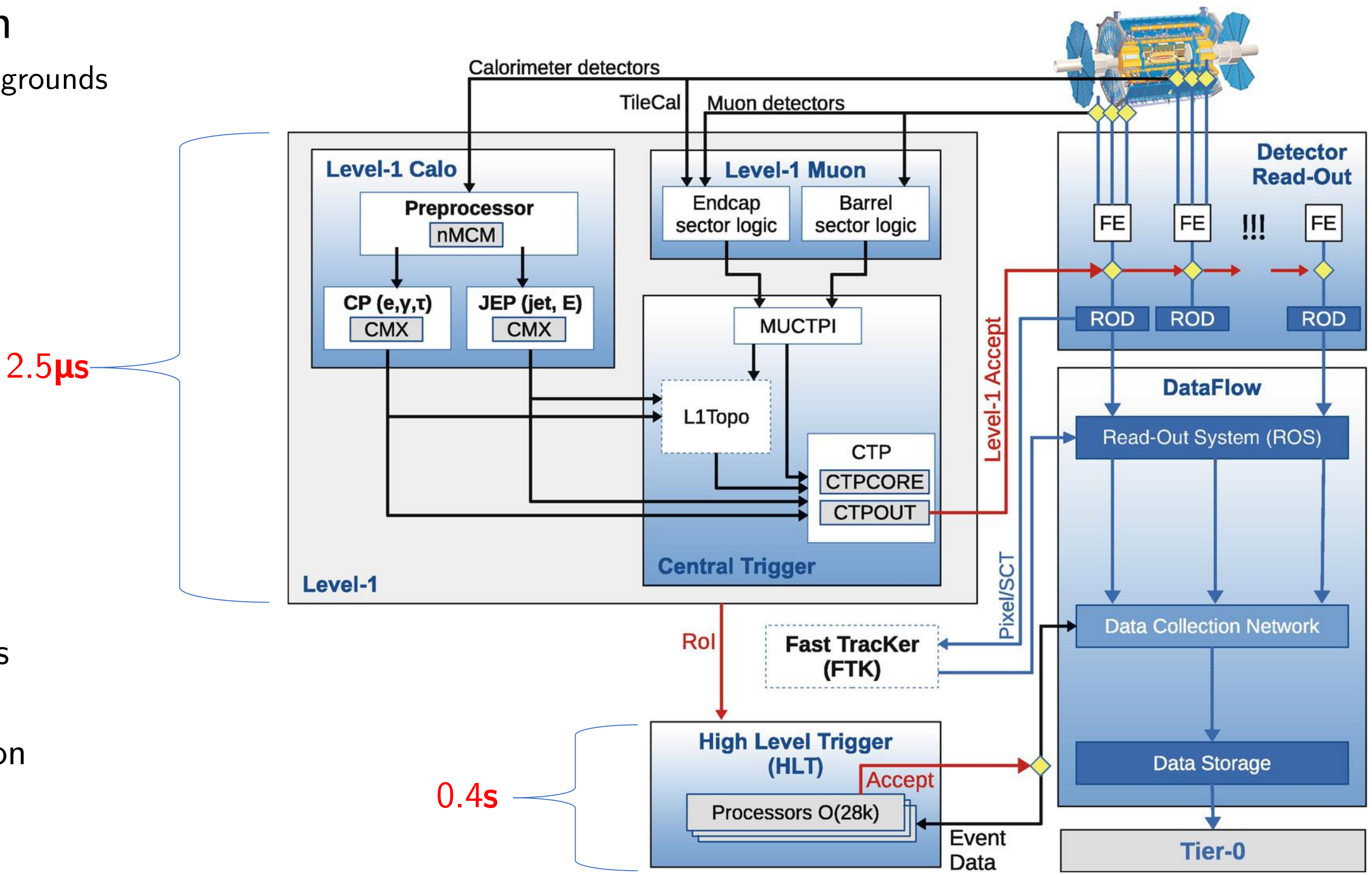
Trigger

- Very high rates at nominal LHC luminosities!
- A full ATLAS event size ~ 1.5 MB/event
- At 40 MHz pp collisions ~ **40 TB/s** of data
- Need **reduction** of the rate!
- Select and store only "interesting" events
- Need a decision in real-time
- High efficiency



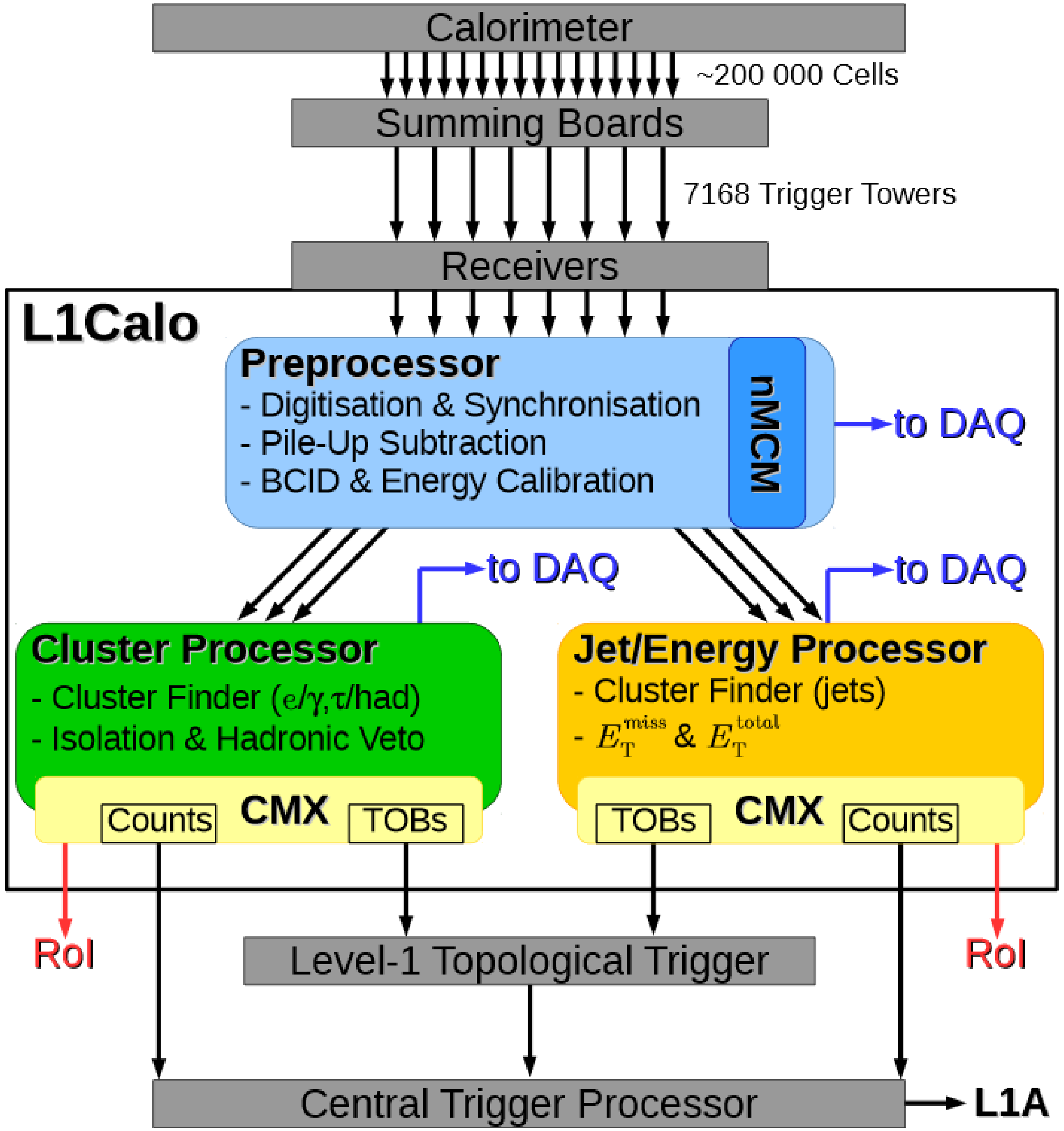
Trigger and DAQ

- Multi-Level trigger system
  - Rapid rejection of high rate backgrounds
- First level trigger (L1):
  - Custom electronics
  - Strict latency budget
  - Reduced granularity
  - No tracking information
  - EM scale
  - ~ **100** kHz accepted events
  - RoI data seeded to the HLT
- Second level trigger (HLT):
  - High performance PC clusters
  - More complete analysis
  - Full event tracking information
  - ~ **1.5** kHz accepted events



Level-1 Calorimeter Trigger

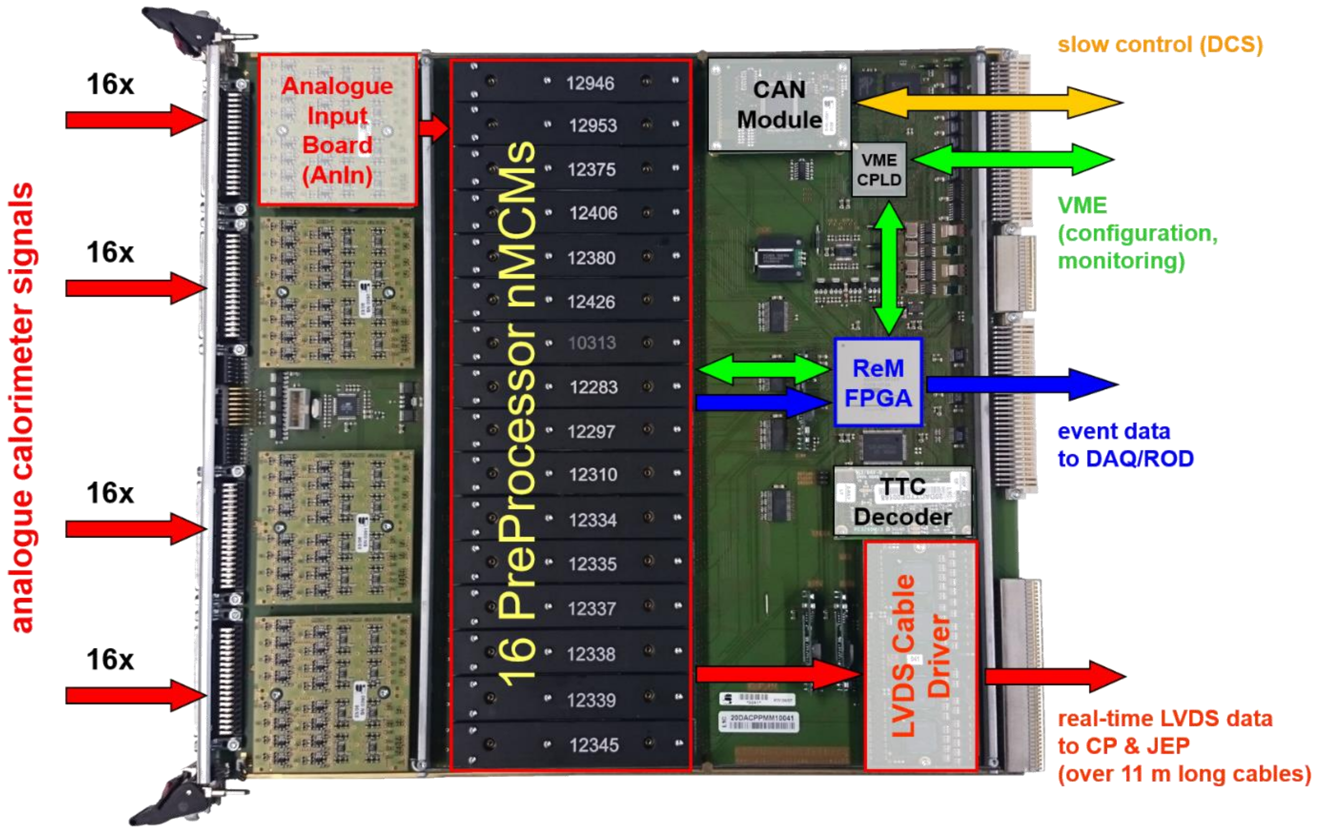
- Search signatures:
  - High E_T electrons and photons
  - High E_T taus and jets
  - Missing E_T
- Coarse analog trigger-towers
- Granularity of mainly 0.1 x 0.1 (Δη x Δφ)
- Bunch-crossing identification
- Object identification
- Pipelined event data readout at ~100 kHz
- Results delivered to the the CTP in real-time ~2.5 µs

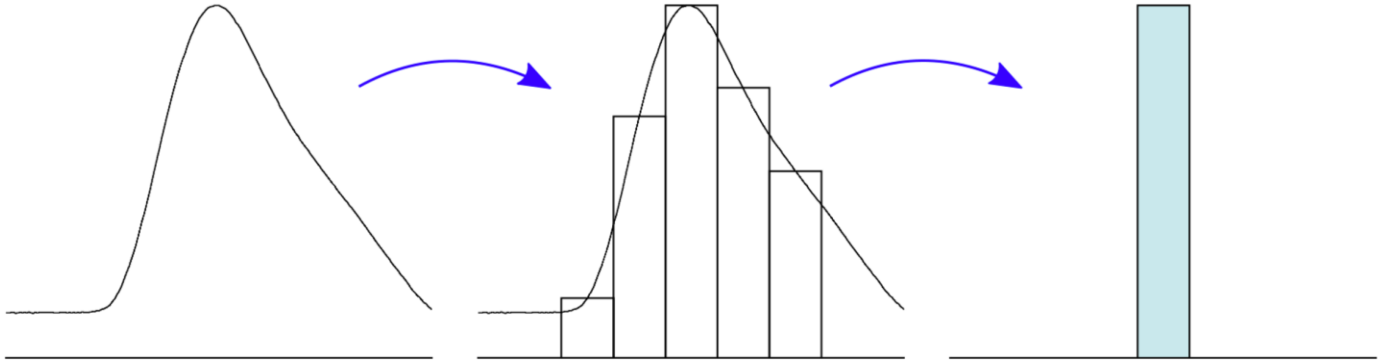


Level-1 Calorimeter PreProcessor

PreProcessor system

- Operated in Run2 and beyond
- Consists of 124 identical PreProcessor Modules (PPMs)
- 16 Multi-Chip Modules(nMCMs) on each PPM:
  - 4 analog calorimeter signal inputs
  - 10-bit dual channel FADCS at 80 MHz
- Digitization and synchronization
- Filtering and peak-finding
- Calibration to EM scale (GeVs)

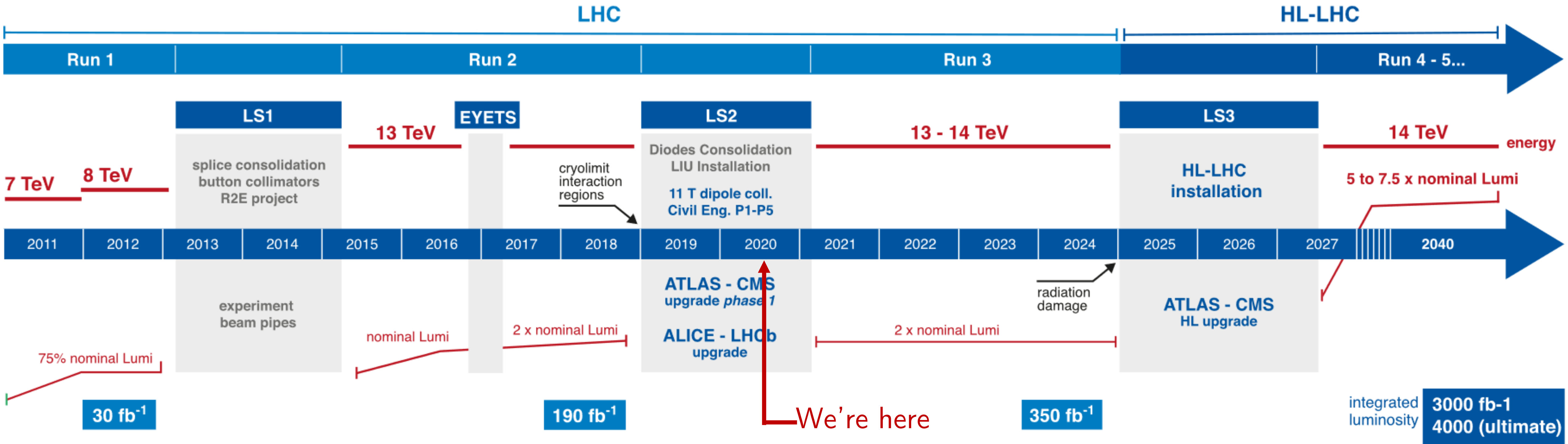




Phase-I Upgrade

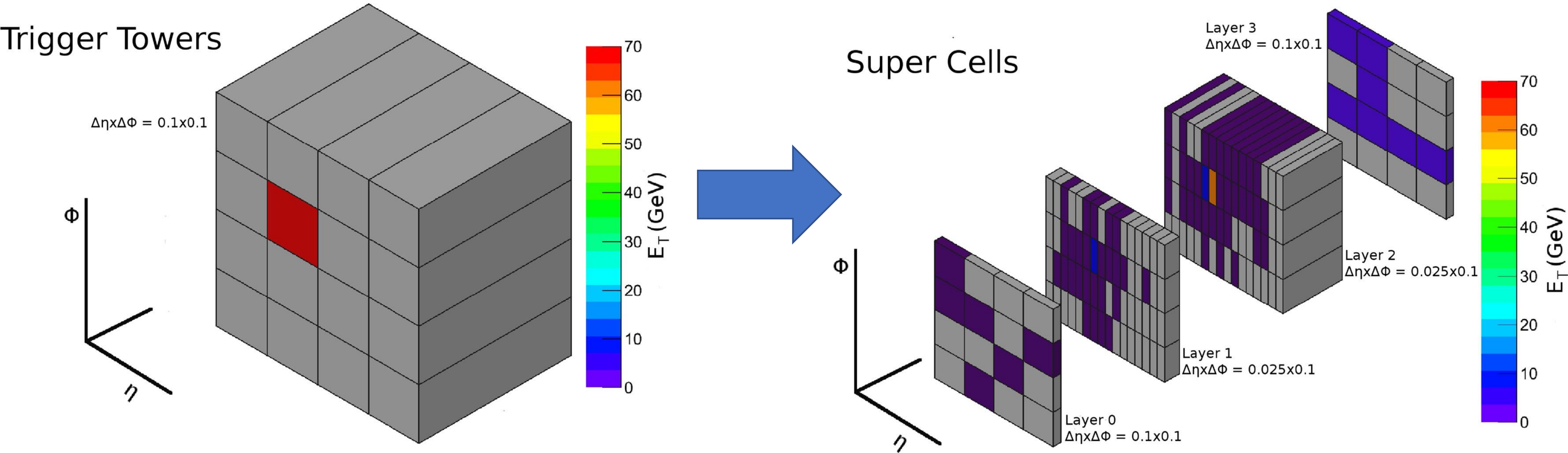
- Run 2:
  - L = 2 x 10^{34} $cm^{-2}s^{-1}$
  - Interaction per BC: $<\mu> = \sim 40$
- Run 3:
  - Match Run2 peak luminosity during start
  - L = 2 - 3 x 10^{34} $cm^{-2}s^{-1}$
  - Harsher pileup conditions $< \mu > = \tilde{}60 - 80$
  - Higher event rates

- New Small Wheel, RPCs
- New calorimeter and trigger electronics
- Multithreading in offline/online software

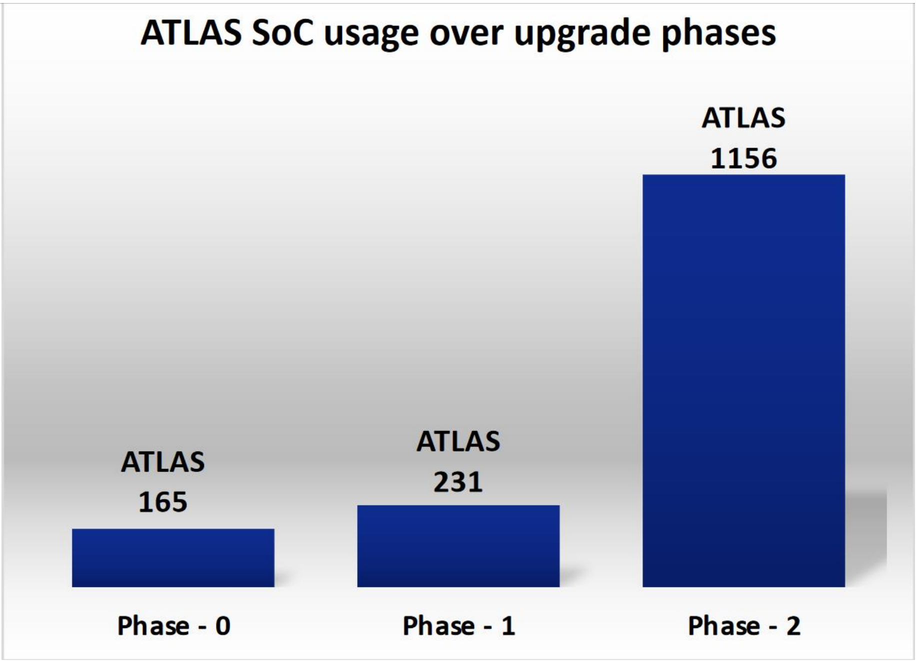


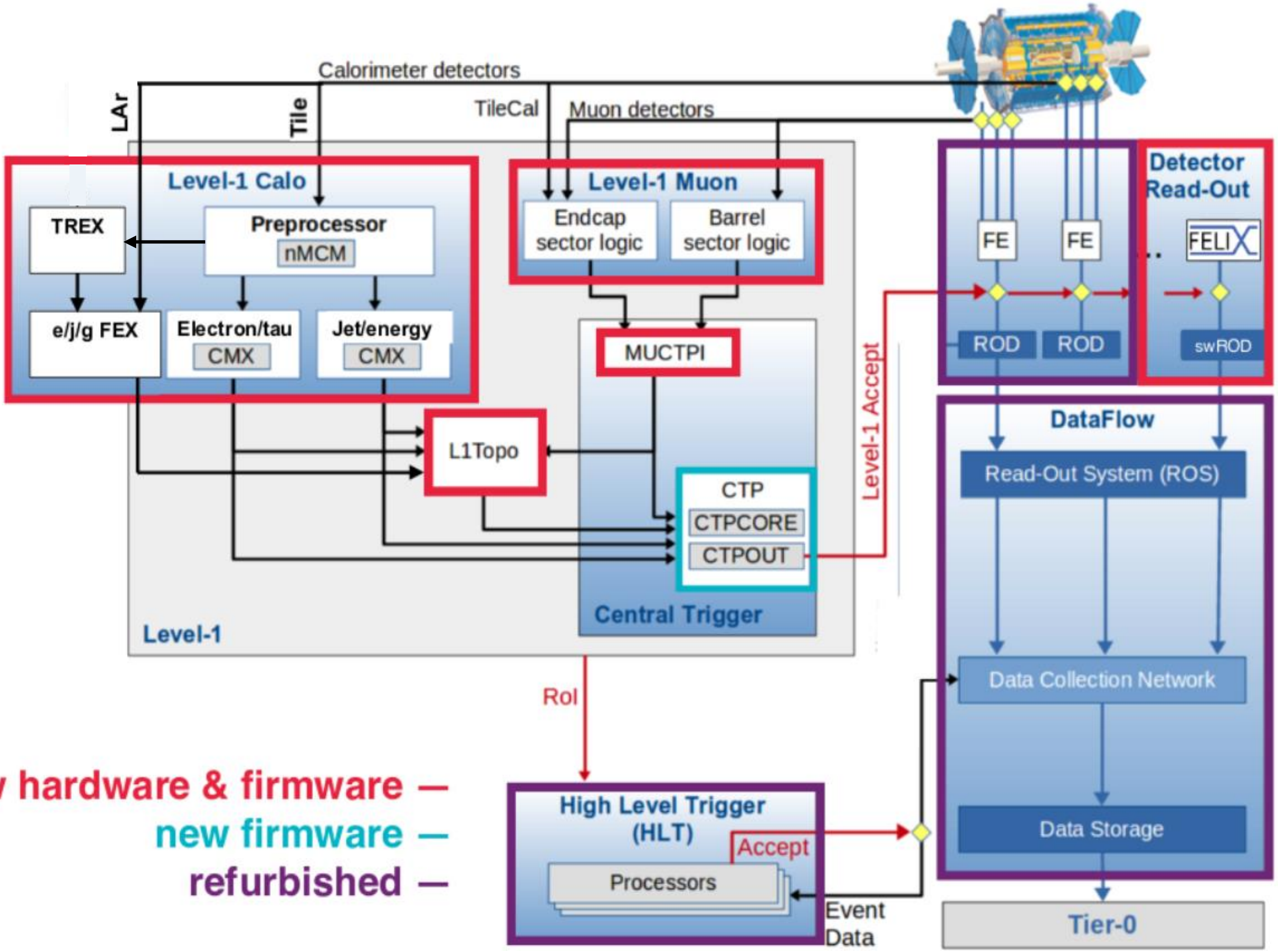
Phase-I LAr Upgrade

- **New calorimeter trigger electronics**
  - 10x granularity increase per trigger-tower
  - Finer segmentation
  - Higher resolution and increased shower information



Trigger and DAQ in Run 3



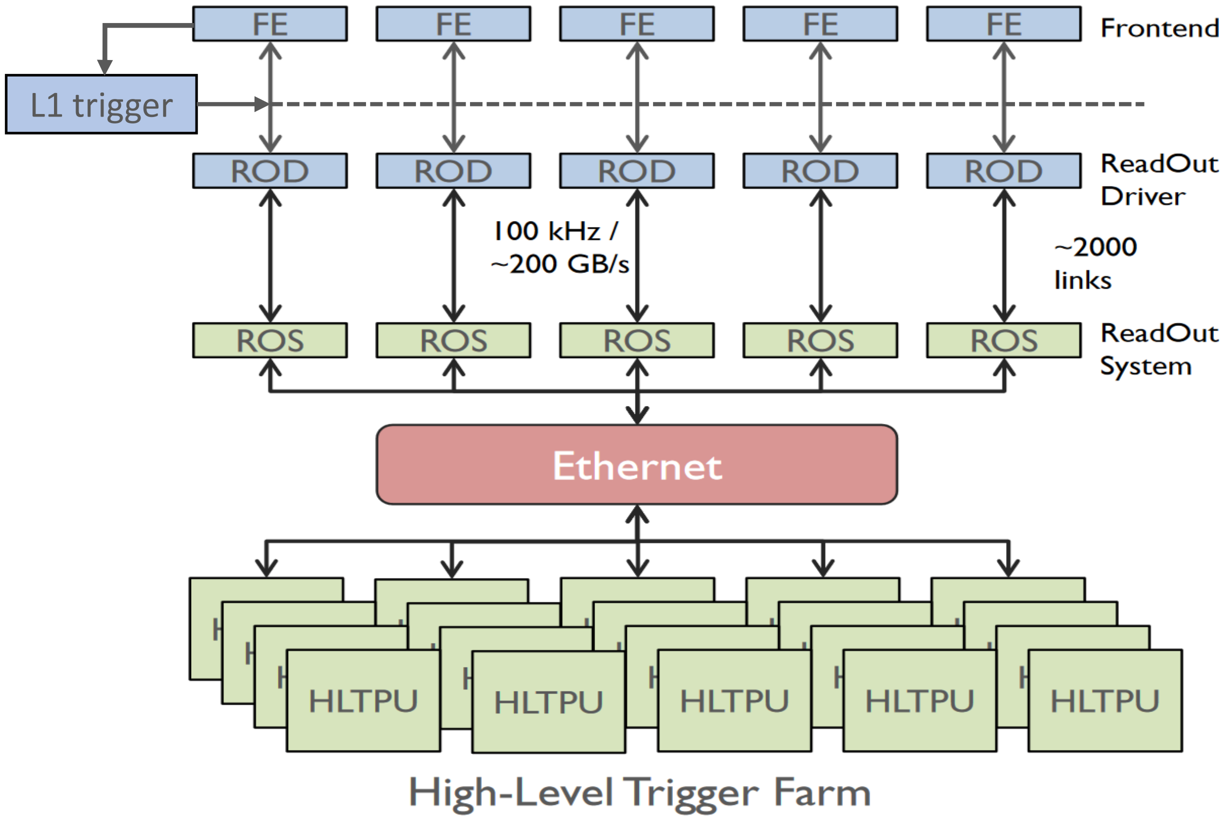


new hardware & firmware —
new firmware —
refurbished —

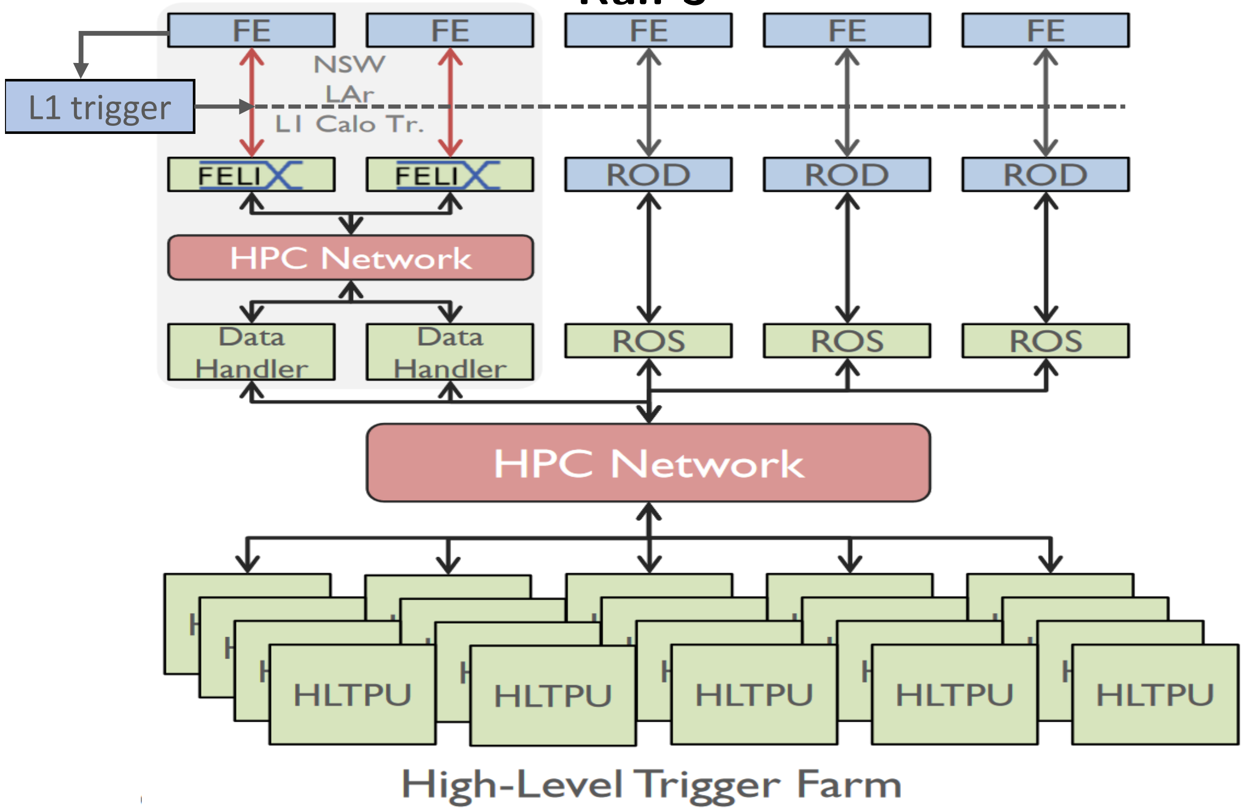
DAQ Upgrade

- New readout platform
- Front-End Link eXchange (FELIX)
- Based on commercially available components
- Routed L1 Trigger clock and control signals
- Direct connection to trigger hardware
- Interfaces with GBT(4.8 Gbps) and FULL(9.6Gbps) mode protocols

Run 2



Run 3



L1Calo Upgrade

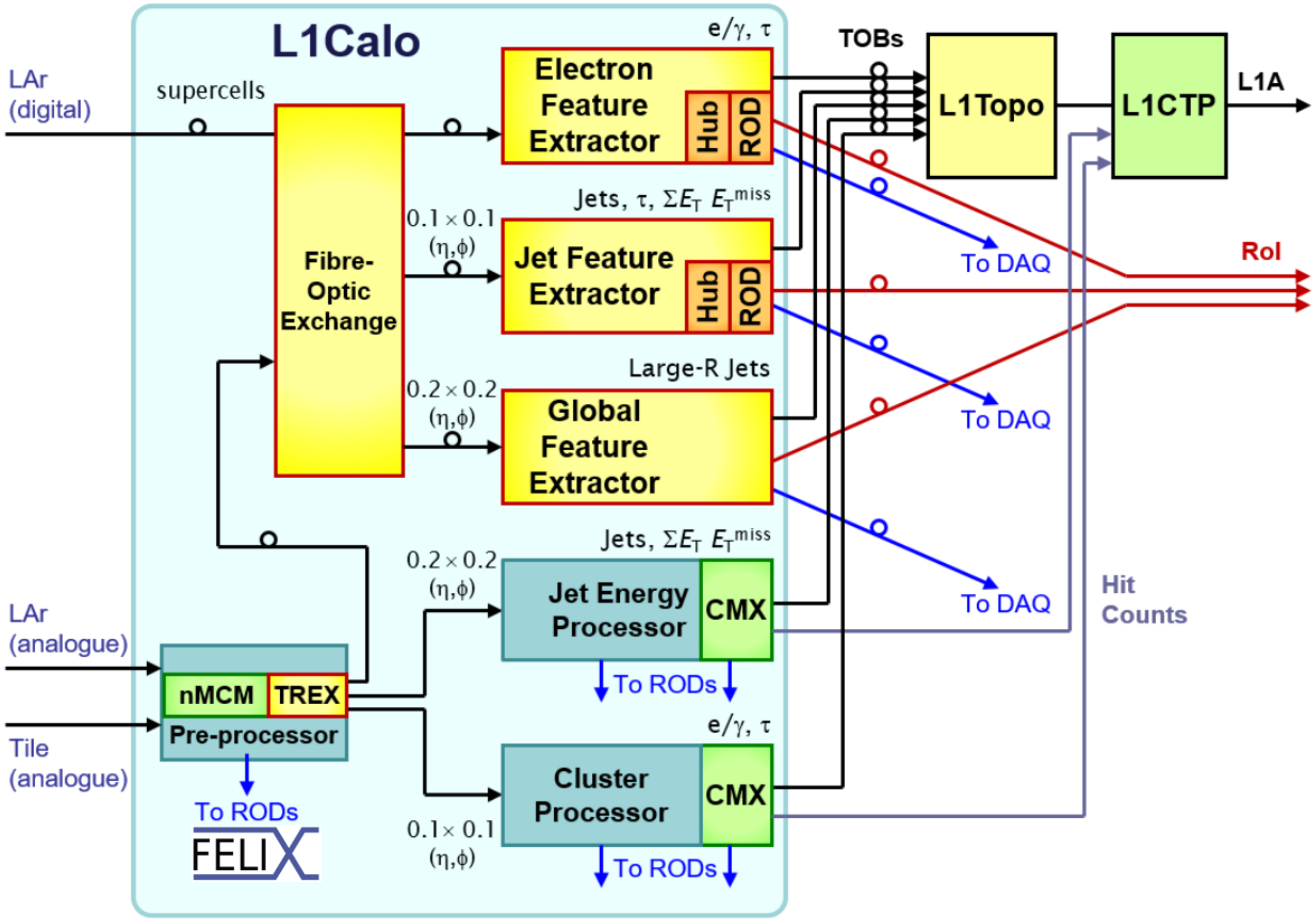
- Increased robustness against pile-up
- Better isolation performance
- Maintaining low trigger thresholds
- High efficiency

- Super-cell digital input from Lar
- Analog trigger-towers from Tile

- Feature extractors:
  - Electron
  - Jet
  - Global

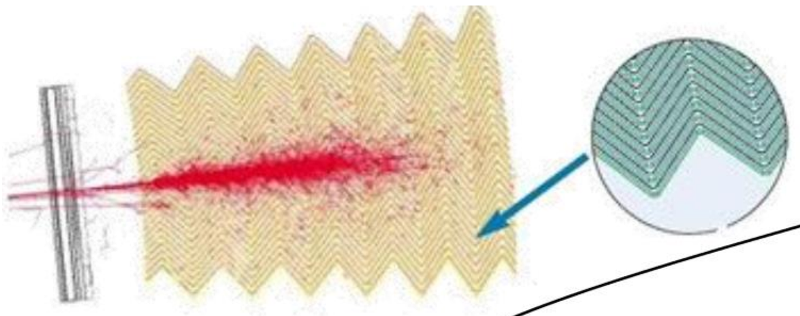
- PreProcessor system with the Tile Rear Extension modules

- Run in parallel with Run 2 system

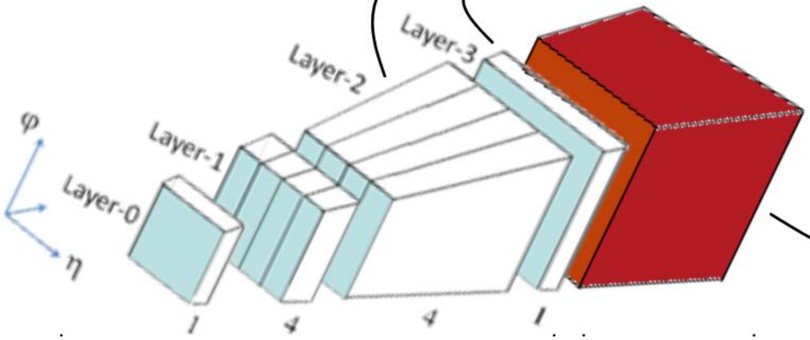


eFEX

- Identification of e/γ and τ candidates
- Using shower-shape and isolation to find e/γ from jet background
- Receives fine granularity data from LAr 0.025 x 0.1 (Δη x Δφ)



EM shower in LAr

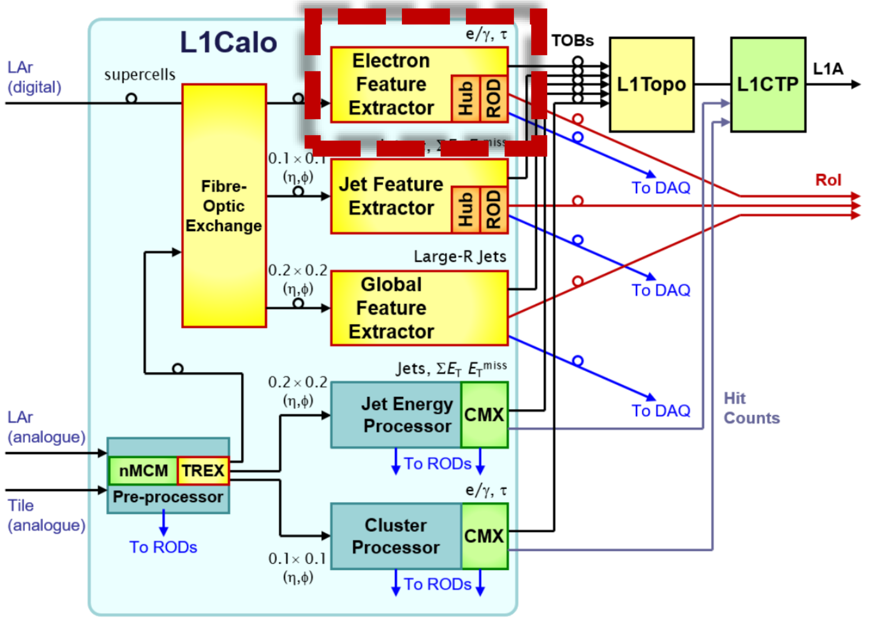


$$w_s{}^2 = \frac{\sum E_i (i - i_{max})^2}{\sum E_i}$$

$$R_\eta = \frac{E_{clu}}{E_{env} + Eclu}$$

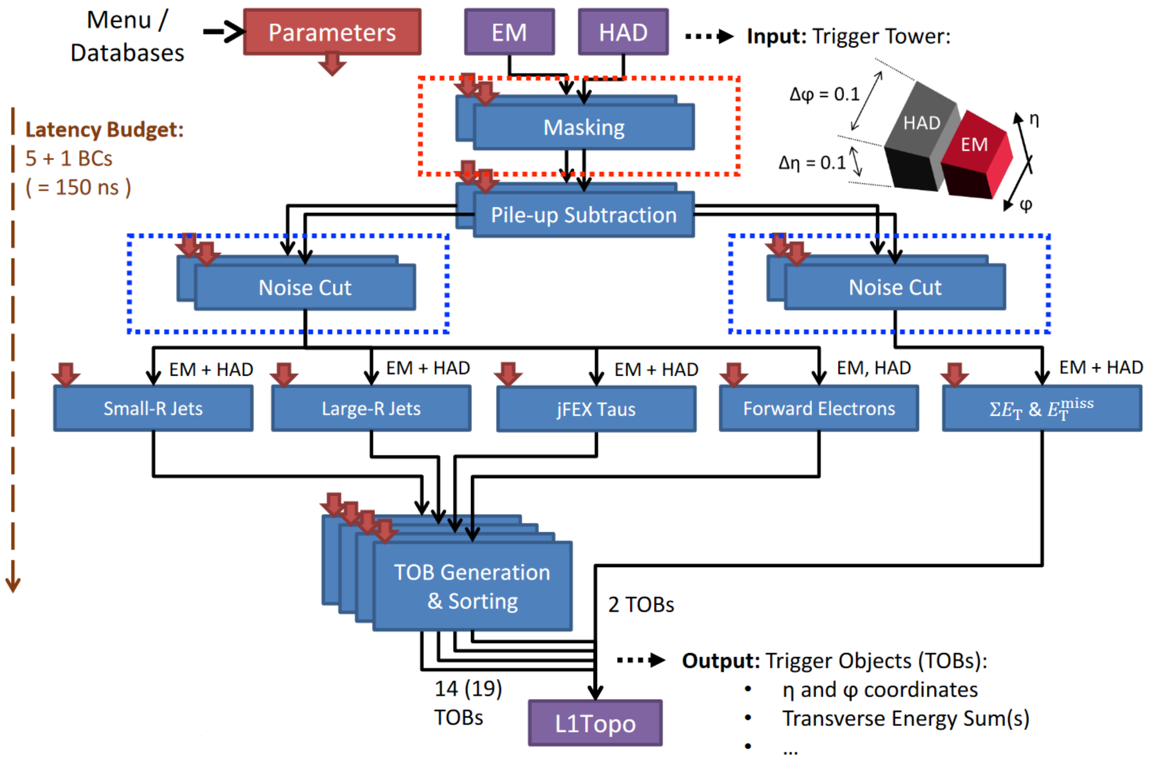
$$f_3 = \frac{E_{L3}}{E_{Tot}}$$

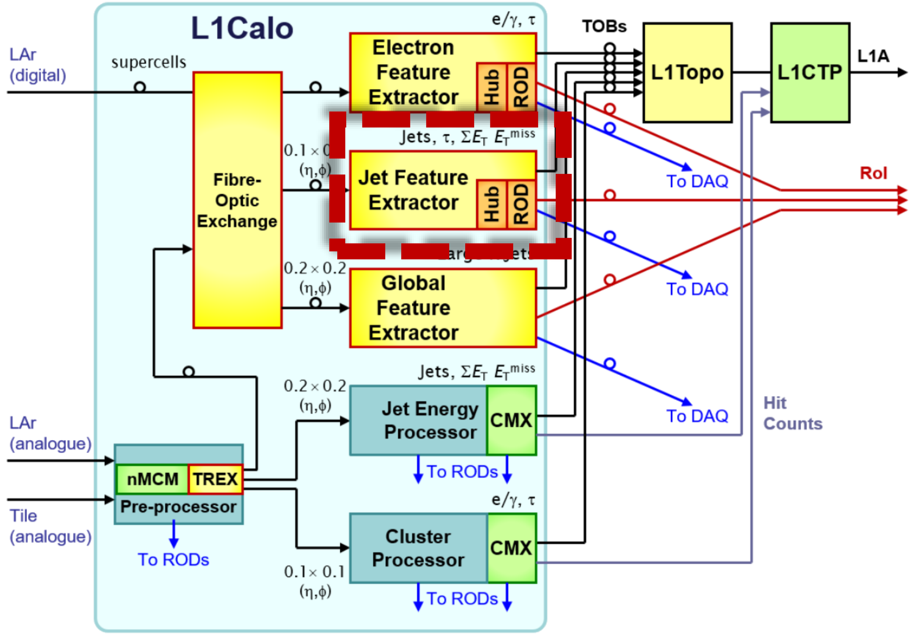
$$R_{Had} = \frac{E_{Had}}{E_{Tot}}$$

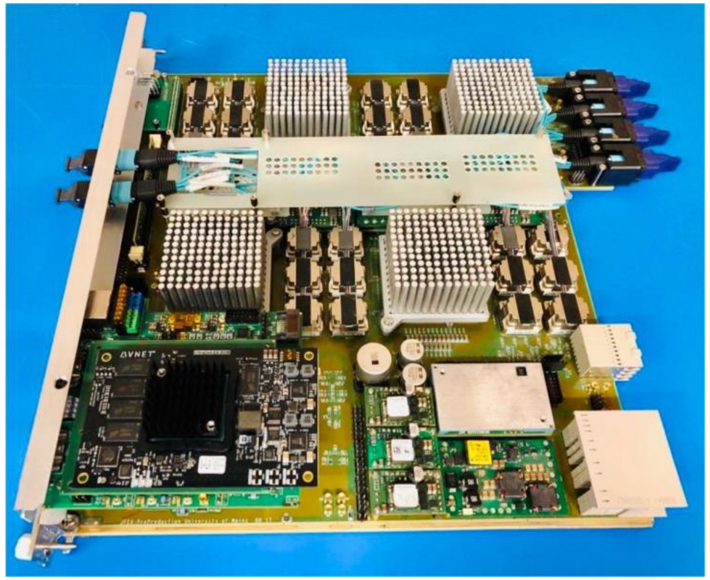


jFEX

- Identification of jets and large area τ particles
- Calculation of global variables:
  - Total transverse energy $\sum E_T$
  - Missing transverse energy E_T^{miss}
- Granularity 0.1 x 0.1 ($\Delta\eta \times \Delta\varphi$)
- Covers $|\eta| < 4.9$ range

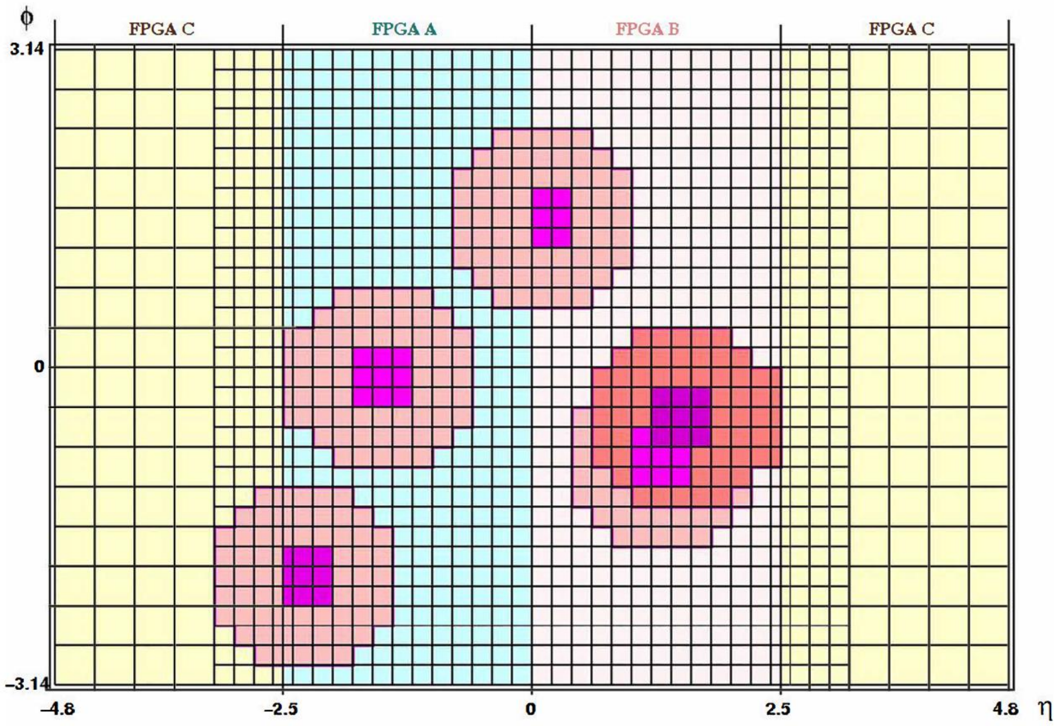


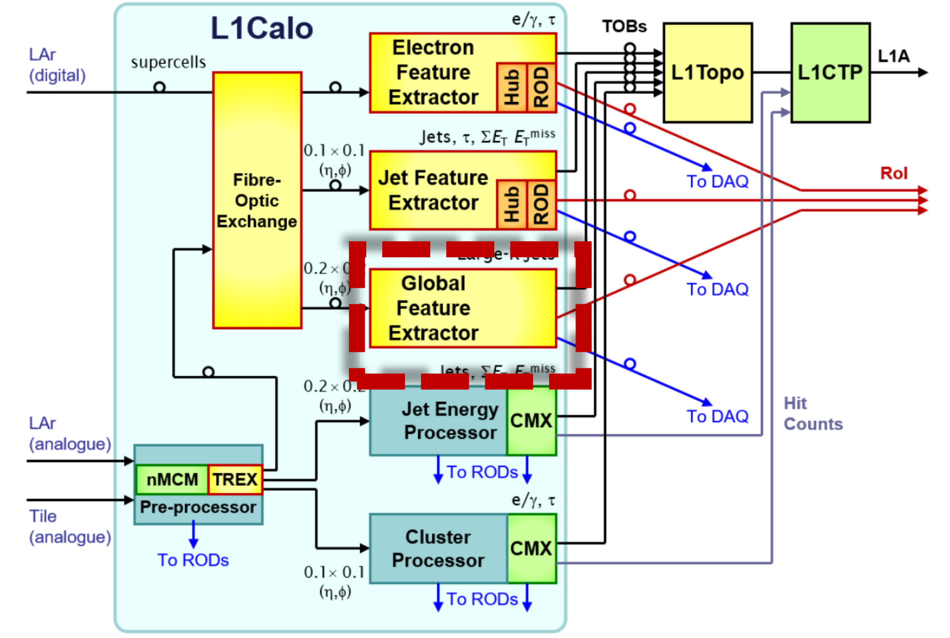


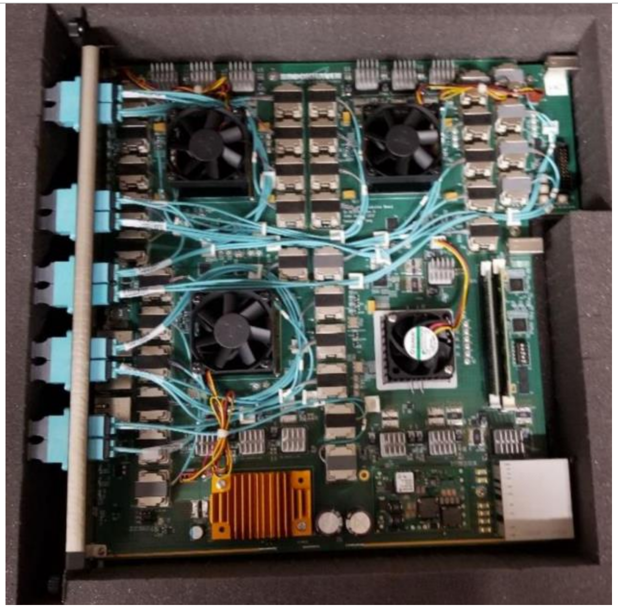


gFEX

- Identification of large-radius jets
- Analysis of event-level features
  - E_T^{miss}, fat jets
- 0.2 x 0.2 (Δη x Δφ) tower-sum data as input
- Entire calorimeter data on a single module

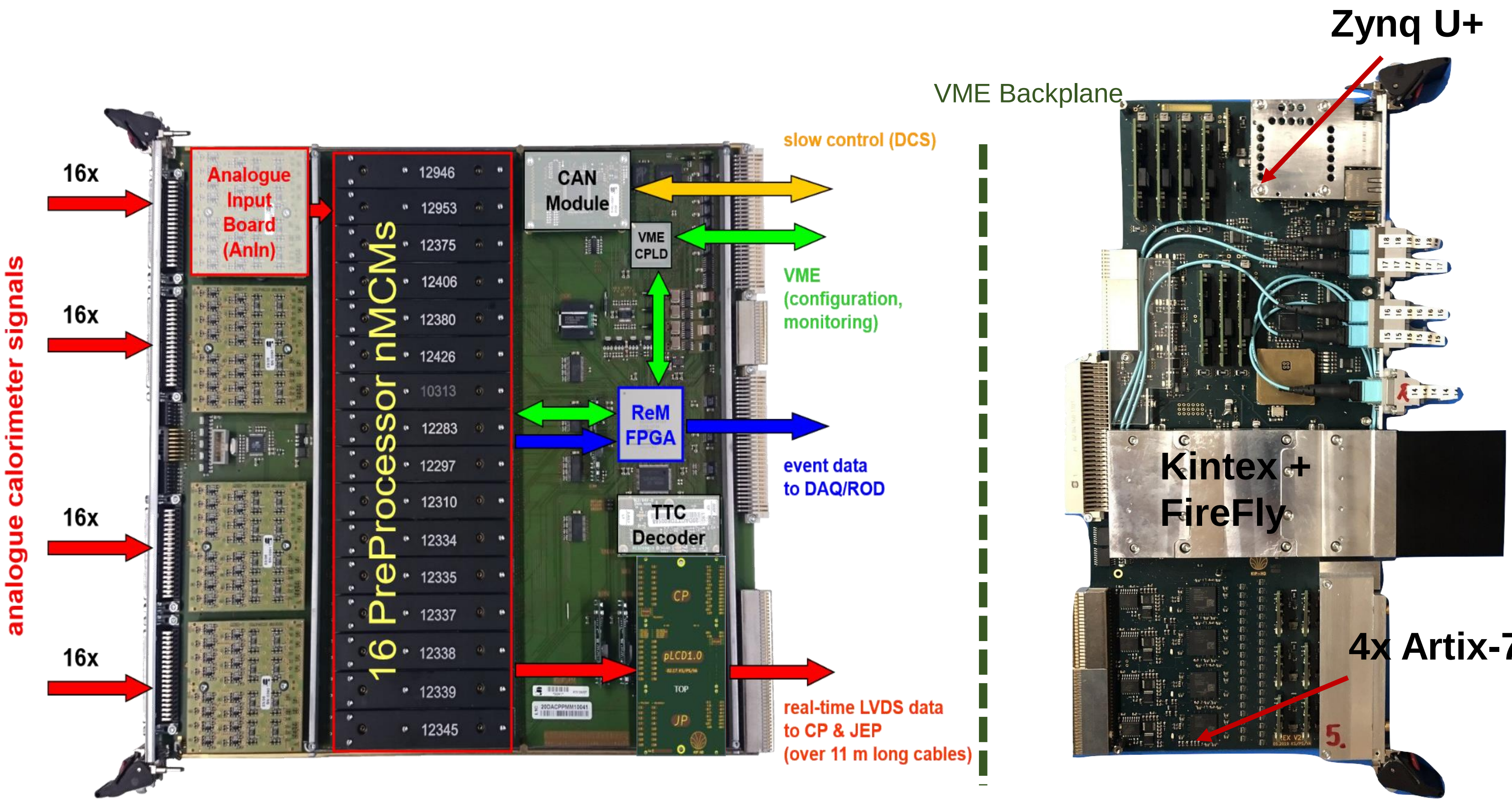






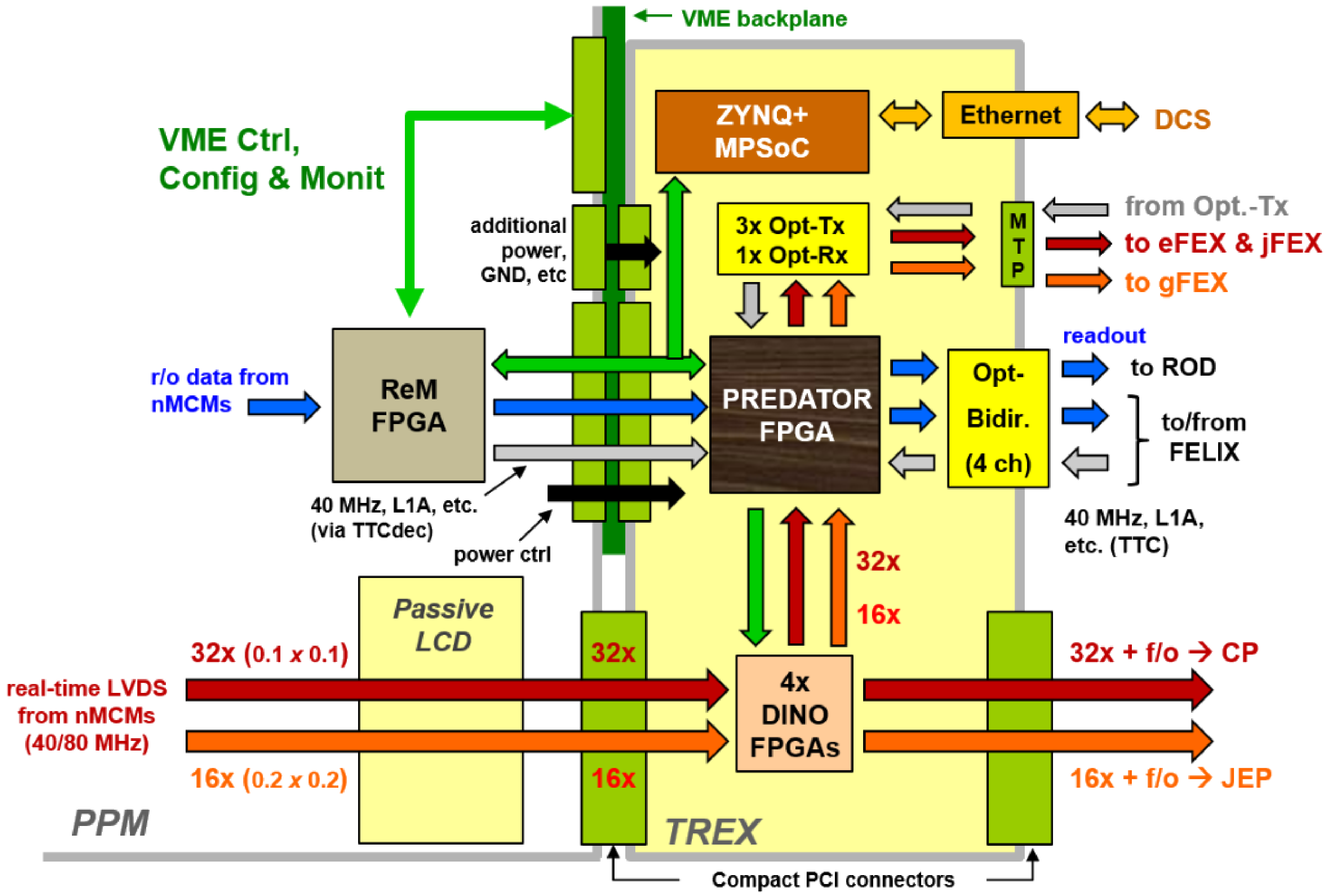
TREX

- Physical extension of the **PPM**
- Provides digitized hadronic E_T results from Tile to the FEXes via optical fibers
- Data readout to the FELIX and Run2 readout drivers (RODs)
- Maintains compatibility with the Run 2 system
- Xilinx Kintex UltraScale (PREDATOR)
- 4 Artix-7 (DINOs)
- Zynq Ultrascale+ MPSoC

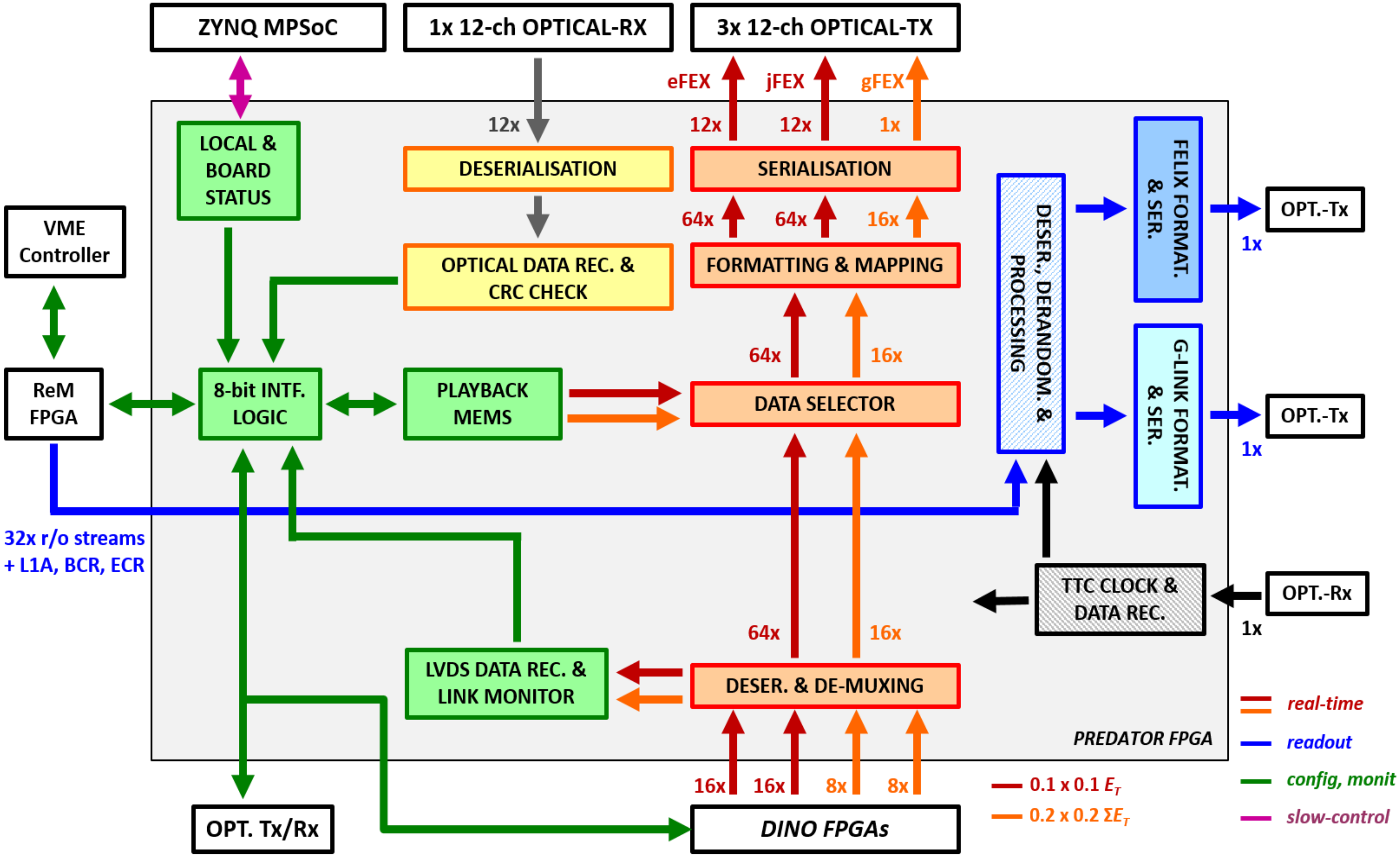


PPM + pre-production TREX module (v2)

TREX functionality

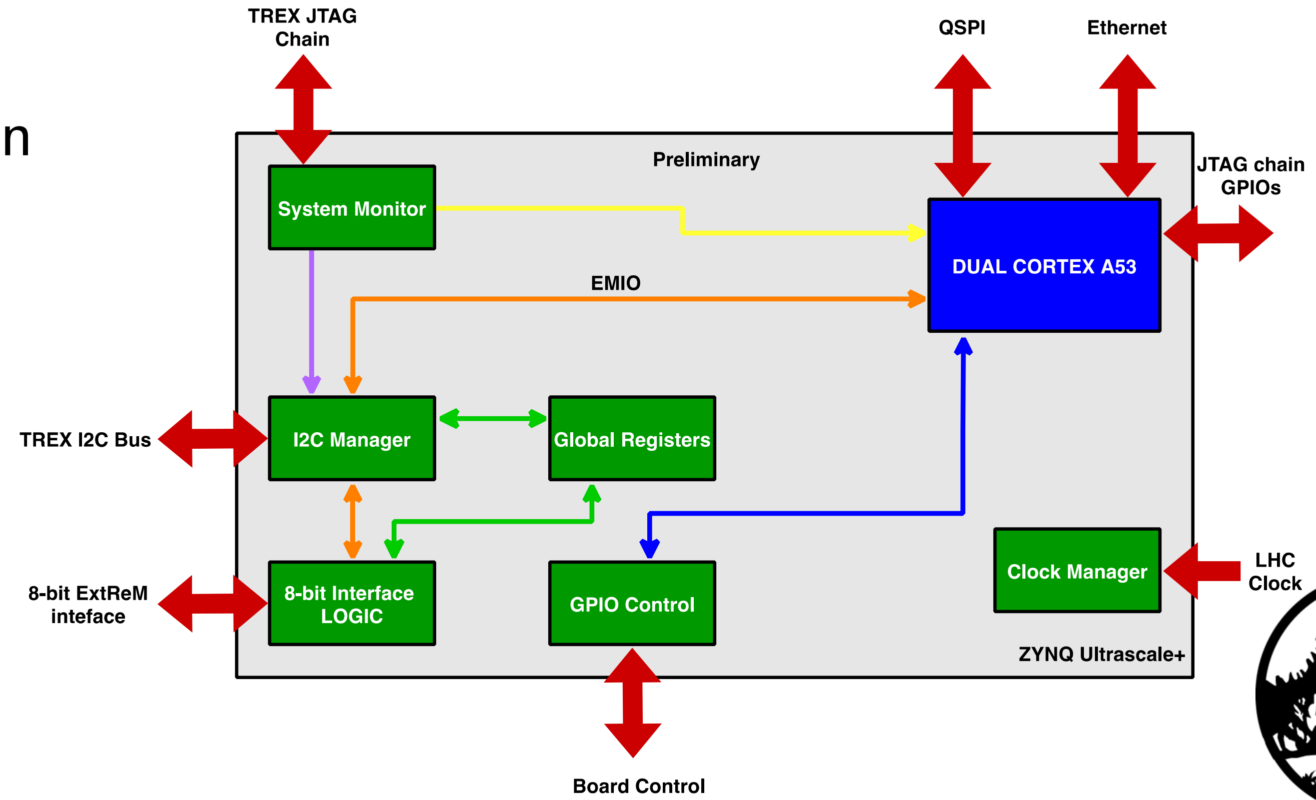


PREDATOR


ZYNQ MPSoC
1x 12-ch OPTICAL-RX
3x 12-ch OPTICAL-TX
eFEX
jFEX
gFEX
12x
12x
12x
1x
LOCAL & BOARD STATUS
DESERIALISATION
SERIALISATION
VME Controller
64x
64x
16x
OPTICAL DATA REC. & CRC CHECK
FORMATTING & MAPPING
DESER., DERANDOM. & PROCESSING
FELIX FORMAT. & SER.
OPT.-Tx
1x
64x
16x
ReM FPGA
8-bit INTF. LOGIC
PLAYBACK MEMS
DATA SELECTOR
G-LINK FORMAT. & SER.
OPT.-Tx
1x
32x r/o streams + L1A, BCR, ECR
TTC CLOCK & DATA REC.
OPT.-Rx
1x
64x
16x
LVDS DATA REC. & LINK MONITOR
DESER. & DE-MUXING
real-time
PREDATOR FPGA
readout
16x
16x
8x
8x
0.1 x 0.1 E_T
config, monit
OPT. Tx/Rx
DINO FPGAs
0.2 x 0.2 ΣE_T
slow-control

Zynq MPSoC

- Full board control (GPIO + I2C)
- Board initialization and configuration
- Monitoring VTI
- JTAG (Virtual cable)
- GbE



- Linux system
  - Xilinx Kernel and filesystem
- Custom device drivers
- Python framework
  - Dedicated apps

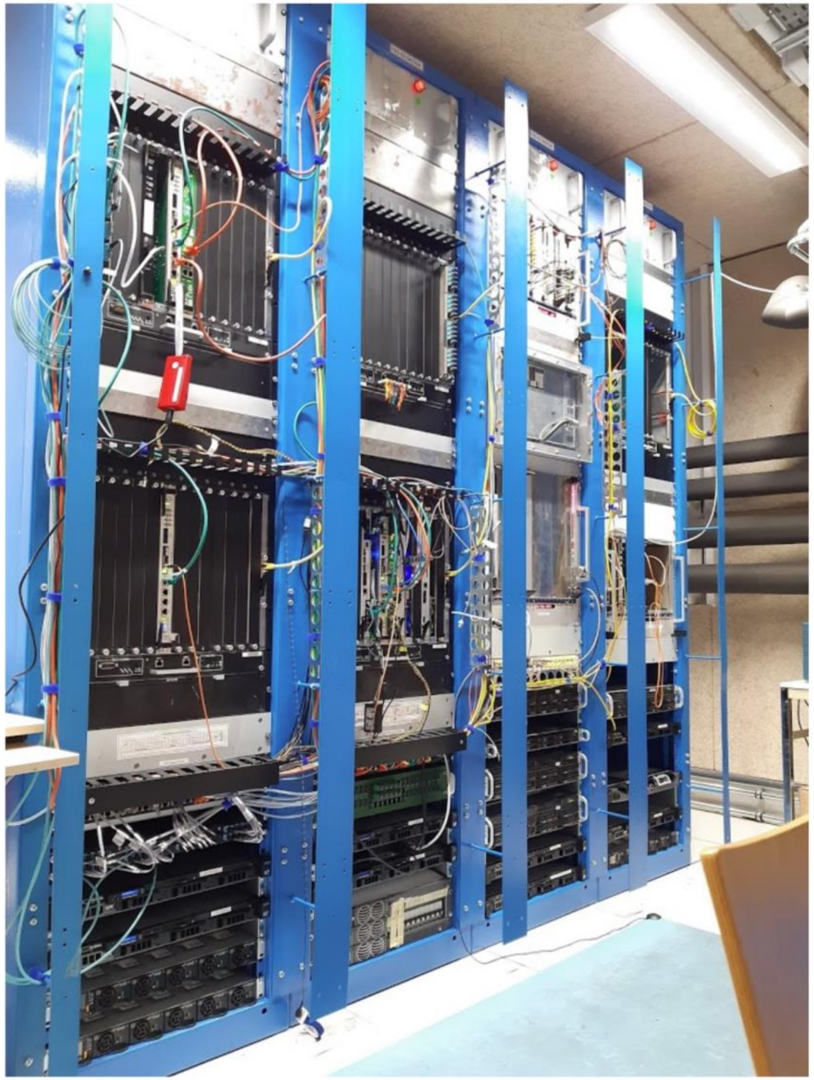
```
Welcome to Jurassic!
TREX Zynq Configurator v0.1
----------------------------------------
1) JTAG I/O Multiplexer
2) PLLs
3) LTC power managers
4) TREX power control
5) TREX programming modes
6) Temperatures and Voltages
7) Exit
```

Surface Test Facility at CERN

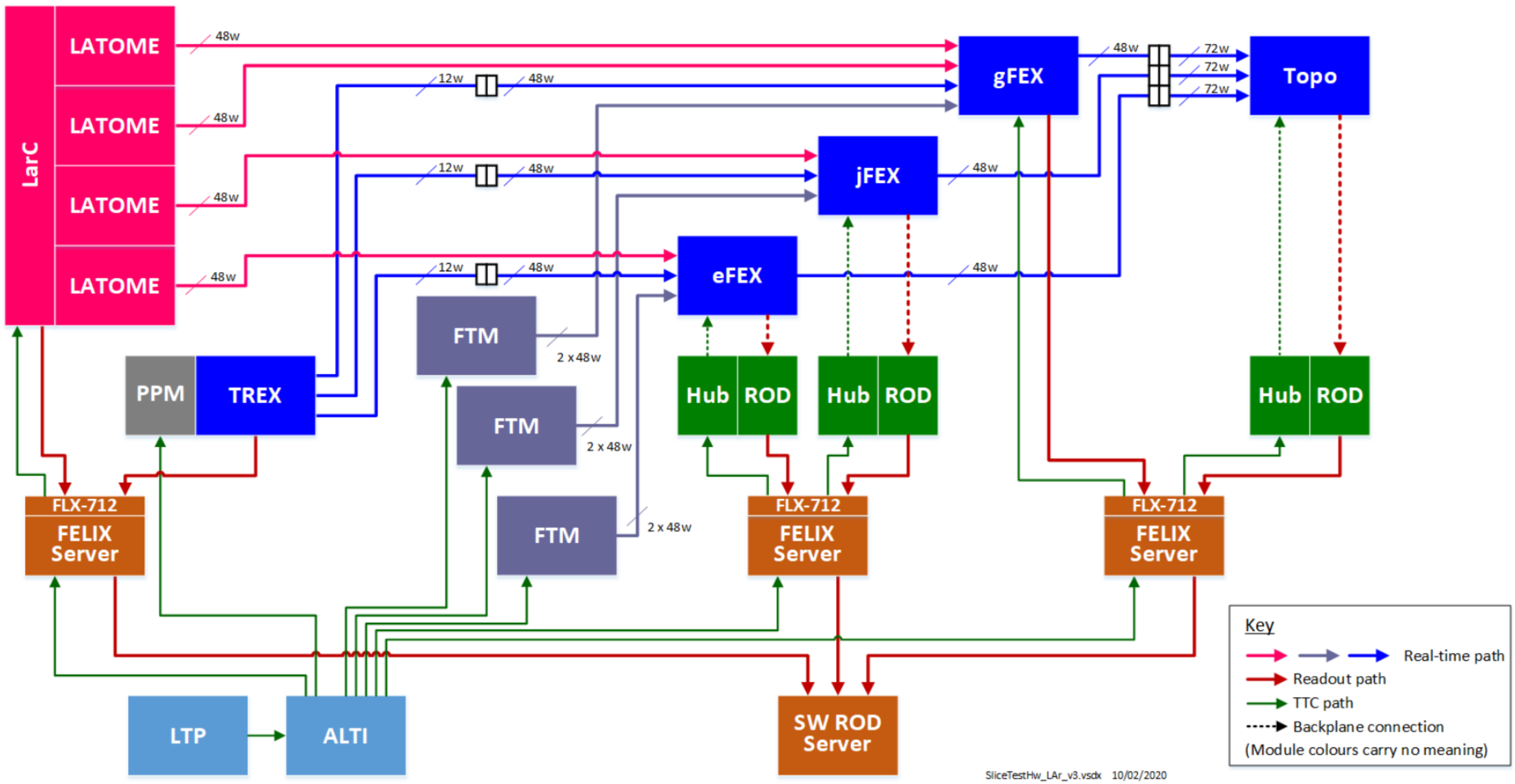
- Phase-I Infrastructure

- CERN ATCA shelves
  - eFEX, jFEX, gFEX modules
  - L1Topo module
  - 4 LATOME modules (LAr trigger interface)

- VME Crates
  - PPM + TREX modules
  - TTC/ ALTI module (provides trigger, timing and control signals)
- PCs:
  - Rack mounted
  - FELIX cards via PCIe
  - Monitoring and detector control
  - JTAG servers



Surface Test Facility at CERN



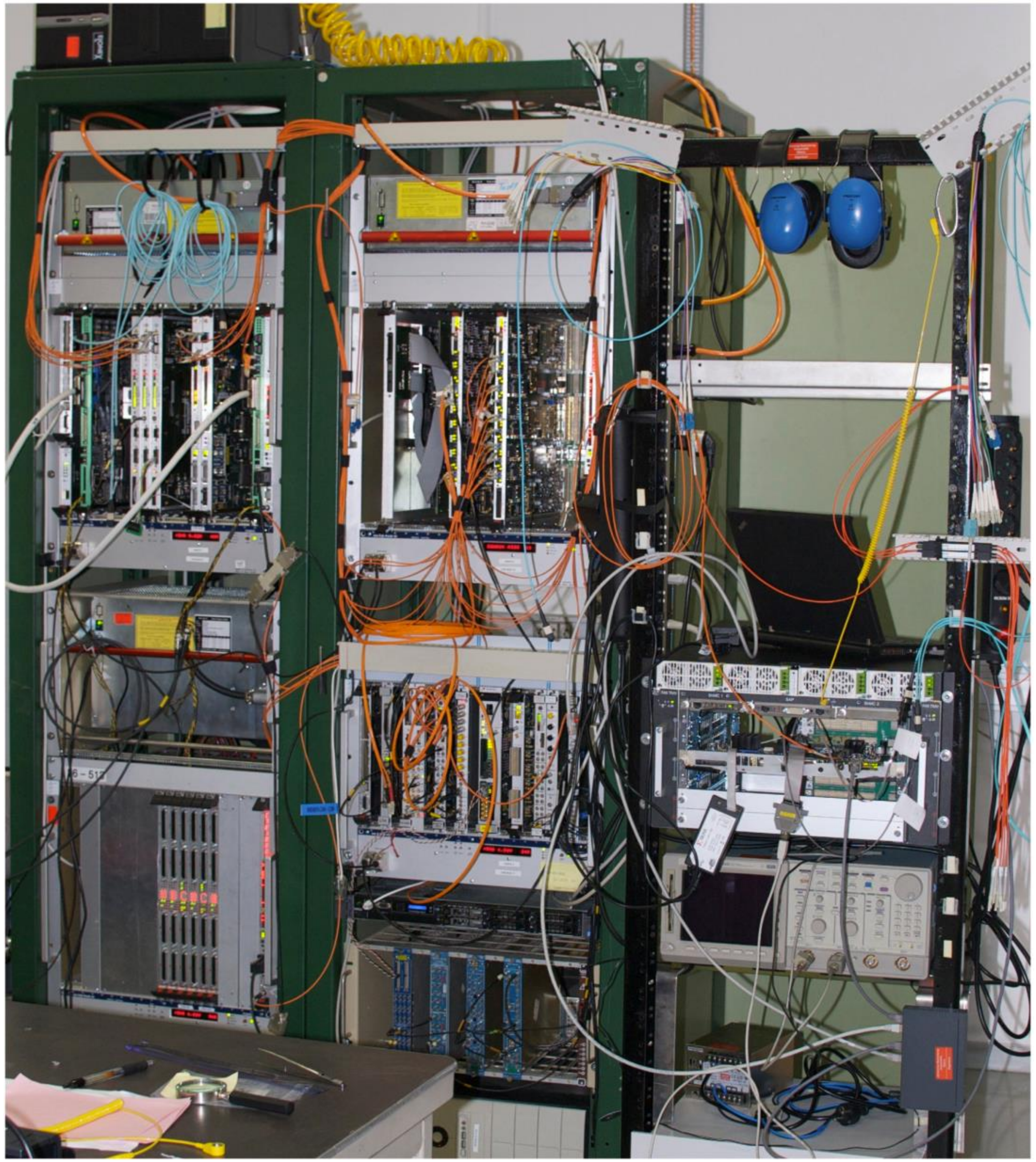
TREX Integration

- Real-time:
  - Protocol testing with all processors
  - Link stability
  - 8b/10b encoding and decoding
- Readout:
  - Data integrity
  - Encoding/decoding of the FELIX format
  - Clock recovery
- Monitoring:
  - Server/ Client based on UPC OA
  - Embedded framework
  - Device drivers for on-board sensors

TREX modules installed at STF

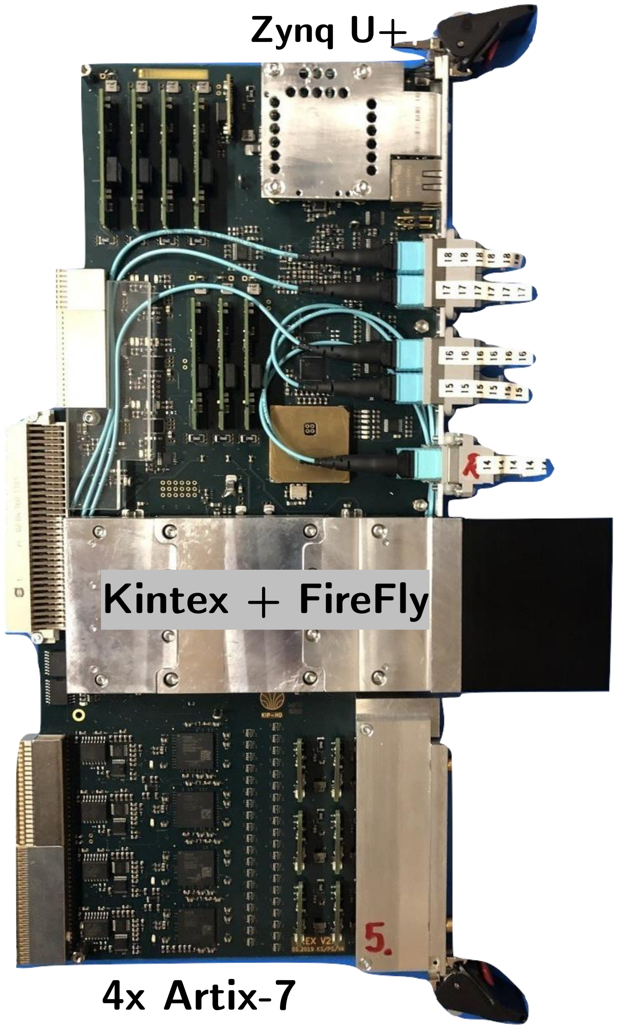
Bat. 104 at CERN

- Run 2 infrastructure
- Allows for testing with legacy systems
- Real-time path:
  - 11m long electrical cabling
  - Cluster Processor
  - Jet Energy Processor
- Readout:
  - Readout driver system
  - Single optical fiber per module
- Legacy Monitoring system
  - Based on CAN

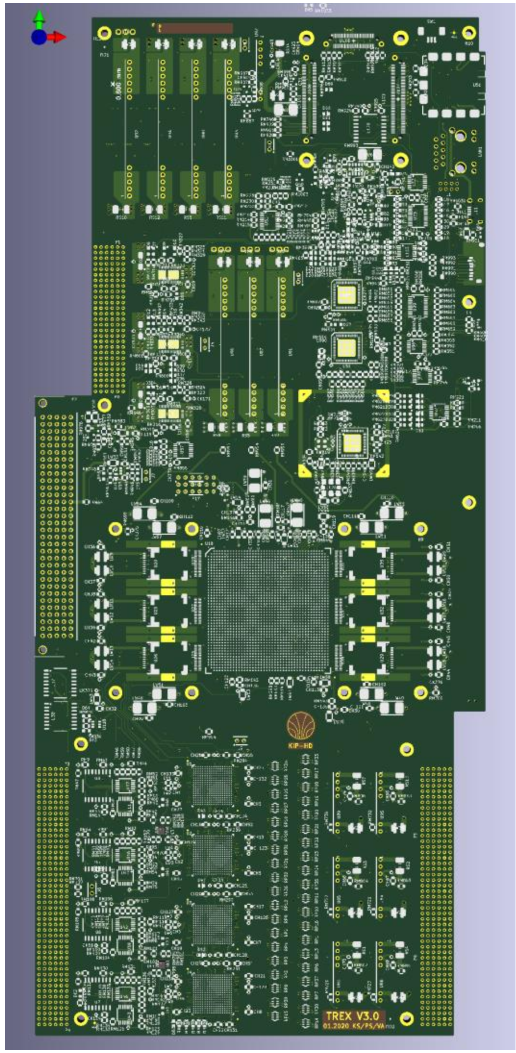


TREX production

- 18-layer PCB
  - FR4-based dielectric
- 5 pre-production boards (v2)
  - Rigorous testing of all hardware components and functionality
- Implementation and design changes of the production board (v3)
- Manual modifications of v2 boards to ensure feature parity
- Preparation for production
  - Schematic frozen
  - QA



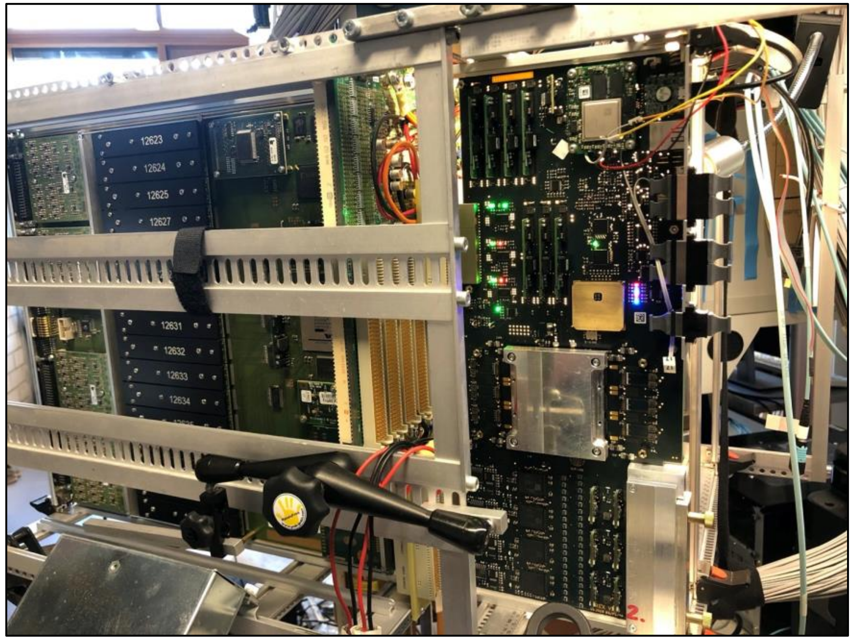
TREX module (v2)

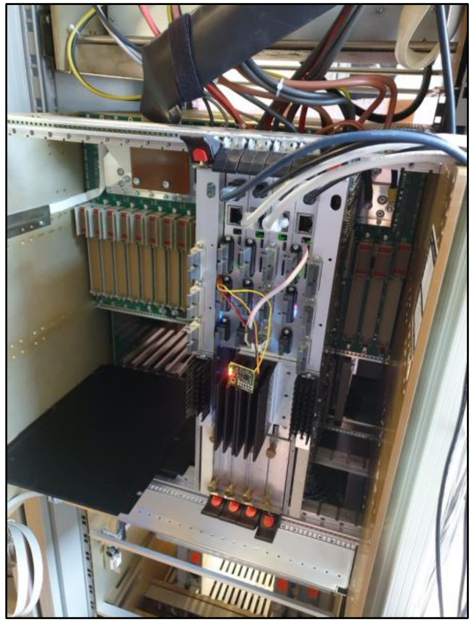


TREX PCB (v3)

Testbenches at Heidelberg

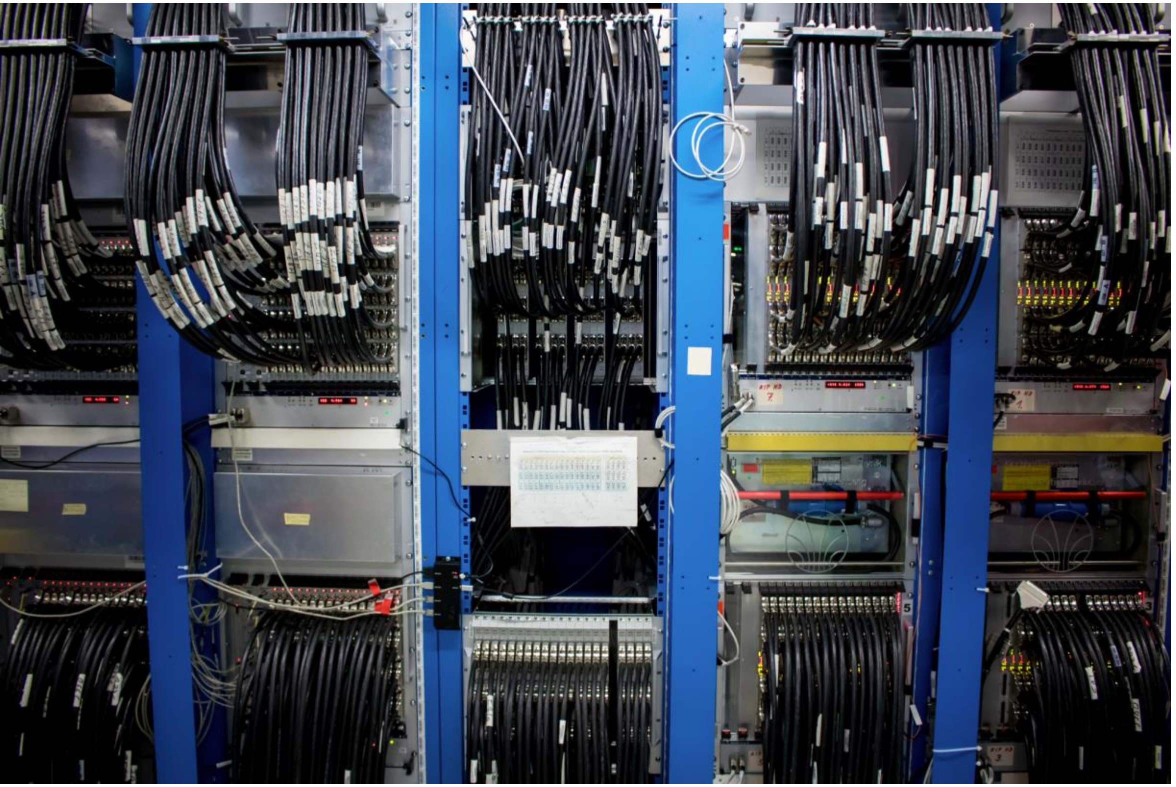
- **Single-board testbench (1st stage)**
  - Custom VME crate with homebrew VME crate controller
  - TREX initialization and power-up
  - Core component testing
  - PPM – TREX communication
  - LVDS loopback testing





- **Multi-board testbench (2nd stage)**
  - Wiener crate with TREX modifications
  - Concurrent Technologies VME crate controller
  - Emulates crate setup at CERN
  - Simultaneous testing of up to 4 TREXes
  - Long-term optical loopback testing
  - System stability

L1Calo in the Cavern



Front view of the L1Calo system

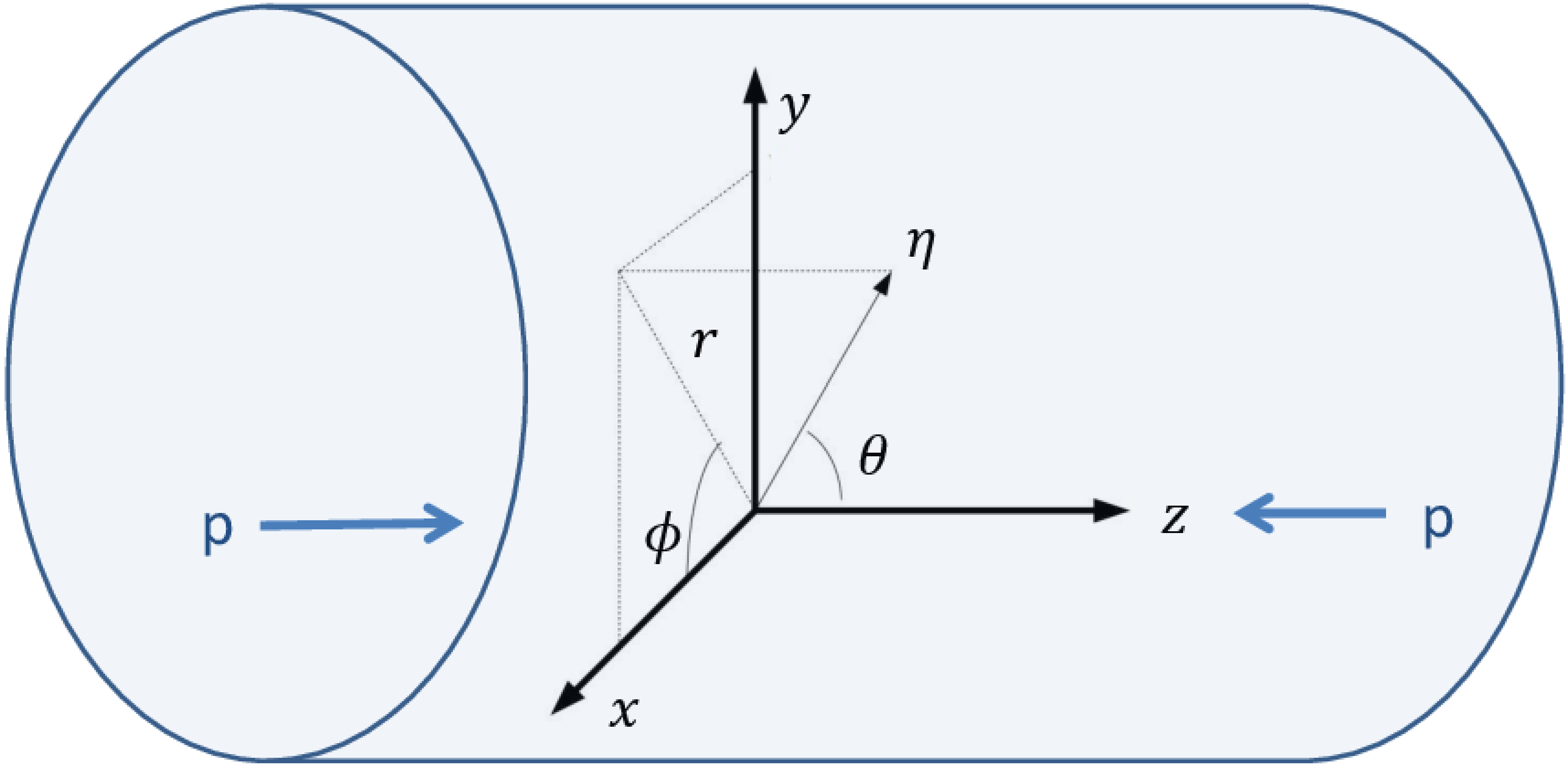
Rear view of the PreProcessor crate

Summary

- L1Calo upgrade is progressing smoothly
- Most of Phase-I modules in pre-production or production state
- Integration tests between modules ongoing
- Data formats/ protocols well defined
- QA/ Validation scheme for production hardware prepared
- Planned installation by the end of the year

Backup

ATLAS coordinate system



$$\eta \equiv -\ln\left[\tan\left(\frac{\theta}{2}\right)\right]$$

FELIX card

ATCA shelves at STF