Physikalisches Institut, Heidelberg University

Pixel Size study of HV-MAPS using TCAD Simulations

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Bundesministerium
für Bildung
und Forschung

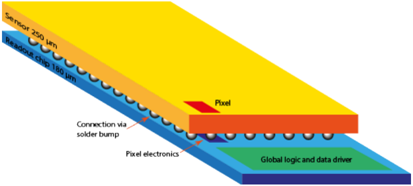
Pixel Detectors

Pixel detectors for particle tracking have resulted resulted in modules which stand

1. High rates
2. Timing requirements
3. Very harsh radiation environment

Current pixel detector technologies:

- Hybrid (passive sensor bump-bonded to an active read-out chip)



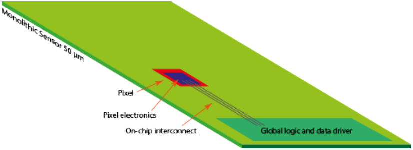
Disadvantages:

- High cost
- Large amounts of material
  → disqualify it for tracking low momentum particles

Pixel Detectors

Current pixel detector technologies:

- Hybrid (passive sensor bump-bonded to an active read-out chip)
- Monolithic (such as the MIMOSA detectors)



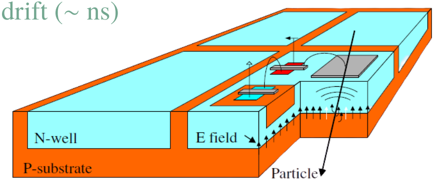
Disadvantages:

- Collect charges via diffusion
  → Slow for high rate applications

Pixel Detectors

Current pixel detector technologies:

- Hybrid (passive sensor bump-bonded to an active read-out chip)
- Monolithic (such as the MIMOSA detectors)
- High Voltage Monolithic Active Pixel Sensors (HV-MAPS)
  - ☐ Integrated readout electronic and sensor (low material budget)
  - ☐ Implemented in a commercial CMOS process (cheaper than hybrid sensors)
  - ☐ Depletion area ~ 15 μm at -60V for 20 Ωcm
  - ☐ Fast charge collection via drift (~ ns)

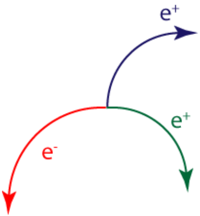


I. Peric /A novel monolithic pixelated particle detector implemented in high-voltage CMOS technology, NIM A 2007

HV-MAPS Application

→ The Mu3e Pixel Tracker

The goal of the Mu3e experiment is to search for the lepton flavour violating decay $\mu^+ \rightarrow e^+e^-e^+$ with an ultimate sensitivity of one in 10^{16} μ-decays



- Energies of the decay particles up to half the muon mass (53 MeV)
- Excellent momentum resolution (background $\mu \rightarrow ee\upsilon\upsilon$)
- Multiple Coulomb scattering affects momentum resolution
- Low material budget
- High Rate of muons decays

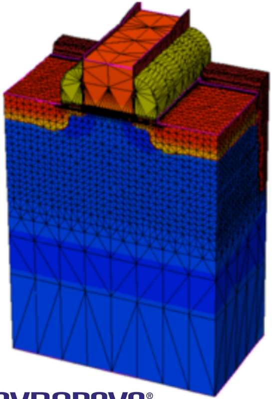
TCAD

Technology Computer Aided Design

Use of computer simulations to develop and optimize semiconductor processing technologies and devices.

Why TCAD?

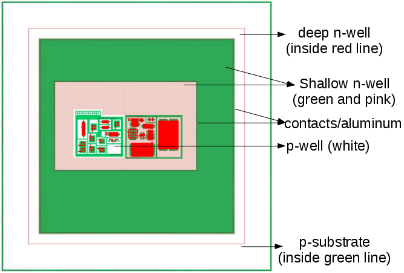
- Fabrication process and electrical behavior.
- Tiny and complex structures in 2D and 3D.
- Save time and money.
- Complement to laboratory measurements.
- Estimates and optimizes properties of the sensor as
  - ☐ **Breakdown Voltage**
  - ☐ **Deplection zone**
  - ☐ **Charge collection time**
  - ☐ **Pixel Capacitance**
  - ☐ **Electric Field**



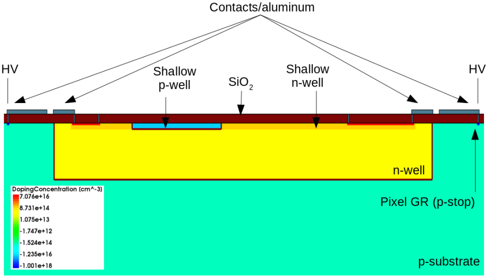
SYNOPSYS®

TCAD Process Flow

- Structure Simulation (Device structure and doping profiles)



*Layout of MuPix8



- Device Simulation (Physical models: temperature, mobility, recombination, avalanche, radiation damage)
  1. Quasistationary (Breakdown Voltage, Capacitance, Electric Field)
  2. Transient Simulation of Minimum Ionizing Particle (MIP) (Charge collection process)

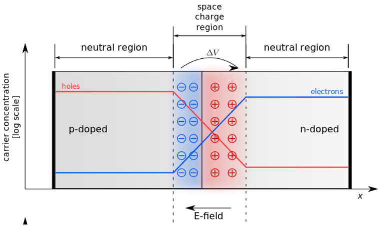
Depletion zone

pn-junction

→ Reversely biased pn-junction is the building block of HV-MAPS structures

Why?

- Intrinsic silicon substrate
  $\sim 10^9$ free charge carriers
  $\sim 10^4$ induced by ionizing particles
- pn-junction reduces the number of free charge carriers by depleting the silicon volume



- Intrinsic silicon: Absence of impurities
- Doping: Mechanism to alter conductivity (inserting additional states in the forbidden region)
  → n-doped: phosphorus, excess of electrons
  → p-doped: boron, excess oh holes

Depletion zone

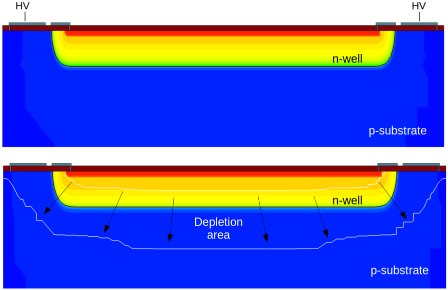
→ Reversely biased pn-junction is the building block of HV-MAPS structures

- Structures created using doping profiles (Gaussian)

- p-doped substrate
- Highly doped n-implant ($\sim 10^{16}$)
- Width of depletion area:

$$W \approx \sqrt{\frac{2 * \epsilon_0 * \epsilon_{Si} * V}{e * N_D}}$$

N_D → Concentration of donors



Depletion zone

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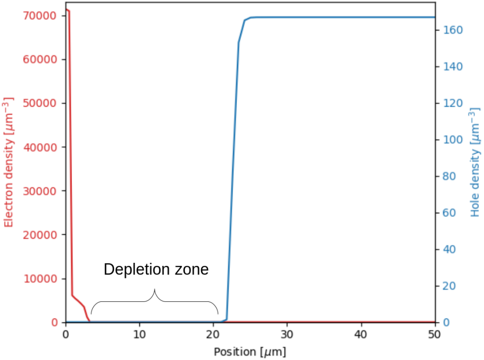

→ Depletion zone:

☐ Region depleted from free charge carriers

Depletion zone

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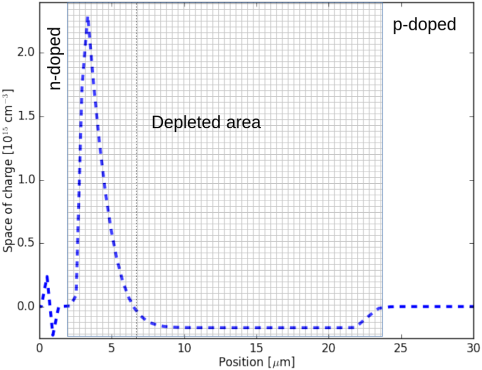

→ Depletion zone:

☐ Region depleted from free charge carriers

☐ Electrically charged

Depletion zone

→ Reversely biased pn-junction is the building block of HV-MAPS structures

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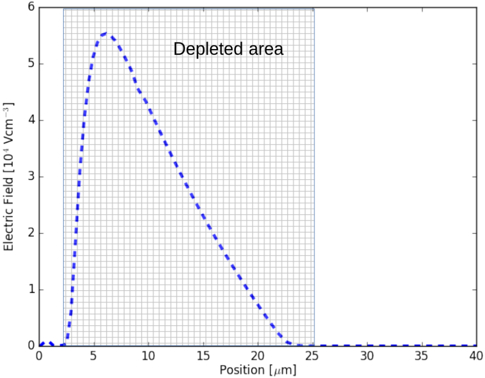
→ Depletion zone:



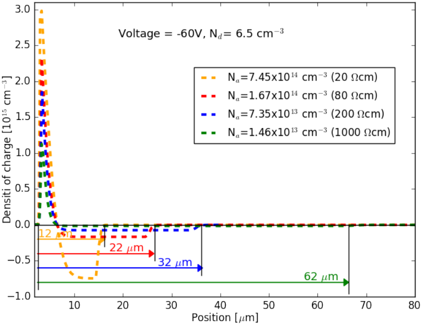
☐ Region depleted from free charge carriers

☐ Electrically charged

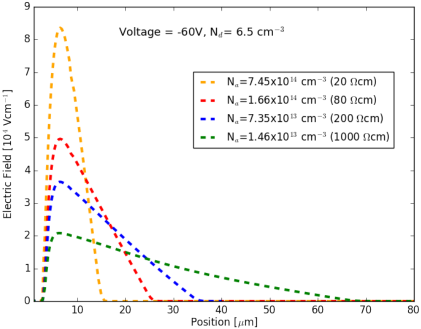
☐ Electric Field that collects the signal charge and suppresses the leakage current

Substrate resistivity

- Depletion depth



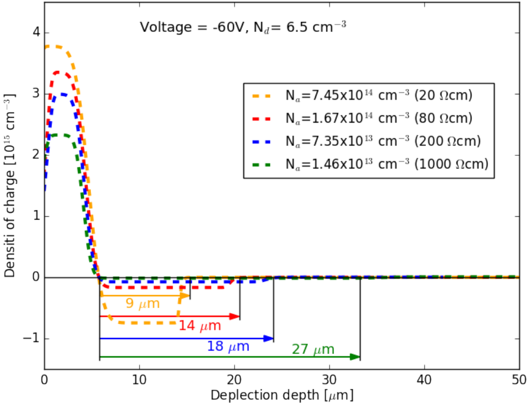
- Electric Field



1. Depletion depth
    - Higher resistivity → Thicker depletion zone (Larger sensitive area)
2. Electric Field
    - Lower resistivity → Higher Electric Field (Faster charge collection)

Substrate resistivity

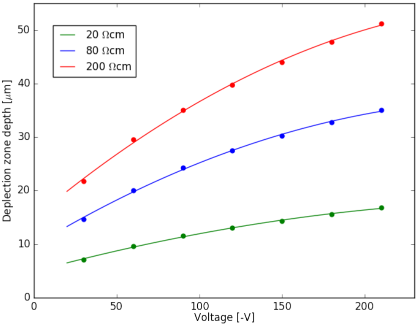
- Lateral depletion



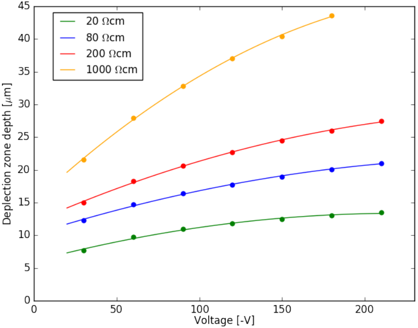
- Higher resistivity → Larger lateral depletion (Higher efficiency and faster collection charge in the area between pixels)

Depletion Vs Voltage (Substrate resistivity)

- Depletion depth (just p-region)



- Lateral deplection



$$depletion = a * |Voltage|^2 + b * |Voltage| + c$$

$a = 1.302 * 10^{-8} * r^2 + 4.4520 * 10^{-6} * r + 4.766 * 10^{-5}$

$b = -6.214 * 10^{-6} * r^2 + 2.3420 * 10^{-3} * r + 3.948 * 10^{-2}$

$c = 2.053 * 10^{-4} * r^2 - 0.1006 * r + 2.9$

$a = -1.292 * 10^{-10} * r^2 - 1.645 * 10^{-7} * r - 1.39 * 10^{-4}$

$b = -9.542 * 10^{-8} * r^2 + 2.702 * 10^{-4} * r + 6.052 * 10^{-2}$

$c = -2.893 * 10^{-5} * r^2 + 0.380 * 10^{-1} * r + 6.069$

*r → resistivity in Ωcm

Depletion Vs Voltage (Substrate resistivity)

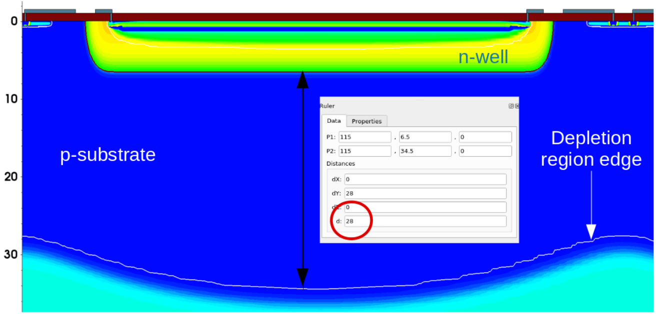
- Depletion depth [μm] (just p-region)

Resistivity	-60 V	-120 V	-180 V
20 Ωcm	9.39	13.00	16.34
80 Ωcm	19.70	27.47	34.23
200 Ωcm	28.87	39.92	49.98

- Lateral deplection [μm]

Resistivity	-60 V	-120 V	-180 V
20 Ωcm	10.26	12.67	14.30
80 Ωcm	13.25	16.49	19.10
200 Ωcm	18.51	23.23	27.57
1000 Ωcm	27.64	37.09	44.84

① Depletion depth (center of pixel):



P1: 115 , 6.5 , 0
P2: 115 , 34.5 , 0
Distances
dX: 0
dY: 28
dZ: 0
d: 28

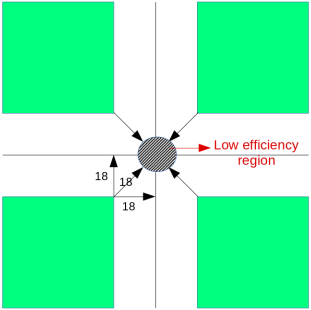
Depletion Vs Voltage (Substrate resistivity)

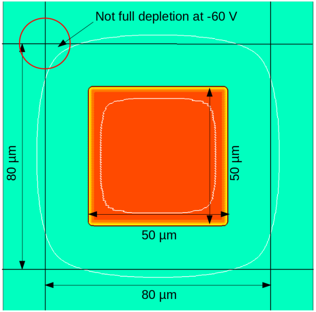
② Lateral depletion: (Let's use a 200 Ωcm MuPix sensors as example)

→ Pixel size requirement: 80 μm → Working Voltage (MuPix 8): - 60 V

- Lateral depletion (using equation): 18.51 μm
- Distance between diodes < 36 μm
- Diode size > 44 μm

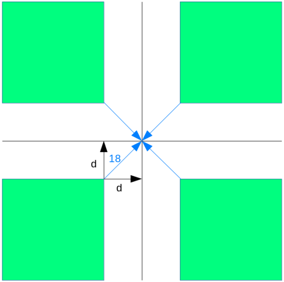
But distance between diodes at the pixel corner is higher

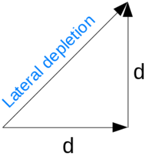




Depletion Vs Voltage (Substrate resistivity)

→ In an ideal case (equal depletion at pixel corners)





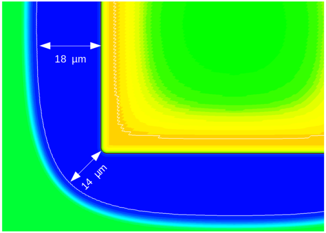
$$(\text{Lateral depletion})^2 = 2 * \text{d}^2$$

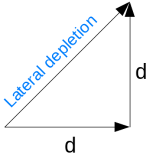
$$\text{Distance between diodes} = 2* \frac{\textit{Lateral depletion}}{\sqrt{2}}$$

- Distance between diodes* < 26 μm
  before → 36 μm
- Diode size* > 55 μm
  before → 44 μm

Depletion Vs Voltage (Substrate resistivity)

→ In an ideal case (equal depletion at pixel corners)





$$(\text{Lateral depletion})^2 = 2 * d^2 = 18^2$$

$$\text{Distance between diodes} = 2* \frac{\textit{Lateral depletion}}{\sqrt{2}}$$

- Distance between diodes* < 26 μm

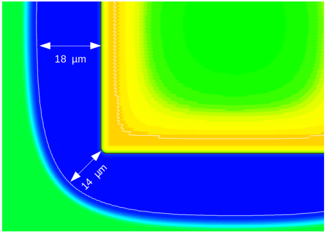
  before → 36 μm

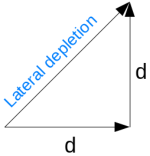
- Diode size* > 54 μm

  before → 44 μm

*Need to be optimize with 3D simulations for lateral depletion in the pixel corners

Depletion Vs Voltage (Substrate resistivity)





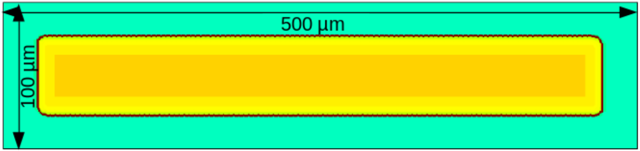
$$(\text{Lateral depletion})^2 = 2 * d^2 = 14^2$$

$$\text{Distance between diodes} = 2 * \frac{\textit{Lateral depletion}}{\sqrt{2}}$$

- Distance between diodes < 20 μm
  before → 26 μm
- Diode size > 60 μm
  before → 54 μm

Depletion Vs Voltage (Substrate resistivity)

→ For a 100 x 500 μm^2 pixel size



❶ Distance between diodes

- 200 Ωcm
  → -60 V: 20 μm
  → -120 V: 24 μm
- 80 Ωcm
  → -60 V: 14 μm
  → -120 V: 18 μm

❷ Diode size

- 200 Ωcm
  → -60 V: 80 x 480 μm^2
  → -120 V: 76 x 476 μm^2
- 80 Ωcm
  → -60 V: 86 x 486 μm^2
  → -120 V: 82 x 482 μm^2

Capacitance

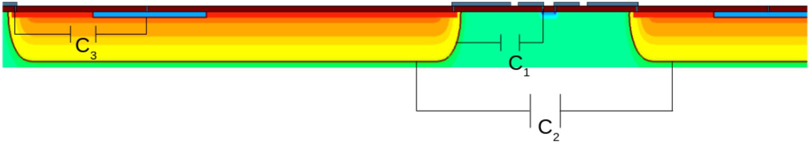
Pixel Capacitance

→ Importance of the capacitance:

- Significant lost of the output voltage step for an amplifier with high detector capacitance
- Interpixel capacitance determines the cross talk between pixels

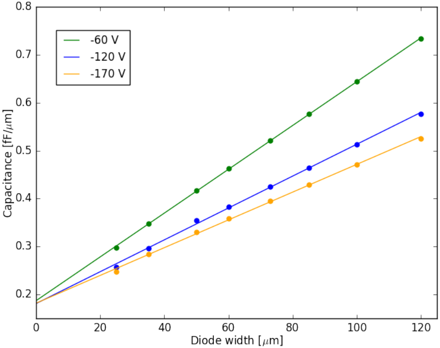
Total Capacitance

- Diode Capacitance
- Interpixel Capacitance
- Capacitance of the p-well

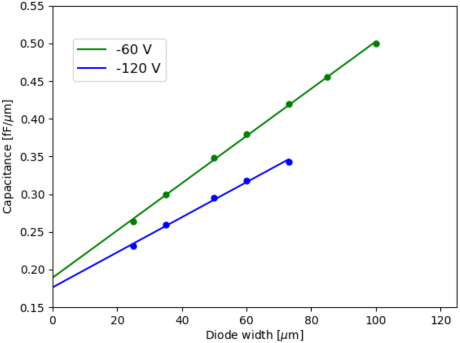


Diode Capacitance Vs Diode width

- 80 Ωcm



- 200 Ωcm

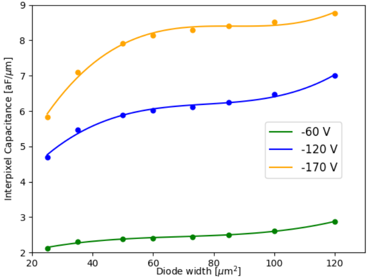


→ 80 Ωcm:

$$C_0[\frac{fF}{\mu m}] = (-1.538 * |V| + 539) * 10^{-5} * diode\ width + 0.18$$

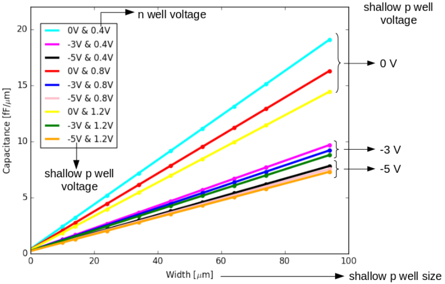
InterPixel and Shallow p-well Capacitance

InterPixel Capacitance (C_1)



*Using pixel isolation

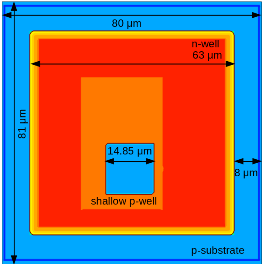
Shallow p-well Capacitance (C_2)



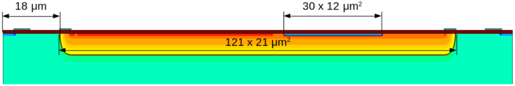
58 % decrease in the capacitance from 0 V to -5 V !!!

Prototypes

- MuPix8



- AtlasPix3



- Total pixel capacitance 80 Ωcm ($C_t = C_0 + C_1 + C_2$)

MuPix8
$C_t = 37.38fF + 0.61fF + 60.13fF$
$C_t = 98.12fF$

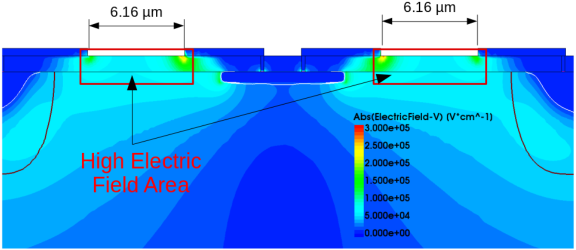
AtlasPix3
$C_t = 15.13fF + 0.60fF + 96.44fF$
$C_t = 112.17fF$

@ -60 V @ 80 Ωcm

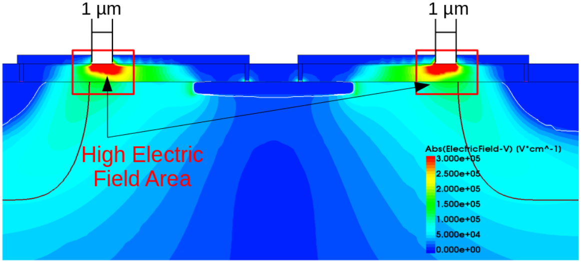
Breakdown Voltge

Electric Field

- AtlasPix3 (200 Ωcm at -60 V)



- MuPix8 (200 Ωcm at -60 V)



Summary

- TCAD simulation is a powerful tool for designing and optimization of semiconductor detectors.

→ Outlook

- Ongoing studies of pixel structure in 3D and charge collection time
- Testbeam results with ATLASPix 3 for charge sharing to be analyzed
- Future testbeam campaign with different pixel size