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Technical specification

Embedded Monitoring and Control Interface

Abstract

This document specifies the features and layout of the new embedded slow control module developed for the HL-LHC experiments. It is based on radiation hard components and primarily meant to serve as a bidirectional interface between experiment front-end electronics and detector control systems (DCS).

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1. Introduction

The importance of the efficient and reliable detector control system (DCS) increases with the complexity of the high energy physics experiments. The High Luminosity upgrade of the LHC puts further radiation tolerance onto the innermost detectors and relevant control systems. To fulfill these requirements a new DCS front-end interface hardware solution based on CERN Radiation Hard Optical Link Project components, the low power Giga Bit Transceiver (lpGBT) and the Versatile Link+ (VL+), is being proposed. This new interface system is targeted for deployment during the Long Shutdown 3 of the LHC. Note that the proposed system is meant to complement the ELMB2 [1] in aspects related to radiation tolerance and appliance.

2. Overview

The new system will consist of two core components: the Embedded Monitoring and Control Interface (EMCI) and the Embedded Monitoring Processor (EMP).
The aim of the EMCI, which is placed in a radiation-hard environment, is to work as an interface for the slow-control signals going in between different Front-Ends (FE) and the DCS system. It is based on the lpGBT, which combines all the signals of the FEs in one bidirectional channel and interfaces with the VTRx+, the optical transceiver, which transmits the data through the high-speed optical link. Both chips were designed at CERN to work in radiation-hard environments.
The connection from the EMCI to the FEs is done using a passive splitter board. This board, plugged into the EMCI by means of an FMC connector, is customized in order to be compatible to the FEs connection interface. Most common versions of the splitter boards are provided, but the user might design his own. Alternatively to interfacing FEs via the splitter board, the EMCI can also be mounted as mezzanine directly onto a carrier equipped with the FMC connector conform to the EMCI pinout. The power input to the EMCI is provided locally through the FMC connector.

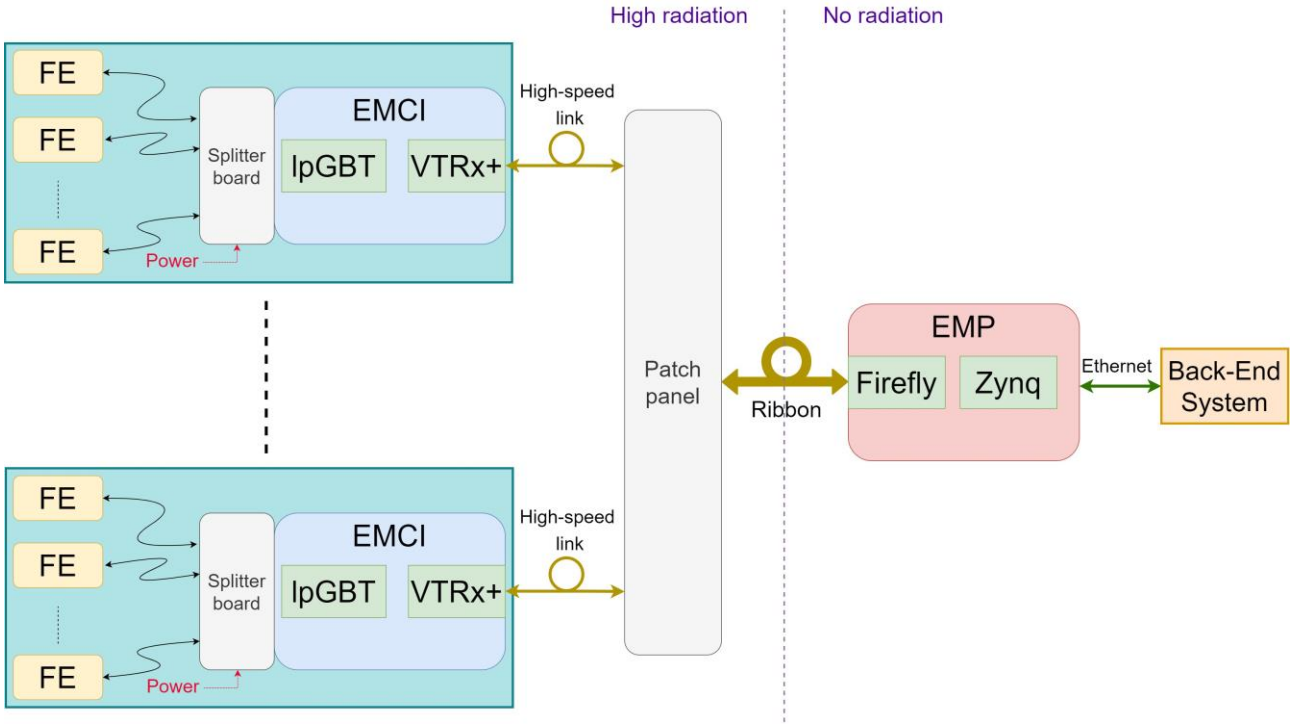

Figure 1: EMCI-EMP block diagram for a typical use case

At the same time, several EMCI VTRx+ are connected through a multichannel optical transceiver mounted on one EMP, which is placed in a radiation soft environment. The EMP, built on COTS components, processes and delivers the data to the counting room by means of an Ethernet connection. Note that the EMP project is still under conceptual design and may evolve in the future.

Given that the lpGBT is the main component of the EMCI, most of the features and descriptions shown in this document are referred to, and can be extended by the lpGBT manual [2].

3. Functionality

The EMCI offers all the features provided by the lpGBT that are listed below:

- eLinks

  The slow-control data to/from FE can be transmitted through electrical connections called eLinks. The EMCI can interface simultaneously up to 28 devices for uplink (RX from the EMCI point of view) transmission and up to 16 devices for the downlink transmission (TX) as well as up to 28 synchronized clock signals, in case the FE requires it. The eLinks use the CERN Low Power Signaling (CLPS) standard, presented in section 4.1.1.1. These communication lines can be DC or AC coupled (see section 4.1.1).

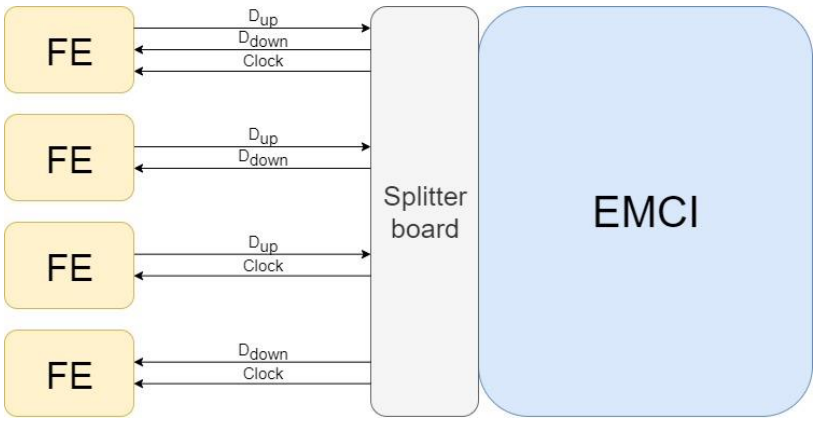

Figure 2: Different eLink connection modes

The eLinks are divided in groups of 4, each group using the same bandwidth. If the bandwidth is set to minimum (x1), all four eLinks are available. However, if the bandwidth is higher (x2 or x4) less eLinks become available in that group (2 or 1, respectively).

Table 1 and Table 2 show the maximum number of eLinks available (for all the groups) depending on the chosen bandwidth. Additionally, there is available an extra slower eLink which can be used to connect an SCA or another device at 80 Mb/s.

Output eLinks (down-link)			
Bandwidth [Mb/s]	80	160	320
Maximum number	16	8	4

Table 1: Maximum number of downlinks per bandwidth

Input eLinks (up-link)												
Up-link bandwidth [Gb/s]	5.12						10.24					
FEC coding	FEC5			FEC12			FEC5			FEC12		
Bandwidth [Mb/s]	160	320	640	160	320	640	320	640	1280	320	640	1280
Maximum number	28	14	7	24	12	6	28	14	7	24	12	6

Table 2: Maximum number of uplinks per bandwidth

- Phase programmable clocks

  Apart from the clocks provided with the eLinks, the EMCI provides 4 extra differential clock signals. These clocks are programmable independently in frequency (40, 80, 160, 320, 640 and 1280 MHz) and in phase (in 48.8 ps steps).

- General purpose I/O

  The EMCI has 16 general-purpose I/O pins synchronous with the internal system clock (40 MHz), which go from 0 V (low) to 1.2 V (high). Each I/O has a programmable built-in pull-up and pull-down circuit.

- I2C interfaces

  The EMCI also has three independent I2C master interfaces (one of which is dedicated to VTRx+ configuration), with the following features:

  - Compliance with I2C 7-bit, 8-bit and 10-bit addressing
  - Concurrent operation of the three channels
  - Independently programmable data transfer rates: 100 kHz, 200 kHz, 400 kHz, 1 MHz
  - Supports single-byte and multi-byte (<=16) I2C read/write bus operations
  - Supports read-modify-write bitwise operations with OR or XOR masks (7-bit addressing)
  - The SCL outputs are configurable as open-drain or CMOS signals
  - Voltage levels are 0V (low) and 1.2V (high)

  Each of the SCL and SDA pins has an internal programmable pull-up resistor.

  An additional I2C slave interface is also available for lpGBT configuration (see section 4.1.4).

- Analog peripherals

  The EMCI provides an 8-channel multiplexed 10-bit SAR ADC and a 12-bit R-2R voltage DAC.
  The ADC has 8 input pins (some of them can be used for internal EMCI measurements by means of a jumper, see Table 3), which can be combined for differential measurements as well as be used individually for single-ended measurements. The input dynamic range goes from 0 V to +1 V and a programmable gain stage (x2, x8, x16 and x32) is used for measuring smaller voltages.
  The ADC is also used for internal measurements of the lpGBT (temperature sensor and power supply voltage).
  The DAC can provide voltages ranging from 0 to +1 V.

ADC channel	Primary use	Secondary use (with jumper)
0	VTRX+ NTC	-
1	VTRX+ RSSI	-
2	External (FMC)	bPOL12V PTAT
3	External (FMC)	bPOL2V5 PTAT
4	External (FMC)	2.5V
5	External (FMC)	12V
6	External (FMC)	-
7	External (FMC)	-

Table 3: EMCI ADC channel use

- High-speed link

  A VTRx+ is plugged into the EMCI for transmitting the data through the fiber optics to/from the EMP. The system has a downlink bandwidth of 2.56 Gb/s and an uplink bandwidth of 5.12 or 10.24 Gb/s, depending on configuration. The links are equipped with Forward Error Correction (FEC) coding and with scrambling circuit to maintain the DC balance of the transmitted data and to enable reliable Clock and Data Recovery (CDR).

4. Implementation

The EMCI core component is the lpGBT, which offers most of the functionality described in section 3. The schematics of the EMCI can be found in the appendix 7.1. A general overview of the EMCI can be seen in Figure 3.

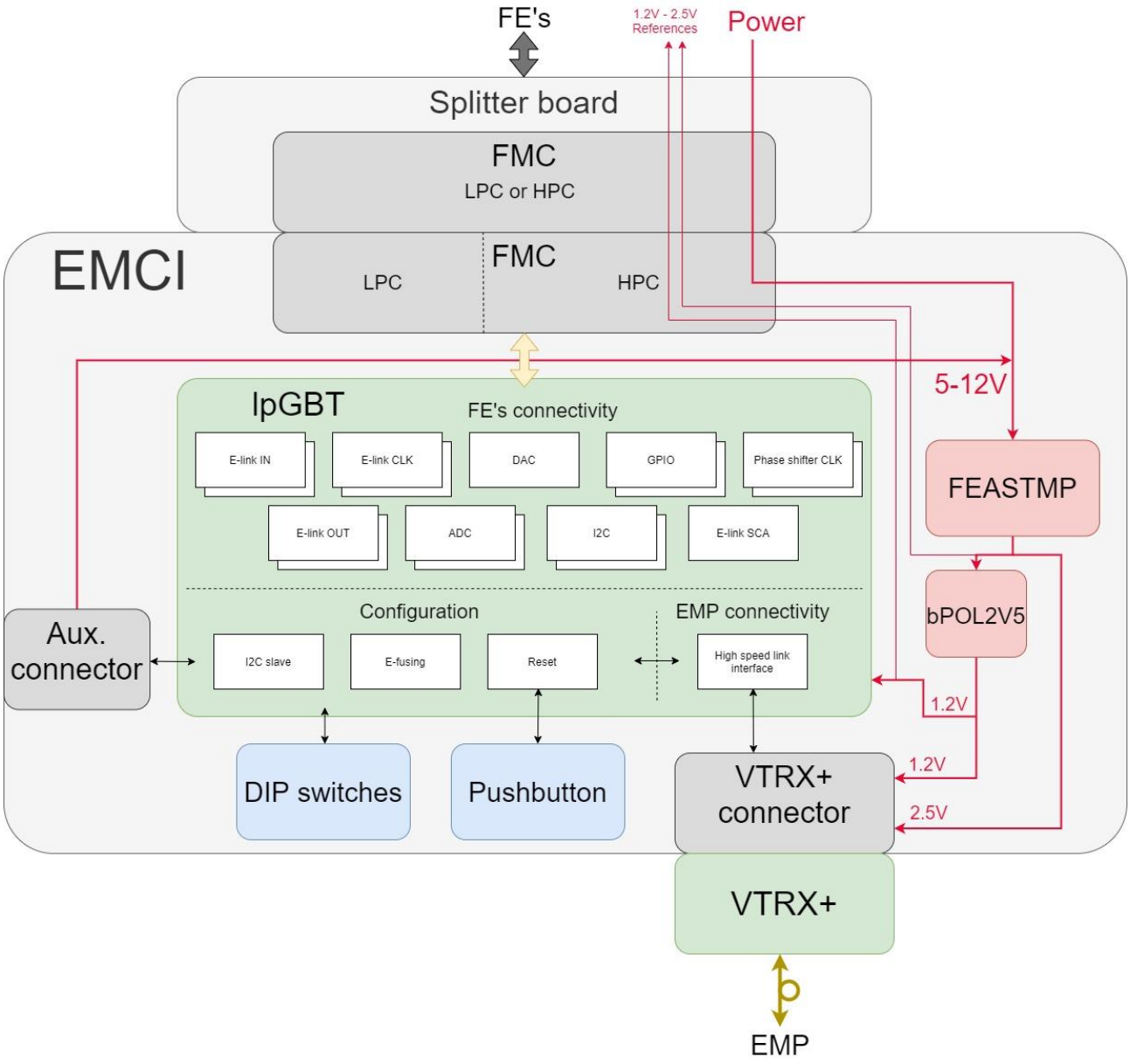

Figure 3: General EMCI block diagram

4.1 Architecture

The schematics of the eLinks and the high-speed interface features are presented below, as well as the power requirements and the configuration of the lpGBT.

4.1.1 eLinks

As explained before, the eLinks supply downlink data and clock and receive uplink data. The transmitters drive 100-ohm differential line without the necessity of any external components to the lpGBT. The receivers can be configured to have an internal 100-ohm termination enabled, as well as the possibility to use an equalizer and common mode bias circuit (see Figure 4).

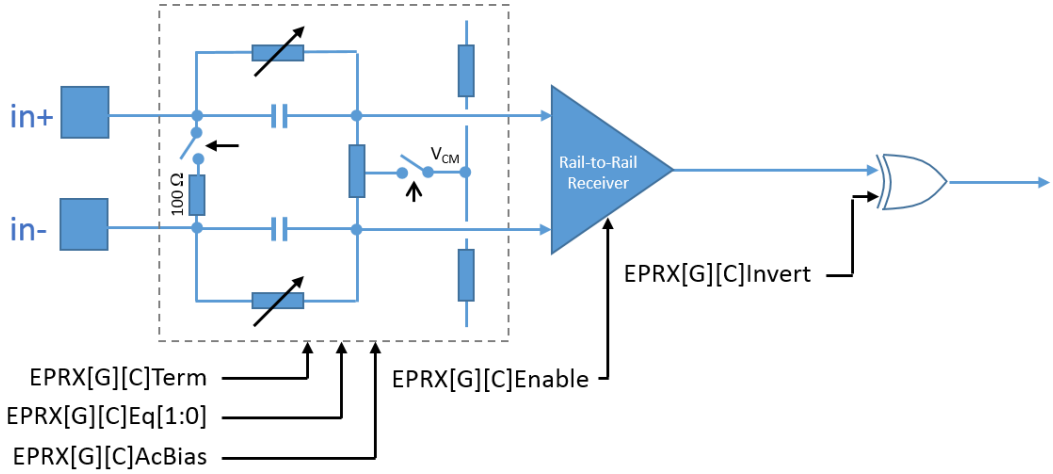

Figure 4: Receiver eLink

In both cases (transmitters and receivers), foreseen external capacitors can be mounted to provide the AC signaling via the IO lines. Otherwise, the board will be populated with 0-ohm resistors. Note that this must be decided when assembling the EMCI PCB and, due to the size of these SMD components, cannot be changed afterwards.

4.1.1.1 CERN Low Power Signaling (CLPS)

The eLinks use the adopted CERN standard called CLPS. Its main characteristics are:

- Link types:
  - Point-to-point.
  - Multi-drop transmitter.
- Maximum data rate:
  - 1.28 Gb/s (NRZ signaling).
- Maximum clock frequency:
  - 1.28 GHz.
- Programmable signaling level:
  - 100 mV to 400 mV (single-ended amplitude);
  - 200 mV to 800 mV (differential amplitude).
- Common mode voltage:
  - 600 mV (nominal, for 1.2 V supply voltage).
- Load impedance:
  - 100 Ohm differential.

4.1.2 High-speed link

The EMCI-lpGBT high-speed link uses the VTRx+ to transmit all the information from the FEs (eLinks, ADC's, I2C…) to/from the EMP. The downlink (FEs direction) uses a bandwidth of 2.56 Gb/s and the uplink (EMP direction) can be configured to use either 5.12 Gb/s or 10.24 Gb/s.

The main clock used by the lpGBT (40 MHz) is recovered directly from the downlink frames, so there is no need to add external clock source (note that this means that the EMCI cannot be configured to transmit data exclusively in uplink direction).

The high-speed link has Forward Error Correction (FEC) capability to detect and correct transmission errors. It also uses de-scrambling (and scrambling), as well as de-interleaving (and interleaving) techniques to improve Clock and Data Recovery (CDR). For more information about these topics, please see the lpGBT user manual, section 4.

4.1.3 Power

The EMCI is powered through the FMC connector (or through the auxiliary connector when debugging) and requires a voltage input of 5-12 V. Actual power consumption depends on the number of eLinks used, as well as the data rate, but some approximations have been made:

- The power consumption of the lpGBT with all eLinks enabled should not exceed 500 mW [3].
- The power consumption of the VTRx+ with all channels enabled should not exceed 254 mW [4].
- The EMCI should not exceed 1W of power, considering the lpGBT, VTRx+, other losses, etc.

The EMCI uses a FEASTMP module [5] to convert the input voltage to 2.5 V (used by the VTRx+) and a bPOL2V5 chipset [6] as a second stage that lowers it down to 1.2 V (used by the lpGBT and the VTRx+). Both devices have been designed at CERN and are radiation hard. Note that both voltages are available in the FMC connector as outputs for reference use only. No current should be drained from these pins.

4.1.4 Configuration

In order to operate the EMCI, the lpGBT and the VTRx+ (by means of the lpGBT) must be pre-configured. The lpGBT has a dedicated I2C slave interface, which is accessible either from the local auxiliary connector or the FMC connector (section 4.2.3) that is used for reading and writing all the registers. Note that this interface (I2C slave) is not to be confused with I2C master interface, driven by the lpGBT. Moreover, when correctly pre-configured, the lpGBT registers are also accessible via the high-speed link interface, making it possible for the EMP to configure the lpGBT directly.

It is possible to permanently store this configuration by means of e-fusing. This way, the lpGBT can restore the default values in the registers that allow configuration through the high-speed link after power cycling. In order to perform e-fusing operation (which can be executed only once), 2.5 V need to be provided to the lpGBT via local auxiliary connector.

The EMCI also uses several DIP switches to pre-configure the state of the lpGBT:

- MODE: this is used to configure the EMCI as duplex up/downlink or as simplex downlink (simplex uplink is not available), as well as choosing the data rate for the high-speed uplink (5.12 or 10.24 Gb/s) and the FEC encoding (FEC5 or FEC12). These parameters are programmable through the auxiliary connector too.
- ADDR: the position of the switches defines the lpGBT I2C address for the configuration.

- SC_I2C: this switch selects the interface through which the lpGBT shall be configured (local I2C slave or remote serial high-speed link). This selection is accessible via the auxiliary connector too.

4.2 Interfaces

4.2.1 Front End interface

In order to keep the PCB as simple and small as possible, all the signals going and coming from all the FEs and the power input to the EMCI are routed to a FMC (HPC) connector (10mm height version). Furthermore, given that each EMCI might be connected to a different set of FEs, a customized splitter board is used. This passive board is plugged into the EMCI with the FMC that can be HPC or LPC (having some of the features not available but still with basic functionality provided). To interface with the FEs, the splitter board separates all the signals through the set of pigtails according to the needs of each user (Figure 5).

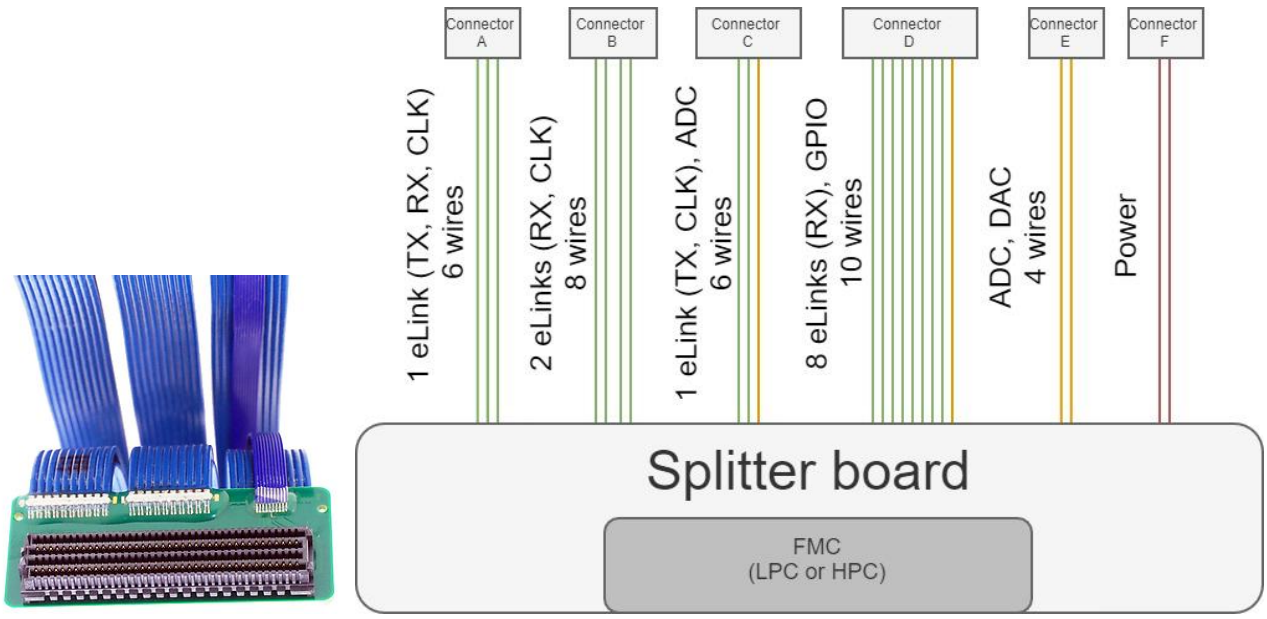

Figure 5: PCB with FMC connector and attached cables (left) and schematic example of a splitter board (right)

Some standard versions of the splitter board are available, but the user may design his own version to cover very specific needs.

The EMCI can be provided with a female FMC connector on the same side as the FEASTMP or with a male FMC connector on the opposite side. Having both connectors mounted is also possible, but only one should be used at the same time because they share the same signals.
This way it is possible to mount the splitter board as a mezzanine, right over the EMCI, or facing out. The EMCI can also be mounted directly onto a carrier.

The final pinout for the FMC connector is not yet defined and depends on the PCB routing. However, it is expected to be partially compatible with the FMC standard (VITA 57.1). All the power and GND assignments are respected, but in order to fit all the connections, some non-general-purpose pins are also used. Moreover, regardless of the behavior of the EMCI (as mezzanine or as a carrier), the pinout assignment and orientation (input or output) is not modified. This way the EMCI is pluggable into any carrier board that follows the standard without damaging any of the devices.

The guidelines for the pinout can be found in appendix 7.2.

4.2.2 Back end interface

The interface to the EMP uses the VL+ system [7]. The VTRx+ module is connected to the EMCI (pinout in appendix 0) and uses two multimode optic fiber channels (TX and RX) to transmit data between the EMP and the EMCI.

4.2.3 Configuration interface

In order to configure the lpGBT locally, a 14-pin AMP connector (5103308-2) is used (pinout in appendix 7.4). The following features are accessible through this connector:

- I2C connection for writing/reading the lpGBT registers
- Mode set for lpGBT
- E-fusing 2.5V
- FEASTMP enable/disable
- Reset line
- 1.2V output
- 5-12V input for power

5. 3D models

The presented 3D model is a sketch of the EMCI, lacking many small components, and may evolve in the future. The final layout will depend on the appropriate PCB signals routing following lpGBT guidelines and pinouts with all the components in place.

Approximate dimensions: 90x75mm

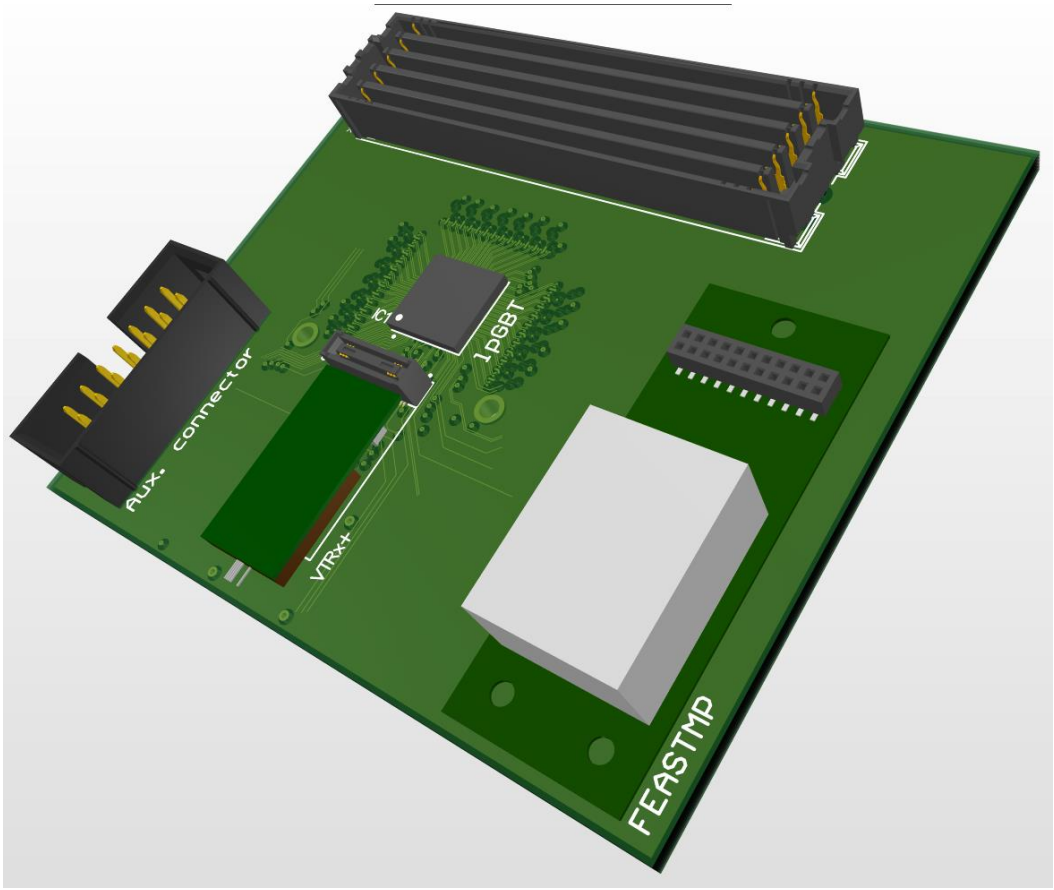

Figure 6: 3D model top side

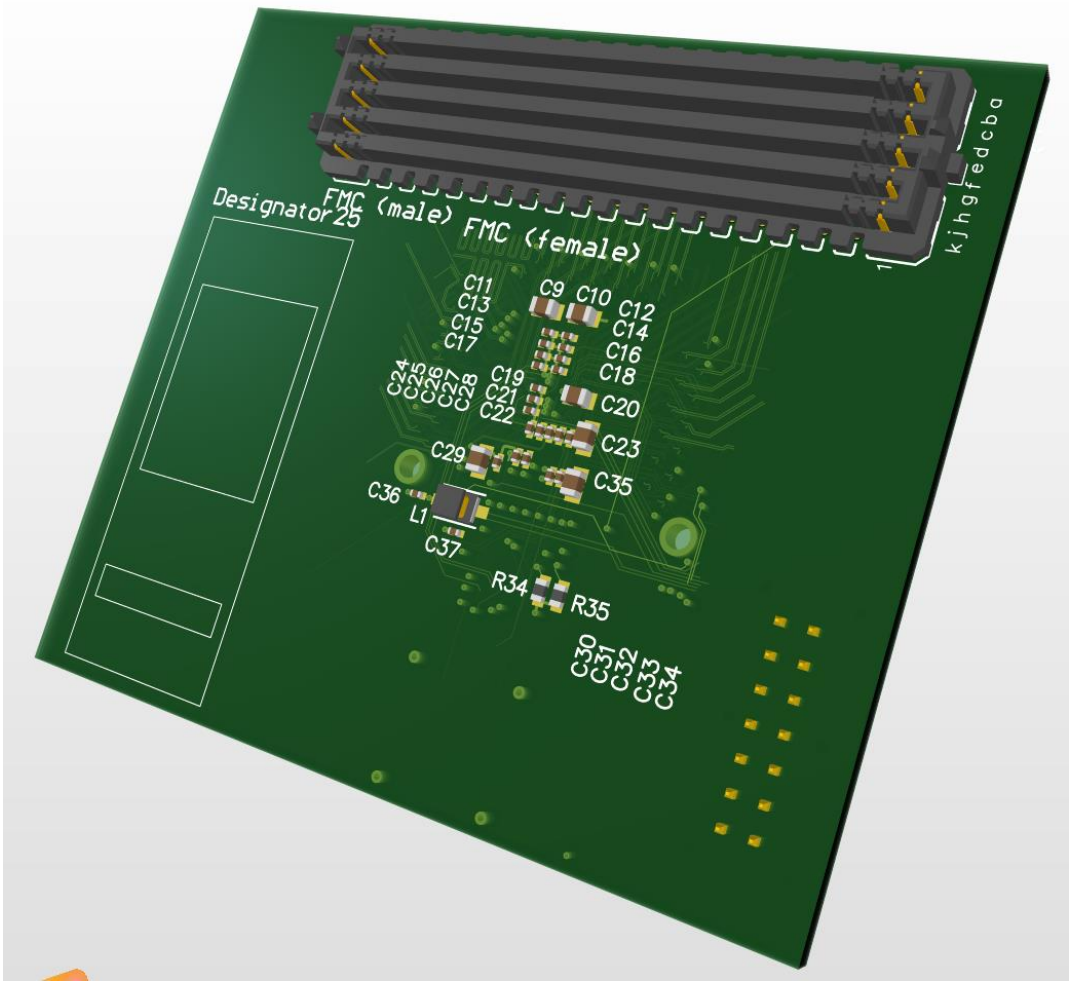

Figure 7: 3D model bottom side

One important factor that will determine the orientation of the FMC connector is the height of the tallest component on the top side (e.g. FEASTMP). In order to place the splitter board as a mezzanine over the FEASTMP, it must be shorter than the two FMC connected, considering also that this assembly has sufficient heat dissipation capability.

6. References

[1] K. Nicpon et al. The Embedded Local Monitor Board upgrade proposals. https://pos.sissa.it/343/034/pdf

[2] GBT Team. lpGBT manual. https://lpgbt.web.cern.ch/lpgbt/manual/

[3] P. Moreira. "The lpGBT: a radiation tolerant ASIC for Data, Timing, Trigger and Control Applications in HL-LHC". Topical Workshop on Electronics for Particle Physics, Sept. 2019

[4] J. Troska. Versatile Link+ Transceiver (VTRx+). Technical Specification, part 2.1. https://edms.cern.ch/ui/file/1719329/1/VTRxPlus_spec.pdf

[5] DCDC converters team. FEASTMP Datasheet. http://project-dcdc.web.cern.ch/project-DCDC/public/Documents/FEAST2Mod_Datasheet_gb2016.pdf

[6] DCDC converters team. bPOL2V5_V2.2 Datasheet. http://project-dcdc.web.cern.ch/project-DCDC/public/Documents/bPOL2V5_V2.2%20datasheet%20rev4.pdf

[7] J. Troska, C. Soos, L. Olanterä. The Versatile Link+ Application Note. https://edms.cern.ch/ui/file/2149674/1/VTRxPlusApplicationNote.pdf

7. Appendix

7.1 Schematics

7.2 FMC pin assignments

Example of pin assignment of the FMC connector is shown in Table 4 and Table 5. The tables show for each row (A to K) and number (1 to 40) the VITA standard pin name (left column) and the corresponding assignments for the EMCI (right column). Note that rows C, D, G and H correspond to LPC. Final pin assignments depend on PCB routing.

	K		J		H		G		F	
	Standard	EMCI	Standard	EMCI	Standard	EMCI	Standard	EMCI	Standard	EMCI
	HPC		HPC		LPC		LPC		HPC	
1	VREF_B_M2C	+2.5V Ref	GND	GND	VREF_A_M2C	+1.2V Ref	GND	GND	PG_M2C	
2	GND	GND	CLK3_M2C_P		PRSNT_M2C_L	GND	CLK1_M2C_P		GND	GND
3	GND	GND	CLK3_M2C_N		GND	GND	CLK1_M2C_N		GND	GND
4	CLK2_M2C_P		GND	GND	CLK0_M2C_P		GND	GND	HA00_P_CC	ELINK_CLK_P11
5	CLK2_M2C_N		GND	GND	CLK0_M2C_N		GND	GND	HA00_N_CC	ELINK_CLK_N11
6	GND	GND	HA03_P	ELINK_OUT_P8	GND	GND	LA00_P_CC	ELINK_IN_P4	GND	GND
7	HA02_P	ADC4	HA03_N	ELINK_OUT_N8	LA02_P	GPIO0	LA00_N_CC	ELINK_IN_N4	HA04_P	ELINK_IN_P12
8	HA02_N	ADC5	GND	GND	LA02_N	GPIO1	GND	GND	HA04_N	ELINK_IN_N12
9	GND	GND	HA07_P	ELINK_OUT_P9	GND	GND	LA03_P	ELINK_IN_P5	GND	GND
10	HA06_P	ADC6	HA07_N	ELINK_OUT_N9	LA04_P	GPIO2	LA03_N	ELINK_IN_N5	HA08_P	ELINK_IN_P13
11	HA06_N	ADC7	GND	GND	LA04_N	GPIO3	GND	GND	HA08_N	ELINK_IN_N13
12	GND	GND	HA11_P	ELINK_OUT_P10	GND	GND	LA08_P	ELINK_IN_P6	GND	GND
13	HA10_P	PSCLK_P0	HA11_N	ELINK_OUT_N10	LA07_P	GPIO4	LA08_N	ELINK_IN_N6	HA12_P	ELINK_IN_P14
14	HA10_N	PSCLK_N0	GND	GND	LA07_N	GPIO5	GND	GND	HA12_N	ELINK_IN_N14
15	GND	GND	HA14_P	ELINK_OUT_P11	GND	GND	LA12_P	ELINK_IN_P7	GND	GND
16	HA17_P_CC	PSCLK_P1	HA14_N	ELINK_OUT_N11	LA11_P	GPIO6	LA12_N	ELINK_IN_N7	HA15_P	ELINK_IN_P15
17	HA17_N_CC	PSCLK_N1	GND	GND	LA11_N	GPIO7	GND	GND	HA15_N	ELINK_IN_N15
18	GND	GND	HA18_P	ELINK_IN_P8	GND	GND	LA16_P	ELINK_CLK_P4	GND	GND
19	HA21_P	PSCLK_P2	HA18_N	ELINK_IN_N8	LA15_P	ELINK_IN_P2	LA16_N	ELINK_CLK_N4	HA19_P	ELINK_CLK_P12
20	HA21_N	PSCLK_N2	GND	GND	LA15_N	ELINK_IN_N2	GND	GND	HA19_N	ELINK_CLK_N12
21	GND	GND	HA22_P	ELINK_IN_P9	GND	GND	LA20_P	ELINK_CLK_P5	GND	GND
22	HA23_P	PSCLK_P3	HA22_N	ELINK_IN_N9	LA19_P	ELINK_IN_P3	LA20_N	ELINK_CLK_N5	HB02_P	ELINK_CLK_P13
23	HA23_N	PSCLK_N3	GND	GND	LA19_N	ELINK_IN_N3	GND	GND	HB02_N	ELINK_CLK_N13
24	GND	GND	HB01_P	ELINK_IN_P10	GND	GND	LA22_P	ELINK_CLK_P6	GND	GND
25	HB00_P_CC	GPIO8	HB01_N	ELINK_IN_N10	LA21_P	ELINK_CLK_P2	LA22_N	ELINK_CLK_N6	HB04_P	ELINK_CLK_P14
26	HB00_N_CC	GPIO9	GND	GND	LA21_N	ELINK_CLK_N2	GND	GND	HB04_N	ELINK_CLK_N14
27	GND	GND	HB07_P	ELINK_IN_P11	GND	GND	LA25_P	ELINK_CLK_P7	GND	GND
28	HB06_P_CC	GPIO10	HB07_N	ELINK_IN_N11	LA24_P	ELINK_CLK_P3	LA25_N	ELINK_CLK_N7	HB08_P	ELINK_CLK_P15
29	HB06_N_CC	GPIO11	GND	GND	LA24_N	ELINK_CLK_N3	GND	GND	HB08_N	ELINK_CLK_N15
30	GND	GND	HB11_P	ELINK_CLK_P8	GND	GND	LA29_P	ELINK_OUT_P5	GND	GND
31	HB10_P	GPIO12	HB11_N	ELINK_CLK_N8	LA28_P	ELINK_OUT_P2	LA29_N	ELINK_OUT_N5	HB12_P	SLOW_ELINK_IN_P
32	HB10_N	GPIO13	GND	GND	LA28_N	ELINK_OUT_N2	GND	GND	HB12_N	SLOW_ELINK_IN_P
33	GND	GND	HB15_P	ELINK_CLK_P9	GND	GND	LA31_P	ELINK_OUT_P6	GND	GND
34	HB14_P	GPIO14	HB15_N	ELINK_CLK_N9	LA30_P	ELINK_OUT_P3	LA31_N	ELINK_OUT_N6	HB16_P	SLOW_ELINK_OUT_P
35	HB14_N	GPIO15	GND	GND	LA30_N	ELINK_OUT_N3	GND	GND	HB16_N	SLOW_ELINK_OUT_P
36	GND	GND	HB18_P	ELINK_CLK_P10	GND	GND	LA33_P	ELINK_OUT_P7	GND	GND
37	HB17_P_CC	RSTOUTB	HB18_N	ELINK_CLK_N10	LA32_P	ELINK_OUT_P4	LA33_N	ELINK_OUT_N7	HB20_P	SLOW_ELINK_CLK_P
38	HB17_N_CC		GND	GND	LA32_N	ELINK_OUT_N4	GND	GND	HB20_N	SLOW_ELINK_CLK_P
39	GND	GND	VIO_B_M2C		GND	GND	VADJ		GND	GND
40	VIO_B_M2C		GND	GND	VADJ		GND	GND	VADJ	

Table 4: VITA 5.12 standard and FMC pinout (rows K to F)

E		D		C		B		A	
Standard	EMCI	Standard	EMCI	Standard	EMCI	Standard	EMCI	Standard	EMCI
HPC		LPC		LPC		HPC		HPC	
GND	GND	PG_C2M		GND	GND	RES1		GND	GND
HA01_P_CC	ELINK_IN_P16	GND	GND	DP0_C2M_P	ELINK_IN_P20	GND	GND	DP1_M2C_P	ELINK_CLK_P21
HA01_N_CC	ELINK_IN_N16	GND	GND	DP0_C2M_N	ELINK_IN_N20	GND	GND	DP1_M2C_N	ELINK_CLK_N21
GND	GND	GBTCLK0_M2C_P		GND	GND	DP9_M2C_P		GND	GND
GND	GND	GBTCLK0_M2C_N		GND	GND	DP9_M2C_N		GND	GND
HA05_P	ELINK_IN_P17	GND	GND	DP0_M2C_P	ELINK_CLK_P20	GND	GND	DP2_M2C_P	ELINK_CLK_P22
HA05_N	ELINK_IN_N17	GND	GND	DP0_M2C_N	ELINK_CLK_N20	GND	GND	DP2_M2C_N	ELINK_CLK_N22
GND	GND	LA01_P_CC	I2C_SLAVE_SCL_0	GND	GND	DP8_M2C_P		GND	GND
HA09_P	ELINK_IN_P18	LA01_N_CC	I2C_SLAVE_SDA_0	GND	GND	DP8_M2C_N		GND	GND
HA09_N	ELINK_IN_N18	GND	GND	LA06_P	ADC0	GND	GND	DP3_M2C_P	ELINK_CLK_P23
GND	GND	LA05_P	ELINK_OUT_P0	LA06_N	ADC1	GND	GND	DP3_M2C_N	ELINK_CLK_N23
HA13_P	ELINK_IN_P19	LA05_N	ELINK_OUT_N0	GND	GND	DP7_M2C_P	ELINK_CLK_P27	GND	GND
HA13_N	ELINK_IN_N19	GND	GND	GND	GND	DP7_M2C_N	ELINK_CLK_N27	GND	GND
GND	GND	LA09_P	ELINK_OUT_P1	LA10_P	ADC2	GND	GND	DP4_M2C_P	ELINK_CLK_P24
HA16_P	ELINK_CLK_P16	LA09_N	ELINK_OUT_N1	LA10_N	ADC3	GND	GND	DP4_M2C_N	ELINK_CLK_N24
HA16_N	ELINK_CLK_N16	GND	GND	GND	GND	DP6_M2C_P	ELINK_CLK_P26	GND	GND
GND	GND	LA13_P	ELINK_IN_P0	GND	GND	DP6_M2C_N	ELINK_CLK_N26	GND	GND
HA20_P	ELINK_CLK_P17	LA13_N	ELINK_IN_N0	LA14_P	I2C_MASTER_SCL_0	GND	GND	DP5_M2C_P	ELINK_CLK_P25
HA20_N	ELINK_CLK_N17	GND	GND	LA14_N	I2C_MASTER_SDA_0	GND	GND	DP5_M2C_N	ELINK_CLK_N25
GND	GND	LA17_P_CC	ELINK_IN_P1	GND	GND	GBTCLK1_M2C_P		GND	GND
HB03_P	ELINK_CLK_P18	LA17_N_CC	ELINK_IN_N1	GND	GND	GBTCLK1_M2C_N		GND	GND
HB03_N	ELINK_CLK_N18	GND	GND	LA18_P_CC	I2C_MASTER_SCL_1	GND	GND	DP1_C2M_P	ELINK_IN_P21
GND	GND	LA23_P	ELINK_CLK_P0	LA18_N_CC	I2C_MASTER_SDA_1	GND	GND	DP1_C2M_N	ELINK_IN_N21
HB05_P	ELINK_CLK_P19	LA23_N	ELINK_CLK_N0	GND	GND	DP9_C2M_P		GND	GND
HB05_N	ELINK_CLK_N19	GND	GND	GND	GND	DP9_C2M_N		GND	GND
GND	GND	LA26_P	ELINK_CLK_P1	LA27_P	DAC	GND	GND	DP2_C2M_P	ELINK_IN_P22
HB09_P	ELINK_OUT_P12	LA26_N	ELINK_CLK_N1	LA27_N	SC_I2C	GND	GND	DP2_C2M_N	ELINK_IN_N22
HB09_N	ELINK_OUT_N12	GND	GND	GND	GND	DP8_C2M_P		GND	GND
GND	GND	TCK		GND	GND	DP8_C2M_N		GND	GND
HB13_P	ELINK_OUT_P13	TDI		SCL		GND	GND	DP3_C2M_P	ELINK_IN_P23
HB13_N	ELINK_OUT_N13	TDO		SDA		GND	GND	DP3_C2M_N	ELINK_IN_N23
GND	GND	3P3VAUX		GND	GND	DP7_C2M_P	ELINK_IN_P27	GND	GND
HB19_P	ELINK_OUT_P14	TMS		GND	GND	DP7_C2M_N	ELINK_IN_N27	GND	GND
HB19_N	ELINK_OUT_N14	TRST_L		GA0		GND	GND	DP4_C2M_P	ELINK_IN_P24
GND	GND	GA1		12P0V	+12V Input	GND	GND	DP4_C2M_N	ELINK_IN_N24
HB21_P	ELINK_OUT_P15	3P3V		GND	GND	DP6_C2M_P	ELINK_IN_P26	GND	GND
HB21_N	ELINK_OUT_N15	GND	GND	12P0V	+12V Input	DP6_C2M_N	ELINK_IN_N26	GND	GND
GND	GND	3P3V		GND	GND	GND	GND	DP5_C2M_P	ELINK_IN_P25
VADJ		GND	GND	3P3V		GND	GND	DP5_C2M_N	ELINK_IN_N25
GND	GND	3P3V		GND	GND	RES0		GND	GND

Table 5: VITA 5.12 standard and FMC pinout (rows E to A)

7.3 VTRx+ pin assignments

VTRx+ connector pinout in PCB:

Pin #	Name	Description	Pin #	Name	Description
1	VCCR2V5	2.5V Power supply for TIA	2	n/c	
3	VCCR2V5	2.5V Power supply for TIA	4	RSSI	RSSI current output from TIA, to be pulled up via a resistor to VCCR2V5
5	GND	Ground	6	GND	Ground
7	RXN	Rx $\overline{\text{output}}$	8	SDA	I2C data (to be pulled-up to VCCT1V2)
9	RXP	Rx output	10	SCL	I2C clock (to be terminated to VCCT1V2)
11	GND	Ground	12	GND	Ground
13	TX1N	Tx Ch.1 $\overline{\text{input}}$	14	RSTN	Laser Driver Reset
15	TX1P	Tx Ch.1 input	16	DIS	Laser Driver Disable
17	GND	Ground	18	GND	Ground
19	TX2N	Tx Ch.2 $\overline{\text{input}}$	20	n/c	
21	TX2P	Tx Ch.2 input	22	n/c	
23	GND	Ground	24	GND	Ground
25	TX3N	Tx Ch.3 $\overline{\text{input}}$	26	n/c	
27	TX3P	Tx Ch.3 input	28	n/c	
29	GND	Ground	30	GND	Ground
31	TX4N	Tx Ch.4 $\overline{\text{input}}$	32	TH1	10k Thermistor Terminal 1
33	TX4P	Tx Ch.4 input	34	TH2	10k Thermistor Terminal 2
35	GND	Ground	36	GND	Ground
37	VCCT2V5	2.5V Power supply for Laser Driver	38	VCCT1V2	1.2V Power supply for Laser Driver
39	VCCT2V5	2.5V Power supply for Laser Driver	40	VCCT1V2	1.2V Power supply for Laser Driver

Table 6: VTRx+ connector pinout

7.4 Auxiliary connector pin assignments

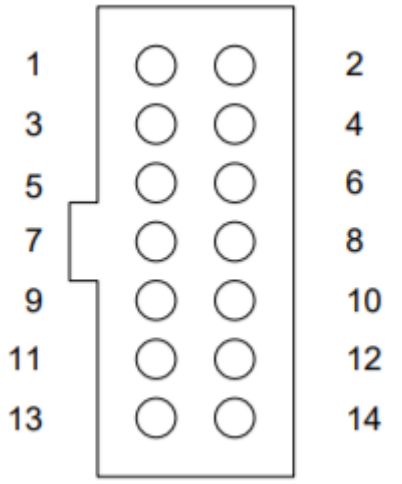

Figure 8: Auxiliary connector schematics

Pin #	Name	Description
1	MODE0	lpGBT mode selection
2	SCL	lpGBT I2C slave communication clock line
3	MODE1	lpGBT mode selection
4	SDA	lpGBT I2C slave communication data line
5	MODE2	lpGBT mode selection
6	GND	Ground
7	DCDC EN	FEASTMP module enable
8	1.2V OUT	1.2V output
9	MODE3	lpGBT mode selection
10	RST	lpGBT reset
11	2.5V IN	lpGBT 2.5V input for e-fusing
12	GND	Ground
13	12V IN	12V input power
14	GND	Ground

Table 7: Auxiliary connector pinout