# WP6: Novel high voltage and resistive CMOS sensors

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# Outline

- Introduction to depleted CMOS devices
- Recapitulation of WP6 program and activities
- Early days: hybrid CMOS devices
- New path: Depleted Monolithic Active Pixel Sensors (DMAPS)
- From early prototypes to proven performance (selection of results*)
  - First HVCMOS devices: the challenge
  - Another approach: smaller electrodes
  - Beyond tracking
- Conclusions
- The future of DMAPS (AIDAinnova)

* Apologies if I missed your favourite result

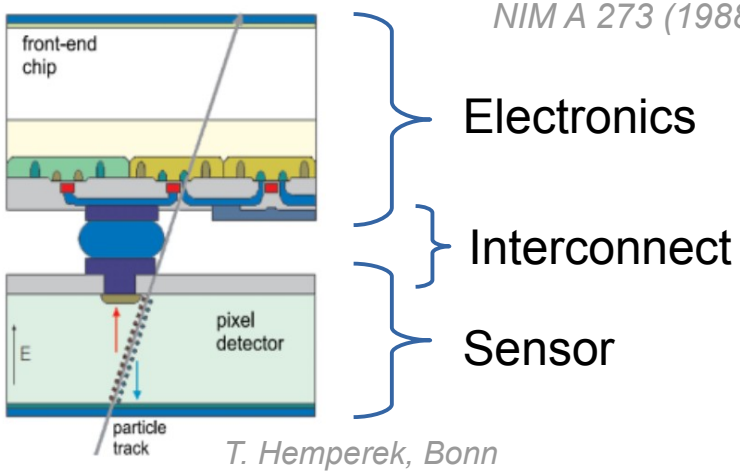
** Note: slides summarize work done within AIDA (in particular included in AIDA publications, ie **not** a DMAPS review)

# Introduction

- Innermost layers of HEP accelerator-based experiments require:
  - **Position resolution,** radiation hardness, rate capability, compactness, low material budget...
- Technology of choice: **silicon pixel sensors**

## Hybrid detectors

*E.H.M. Heijne et al., NIM A 273 (1988) 615*

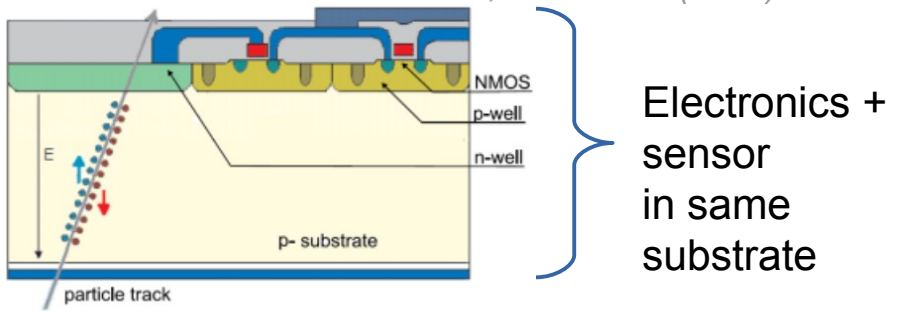



*T. Hemperek, Bonn*

- Standard in current experiments
- Design allows for optimization of electronics and sensor

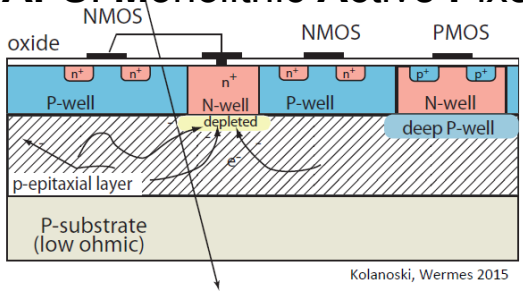
## Monolithic detectors

*S. Parker, NIM A 275 (1989) 494*




- Less material, less complexity
- Smaller pixel possible

- Initially on ρ-low under-depleted bulk
- **MAPS**: **M**onolithic **A**ctive **P**ixel **S**ensor



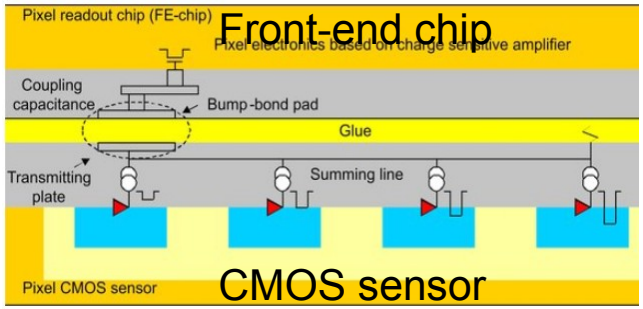

*R. Turchetta et al. Sensors (2008)*

**Goal of WP6**: Exploration of an innovative tracking-detector technology based on **depleted** CMOS sensors

*I. Peric et al., NIM A 582 (2007) 876*

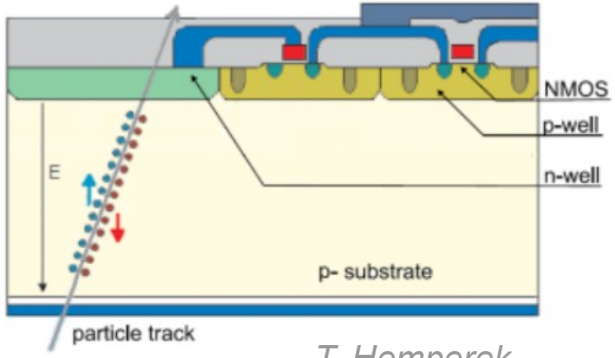
# Recapitulation of WP6 program and activities

- **Goal of WP6**: Exploration of an innovative tracking-detector technology based on active CMOS sensors
- Initially, the focus of the activities were to investigate **AC coupled devices**
  - The reasons behind this approach:
    - AC coupling simpler (lower cost)
    - Full monolithic devices “too complicated”
    - (longer timescale)




*I. Peric*

- However, though hybrid CMOS devices were fabricated within the WP6 activities, the process was rather complicated
- In parallel, quick progress was made on **monolithic devices** (together with very encouraging results)
  - One substrate + no hybridization!
  - (less material, smaller pixels – no bumps,
  - lower cost)

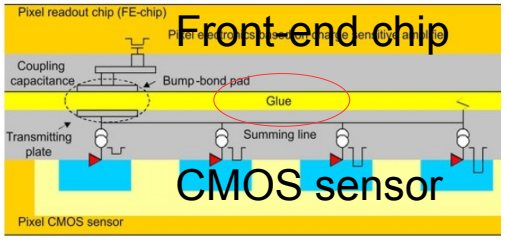


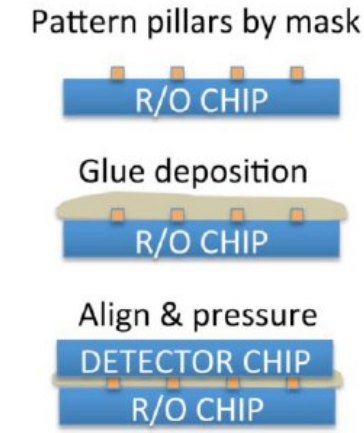

*T. Hemperek*

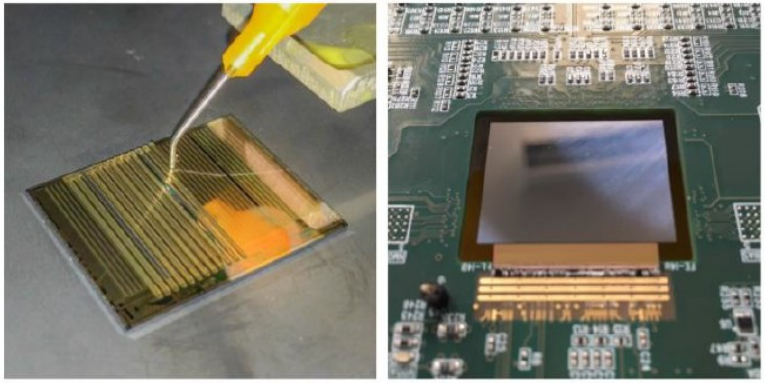
*Progress on DMAPS main result of WP6* → Task 6.3 Sensor development

# Hybrid CMOS Devices I

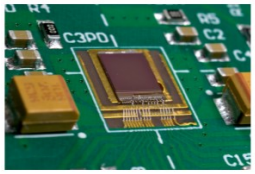
- **AC coupled devices**
  - "Simple" glue dispensing and "pick and
  - place" procedure: not uniform couplings
  - Improved approach with "pillars"
  - Many prototypes produced and their performance
  - before and after irradiation measured
    - 99.7% hit efficiency after 1E15 neq/cm2
    - However, fabrication process complicated
    - *No* advantage over standard hybrid devices



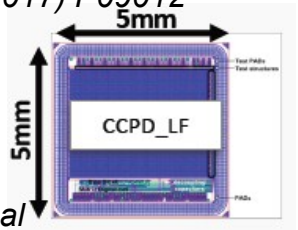



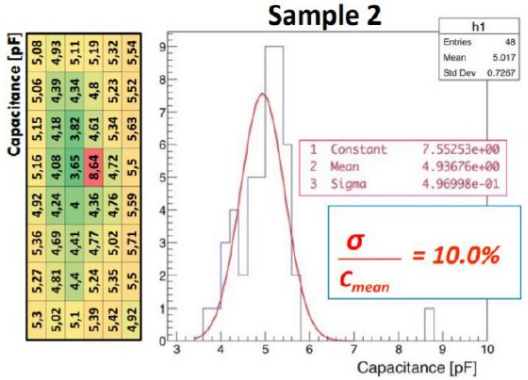
M. Benoit et al., JINST 13 (2018) P02011



I. Kremastiotis et al., JINST 12 (2017) P09012



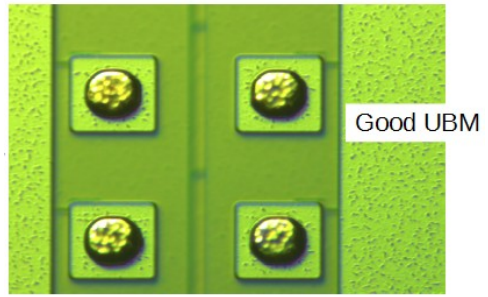

L. Vigani et al 2018 JINST 13 C02021

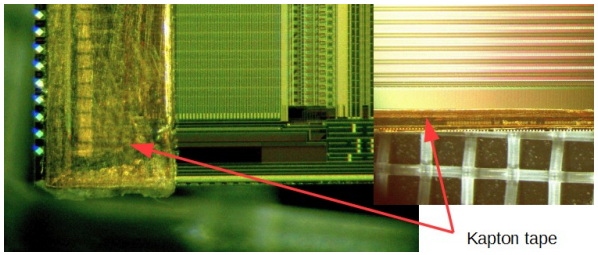



Difficult to achieve uniformity

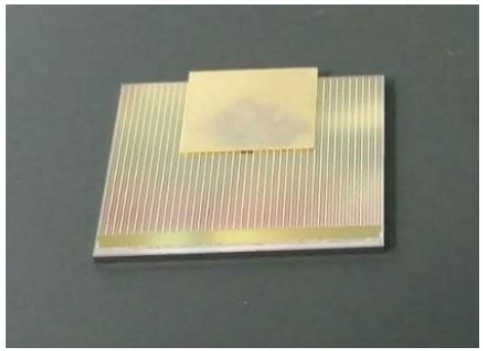
# Hybrid CMOS Devices II

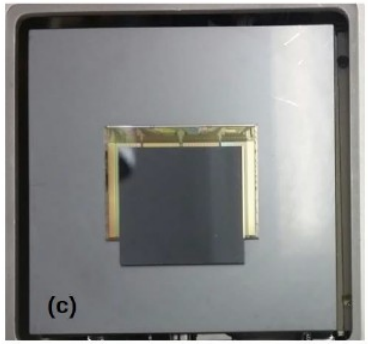
- **AC/DC coupled devices**
  - Combine DC and AC coupling to ensure
  - uniformity
  - Prototypes “investigators” produced
  - Metalization of pads in single tiles (CMOS devices) needed
    - Protection of wire-bonding pads
  - Selective removal of bumps in front-end (FEI4)
  - Flip-chip process

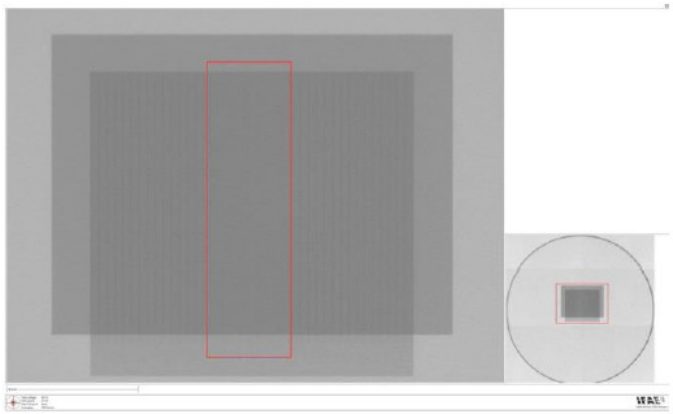



*Several devices fabricated, but process complicated: no advantage over standard hybrid devices*



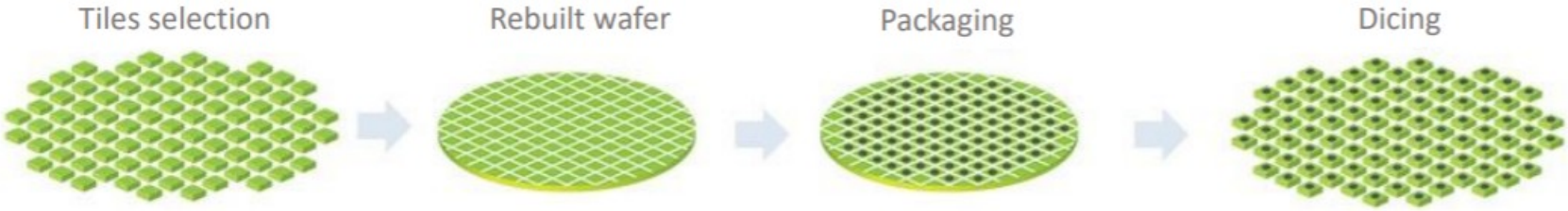


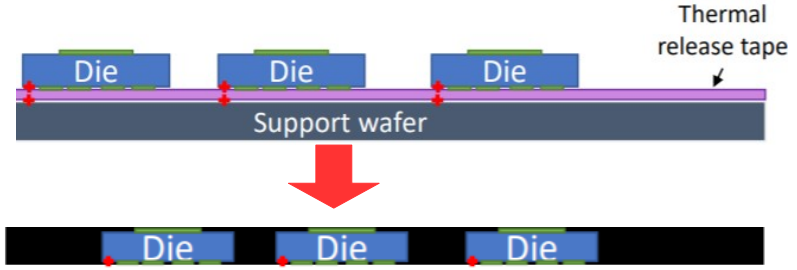
*AIDA-2020-D6.6 report*

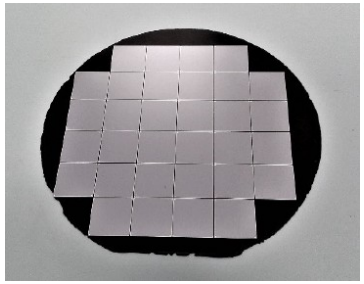
# Hybrid CMOS Devices III

- **Wafer Level Packaging (WLP)**
  - One problem with CMOS hybrid devices is the fabrication of large sensors, due to reticle limit ~4cm$^2$ (stitching is one option)
  - WLP allows to select good tiles and "reconstruct" wafer for further processing




  - Technology also potentially promising for standard hybrid devices (with "low" yield technologies – eg 3D sensors)
    - Could avoid UBM process of bad sensors (cost saving)
  - Tests showed that **bows about 100µm** could be achieved, **but** position needed improvement for further photolithography steps



MicroFabSolutions

*AIDA-2020-D6.7 report*

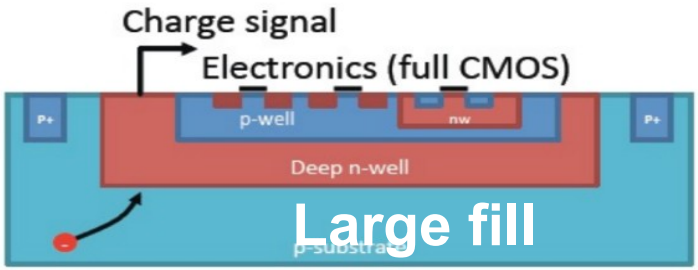
# Depleted Monolithic Devices

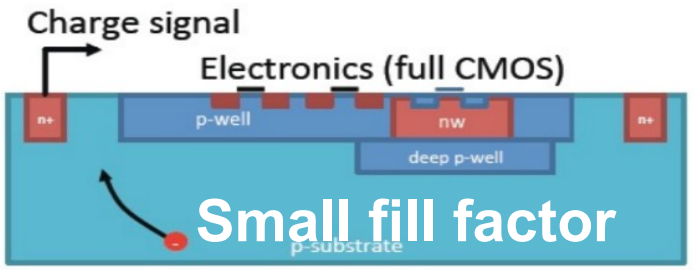
- **HL-LHC** is a **harsh radiation environment** (~1E16 $n_{eq}/cm^2$, 500 Mrad)
- For CMOS devices need higher radiation harness: **depleted substrates**
  - High voltage or high resistivity approach (HV/HR-CMOS)

    *I. Peric et al., NIM A 582 (2007) 876 (non-AIDA)*

$$d \sim \sqrt{\rho \cdot V}$$

*Two approaches to depleted-CMOS*




- Electronics **inside** n-well
  - Full CMOS inside
  - Large collection node
  - Shorter drift distances (more rad hard)

**Cons**

- Higher noise or power
- (larger capacitance)

- Electronics **outside** n-well
  - Full CMOS inside
  - Small collection node
  - Small capacitance (less noise & power)

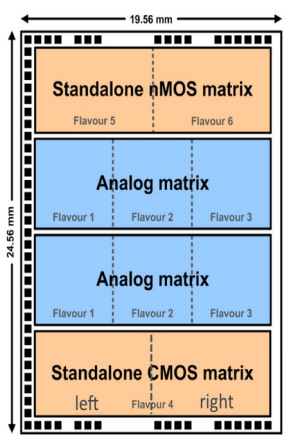
**Cons**

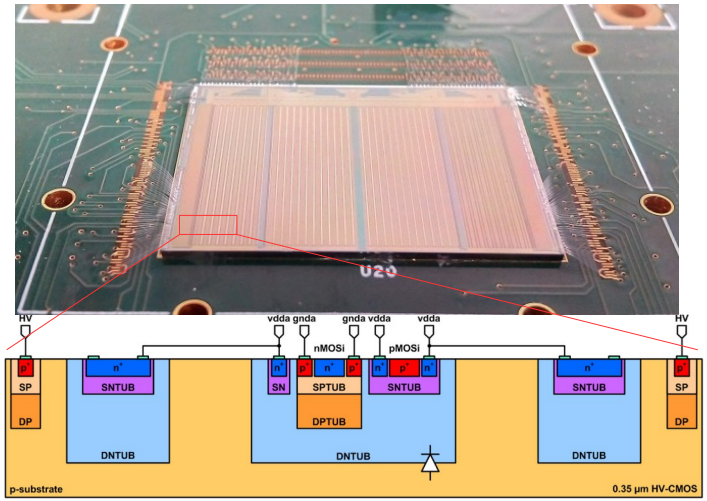
- Potential lower radiation hardness (larger drift)

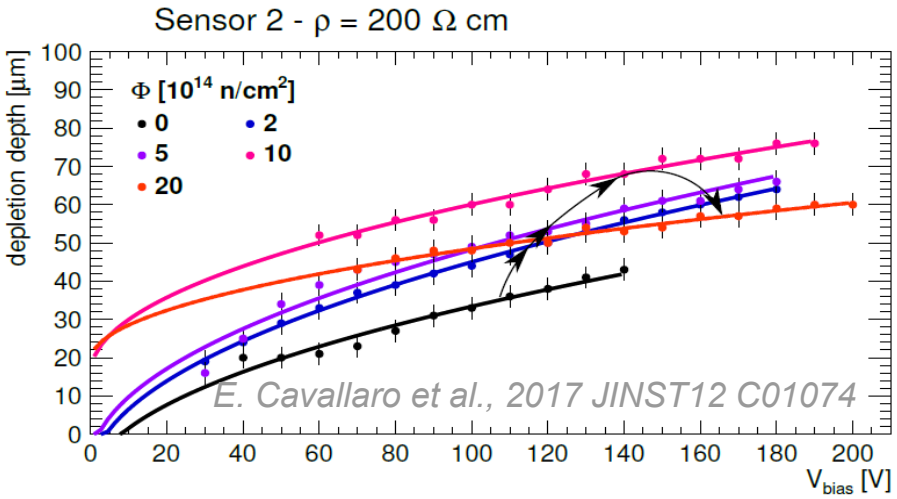
# Depleted CMOS: First Prototypes

**H35demo**: early full size (~2x2cm$^2$) investigator with large fill factor

- AMS 350 nm HV-CMOS
- 50x250 µm$^2$ pixels
- Two monolithic and two analog-only matrices (for AC coupling)
- Resistivity: 20-80-200-1000 Ωcm
- Pixel: CSA + Discr/2$^{nd}$ Ampl

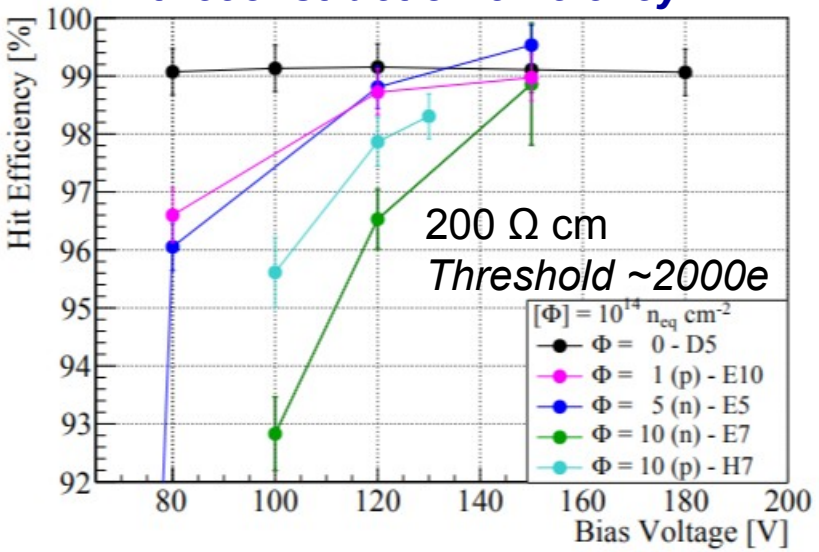



- Good efficiency after 1E15 neq/cm2
- **However**, 350 mW/cm2

***Hit reconstruction efficiency***

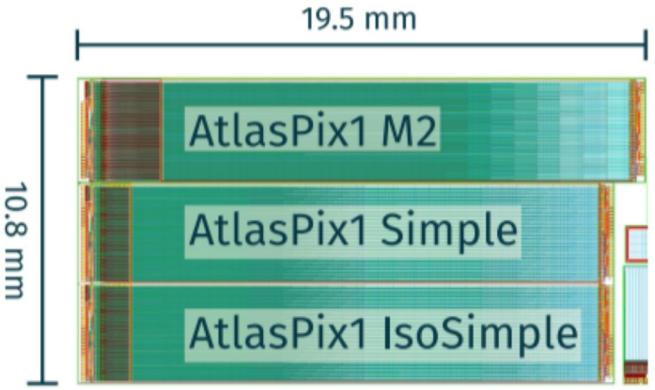


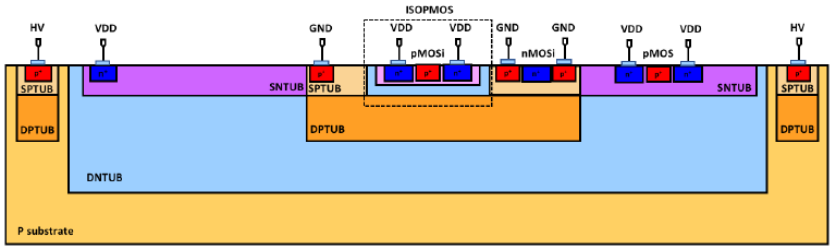

*S. Terzo et al 2019 JINST 14 P02016*

# Depleted CMOS: Large Electrodes

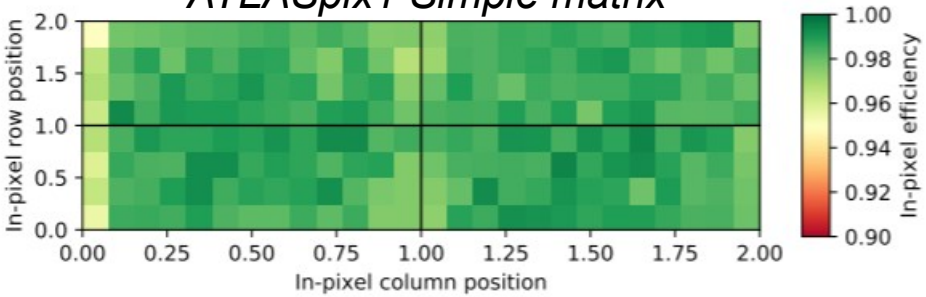
**ALTASpix1**: large size prototype with large fill factor

- AMS 180 nm HV-CMOS process
- 130 x 40 µm² (M2: 60 x 50 µm²) pixels
- Three flavours: simple (nMOS transistors), IsoSimple (CMOS) and M2 (triggered readout)
- Similar to to column-drain readout
- Resistivity: 20-80-200-1000 Ωcm




*ATLASpix1 Simple matrix*




99.5% after 1E15 neq/cm2 (n)

*F. Ehrler et al., NIM A 936 (2019) 654-656*
*M. Kiehn et al 2019 JINST 14 C08013 (non-AIDA)*

- Very good results after irradiation
  - At 80V and threshold ~1000e
  - Up to **2E15 neq/cm2** (n)
- Power dissipation <150 mW/cm²


ATLASpix3:

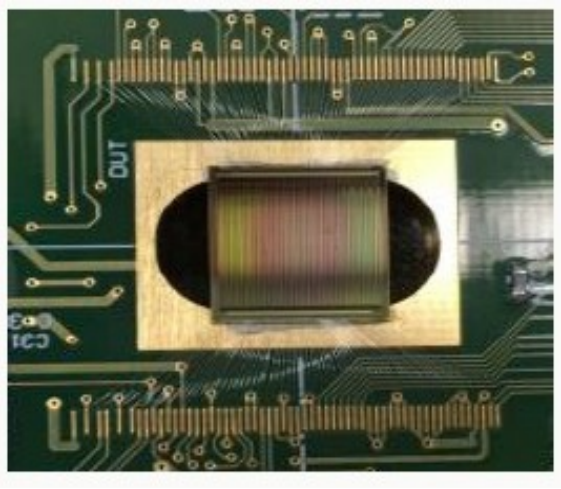
- TSI 180 nm
- 50 x 150 µm² pixels
- Compatible with RD53 readout

*R. Schimassek et al, TWEPP 2019*

# Depleted CMOS: Large Electrodes

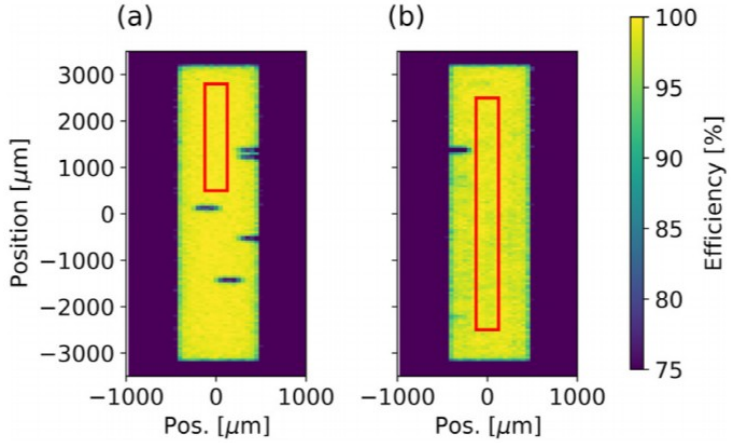
**LF-Monopix**: large size prototype with large fill factor

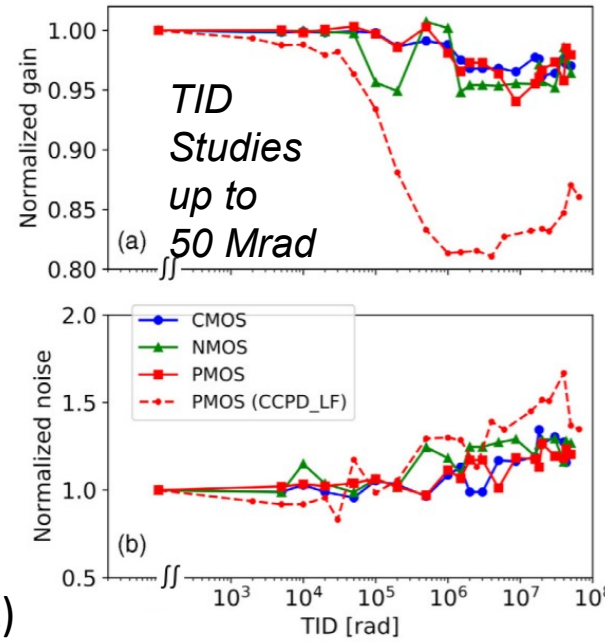
- LFoundry 150 nm process
- 50 x 250 µm² pixels
- Resistivity > 2000 Ωcm
- Thickness: 750, 200, 100 µm
  - Backside processing for full depletion
- Column-drain readout




10 mm x 10 mm

*T. Hirono et al., NIMA 924 (2019) 87*



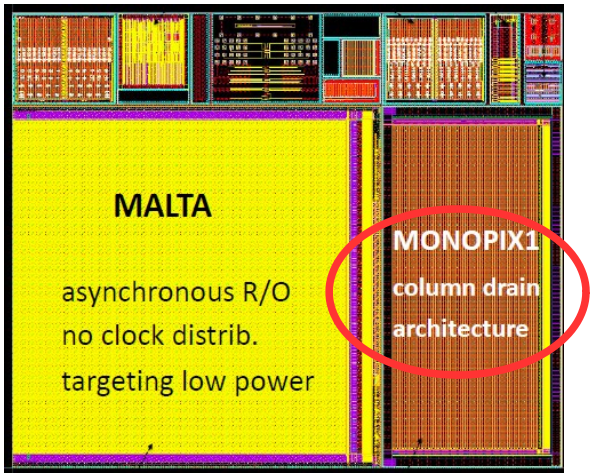




- Results at 130 V and 1700 e threshold
- 98.9% hit reconstruction efficiency (1E15 neq/cm²)
- LFMonopix2 (50 x 150 µm²) recently submitted (tbc)

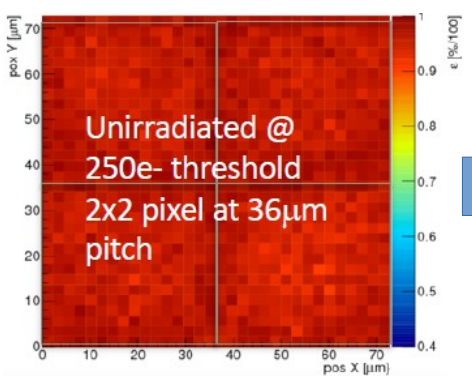
# Depleted CMOS: Small Electrodes

**TJ-Monopix:** small electrode prototype

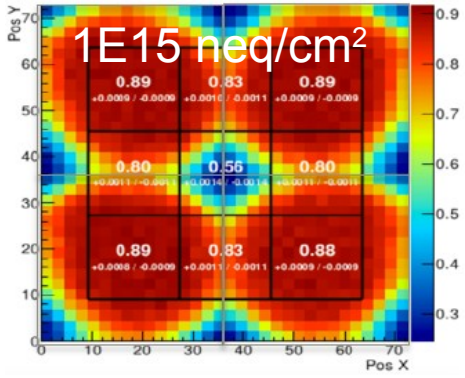
- TowerJazz 180 nm CMOS CIS
- Full CMOS in pixel
- 36 x 40 µm$^2$ pixels
- Epi thickness: 20 – 30 µm
- Resistivity: 1 kΩ cm
- **Modified process** to improve lateral depletion
  - See next slide



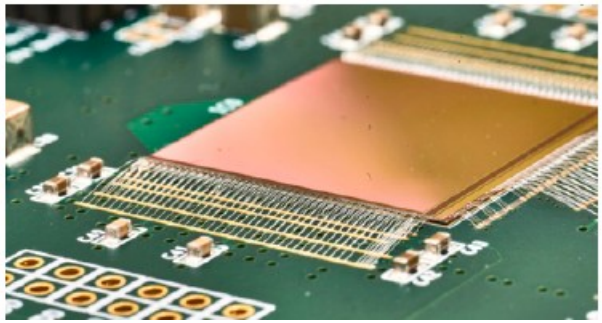

8 mm x 18 mm




*350e threshold*




*570e threshold*



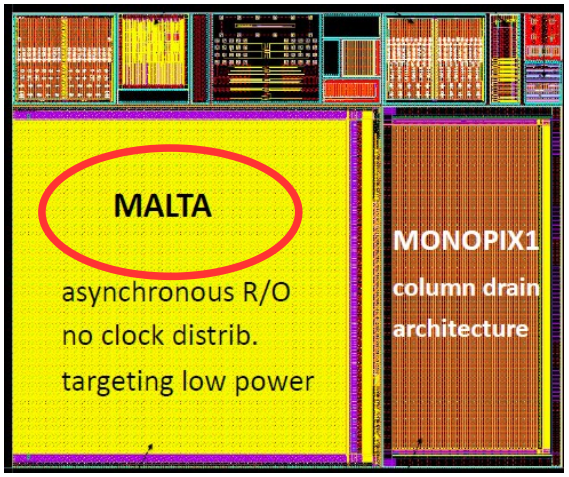
*I. Caicedo et al., JINST 14 (2019) C06006*
*N. Wemes, CERN Seminar 2020*

- Low threshold, low noise and low power dissipation (3µW/pixel)...
- Irradiation results (to 1E15neq/cm$^2$) showed some loss of efficiency in corners
  - Add p-implant to improve transverse E field, higher resistive substrates,... (TJ-Monopix2, MALTA next slides)

# Depleted CMOS: Small Electrodes

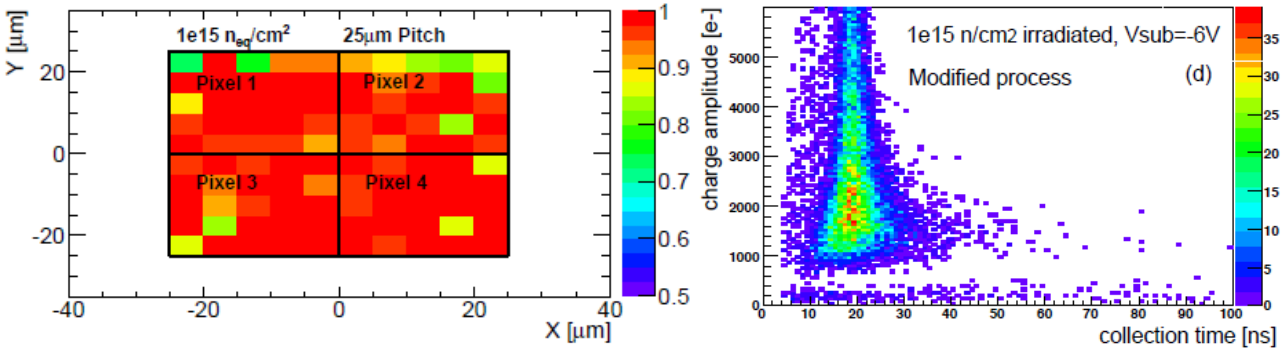
## MALTA

- TowerJazz 180 nm CMOS CIS
- Full CMOS in pixel
- 25 x 25 μm² (and other sizes) pixels
- Epi thickness: 20 – 30 μm
- High resistivity: 1-8 kΩ cm
- **Modified process*** to improve lateral depletion
  - Derived from ALICE development (CERN)

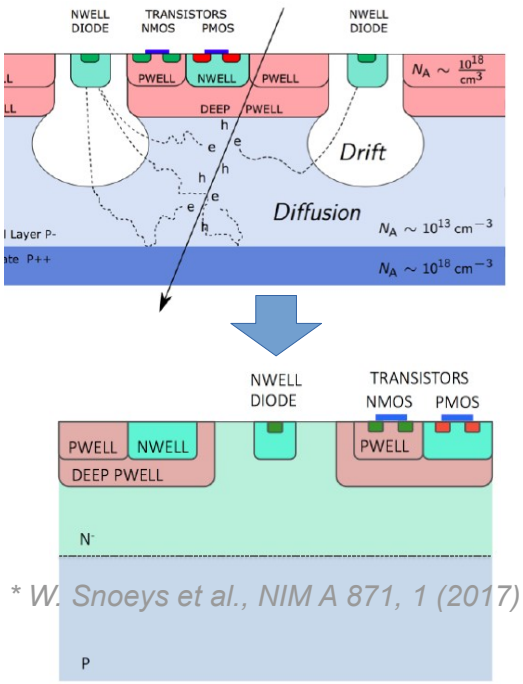



*H. Pernegger et al 2017 JINST **12** P06008*

16 mm x 18 mm




98.5% efficiency after 1E15 neq/cm2 & Fast charge collection



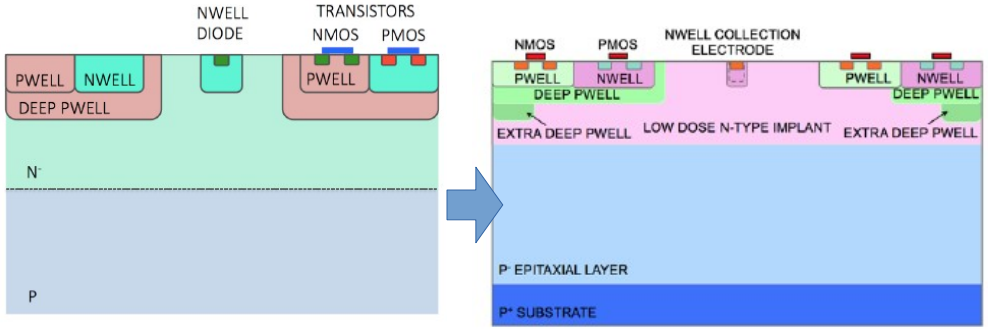

- Very good results after irradiation with modified process
  - *Applies also to TJ-Monopix, devices on same wafer and same sensor design!*
- Further optimization being investigated (next slide)

** W. Snoeys et al., NIM A 871, 1 (2017) 90*

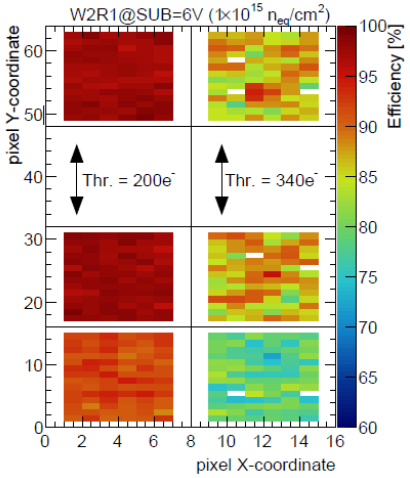
# Depleted CMOS: Small Electrodes

## Mini-MALTA

- TowerJazz 180 nm CMOS CIS
- Full CMOS in pixel
- 36.4 x 36.4 μm² pixels
- Epi thickness: 20 – 30 μm
- High resistivity: 1 kΩ cm
- **Modified process*** to improve lateral depletion
- TCAD simulations used to optimize sensor design
  - *Simulations used in general as a*
  - *tool to aid design (AIDA-2020-D6.1)*




*Improve E field in corners*




- Many options tested
- Very good results up to 1E15neq/cm2

*M. Dyndal et al., 2020 JINST 15 P02005*

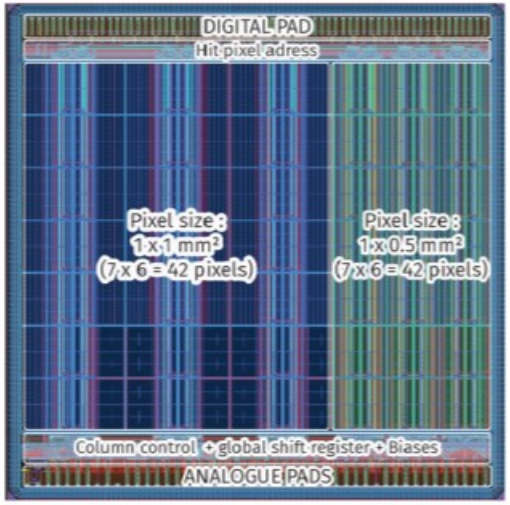
**Table 2**. Summary of the efficiency measurements for various Mini-MALTA chips. The values are shown separately for different sensor regions. All chips were operated at low threshold settings. The uncertainties listed are statistical.

| Chip ID | EPI [μm] | Fluence [1 MeV $n_{eq}/cm^2$] | SUB [V] | Process modification | Efficiency (enlarged trans. region) [%] / threshold [e⁻] | Efficiency (standard trans. region) [%] / threshold [e⁻] |
|---|---|---|---|---|---|---|
| W2R11 | 30 | unirrad. | −6 | n⁻ gap | 99.6±0.1 / 200e⁻ | 99.1±0.1 / 380e⁻ |
| | | | | extra deep p-well | 99.6±0.1 / 200e⁻ | 98.9±0.1 / 380e⁻ |
| | | | | continuous n⁻ | 99.6±0.1 / 200e⁻ | 97.9±0.1 / 380e⁻ |
| W2R1 | 30 | $1\times10^{15}$ | −6 | n⁻ gap | 97.6±0.1 / 105e⁻ | 86.5±0.1 / 210e⁻ |
| | | | | extra deep p-well | 97.9±0.1 / 105e⁻ | 87.0±0.1 / 210e⁻ |
| | | | | continuous n⁻ | 91.9±0.1 / 105e⁻ | 78.8±0.2 / 210e⁻ |
| W4R2 | 25 | $1\times10^{15}$ | −6 | n⁻ gap | 98.8±0.1 / 120e⁻ | 90.7±0.1 / 275e⁻ |
| | | | | extra deep p-well | 99.2±0.1 / 120e⁻ | 92.5±0.1 / 275e⁻ |
| | | | | continuous n⁻ | 95.8±0.1 / 120e⁻ | 79.4±0.2 / 275e⁻ |
| W5R3 | 25 | $2\times10^{15}$ | −10 | n⁻ gap | 92.1±0.2 / 120e⁻ | 73.1±0.3 / 230e⁻ |
| | | | | extra deep p-well | 93.7±0.2 / 120e⁻ | 76.4±0.3 / 230e⁻ |
| | | | | continuous n⁻ | 86.5±0.2 / 120e⁻ | 70.9±0.3 / 230e⁻ |

# Other Applications

**CACTUS** (CMOS Active Timing μ Sensor)

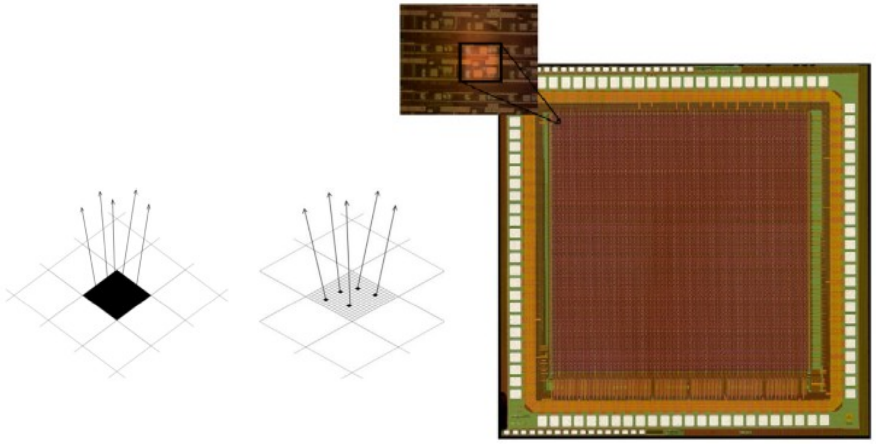
- Timing in a depleted CMOS device for pile-up rejection
- Target 50-80 ps/mip
- First investigator in LF 150 nm technology




*F. Guilloux et al., PoS (TWEPP-17) 024*

**DECAL** (digital electromagnetic calorimeter)

- Reconfigurable depleted MAPS sensor for digital electromagnetic calorimetry
- Improve E resolution by measuring number of particles in calorimeter shower



*P. Allport et al.,*
*NIMA 958 (2020) 162654*

# Conclusions

- WP6 target was to investigate HV/HR CMOS devices for tracking in HEP
- Early on, **depleted monolithic devices** identified as the most promising approach
  - However, big effort on AC coupled devices w/ many lessons learned
- Two approaches pursued on DMAPS: large and small electrodes
  - Both produced very promising results, demonstrating that DMAPS are a leading option for *moderate* radiation hardness requirements
    - Large electrode probably best suited for radiation hardness
    - Small electrode best if low power dissipation critical
- The potential of/interest in the technology reflected in about **30** publications within AIDA2020 (and many more non-AIDA)

**Thanks to all the groups that made such a big progress on DMAPS**

# Outlook – AIDAinnova

- However technology a bit late (system aspects) for LS3 upgrades
  - But huge advancement, can not be ignored, even by the most conservative researchers...
- DMAPS are becoming option/baseline for future experiments
  - CEPC (investigating TJ 180nm), ILC, LS4 upgrades...

- **AIDAinnova** aim to continue playing critical role in pre-TDR projects
- Proposed physics oriented WP structure:
  - High granularity and low mass devices:

    *Higgs factories, ALICE, Belle*
  - Radiation hard and fast devices

    *LS4 upgrades of ATLAS/CMS, LHCb*

**Thanks to all the groups that made such a big progress on DMAPS and looking forward to continue the activities within AIDAinnova**

# Back Up Slides

## Deliverables

| Del. no. | Deliverable name | WP no. | Planned delivery date | Actual delivery date | Status | Comments |
|---|---|---|---|---|---|---|
| D6.5 | Optimised interconnection process | 6 | M42 | 13/05/2019 | Achieved | Report<br>Justification for delay |
| D6.6 | Assemblies delivered | 6 | M40 | 31/08/2018 | Achieved | Report |
| D6.1 | TCAD libraries | 6 | M40 | 30/09/2018 | Achieved | Report |
| D6.2 | Sensor-design guidelines | 6 | M46 | 02/04/2019 | Achieved | Report |
| D6.7 | Recommendation for industrialisation | 6 | M46 | 22/03/2019 | Achieved | Report |
| D6.3 | Performance characterisation results | 6 | M58 | 20/04/2020 | Achieved | Report |
| D6.4 | Radiation tolerance assessment | 6 | M58 | 25/03/2020 | Achieved | Report |
| D6.8 | Final report on HV/ HR CMOS devices | 6 | M58 | 20/04/2020 | Achieved | Report |

## Milestones

| Mil. no. | Milestone name | WP no. | Planned delivery date | Actual delivery date | Status | Comments |
|---|---|---|---|---|---|---|
| MS7 | Simulation workshop on HV/HR-CMOS TCAD and Geant4 simulations | 6 | M6 | 26/05/2016 | Achieved | Justification for delay<br>Report |
| MS11 | MPWR submission | 6 | M12 | 03/06/2016 | Achieved | Report |
| MS26 | First test beam campaign with initial sensor prototype assemblies | 6 | M16 | 21/12/2016 | Achieved | Report |
| MS27 | First irradiation campaign with sensor prototype assemblies | 6 | M16 | 21/12/2016 | Achieved | Report |
| MS28 | First functional HV/HR-CMOS assembly with capacitive interconnection | 6 | M16 | 30/09/2016 | Achieved | Report |
| MS48 | Simulation tutorial on HV/HRCMOS TCAD and Geant4 simulations | 6 | M24 | 28/04/2017 | Achieved | Report |