AIDA 2020

Final Annual Meeting

WP4

Microelectronics and interconnections

Christophe de la Taille (CNRS/IN2P3)
Valerio Re (INFN/Univ. Bergamo)

WP4 network on microelectronic technologies

WP4 had the goal of supporting a network of physicists and engineers working on advanced microelectronic technologies to improve the state of the art of detectors for high energy physics. Readout chips were provided to other WPs for sensor development and testing.

- Qualification of 130 nm and 65 nm CMOS technologies for detector readout (noise, speed, radiation hardness, circuit blocks)

- Design and testing of 65 nm CMOS pixel readout chips, from small prototypes and circuit blocks to the large-scale RD53 integrated circuits for ATLAS and CMS

- Design and testing of 130 nm CMOS chips for the readout of calorimeters and gaseous detectors

- Development of advanced interconnections based on Through-Silicon Vias (TSV) in the substrate of CMOS chips

WP4.2: 65 nm CMOS pixel readout chips

(CERN, IPASCR, CNRS-CPPM, CNRS-OMEGA, INFN-MI, INFN-PV, INFN-TO, UBONN, AGH-UST)

- Main goal of Task 4.2: design and organize an engineering run for the fabrication of 65 nm CMOS chips for the readout of silicon pixel sensors made available by WP7.

- Deliverable: large-scale demonstrator chip RD53A (with a silicon area of about 2.2 cm^2) designed within the CERN-based RD53 collaboration.

- Evaluate the performance that can be attained with a large format integrated circuit in the 65 nm CMOS technology in view of its application to the readout of pixel sensors at the High Luminosity LHC in the next decade.

- This activity went through several stages before the submission of RD53A, including technology qualification (radiation hardness to 1 Grad), design and test of circuit blocks and small-scale prototypes

Small-Scale 65 nm CMOS chips

This activity started with extensive studies for the qualification of the technology, especially of its radiation tolerance at extremely high total ionizing dose (1 Grad), and with the submission of small-scale prototypes of pixel readout chips.

Two different chips were designed with a 64x64 50 μm x 50 μm pixel matrix (about 16 mm^2) with different architectures for the analog front-end and the digital readout, different techniques for digital-to-analog isolation,...

FE65_P2 (Bonn): submitted end of September 2015 (with LBNL)

CHIPIX65 demonstrator (INFN): submitted Q2 2016

These prototypes were also bonded to pixel sensors, allowing other WPs to do preliminary tests with their devices

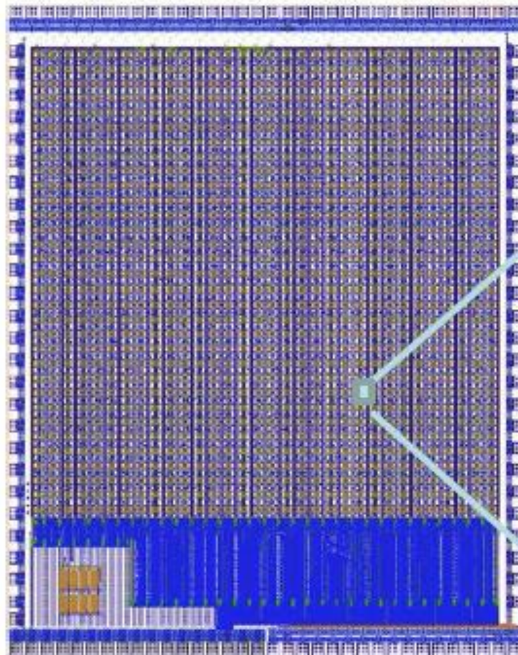
Small-Scale 65 nm CMOS chip: FE65_P2

FE65_P2 prototype chip *(Bonn-LBNL)*

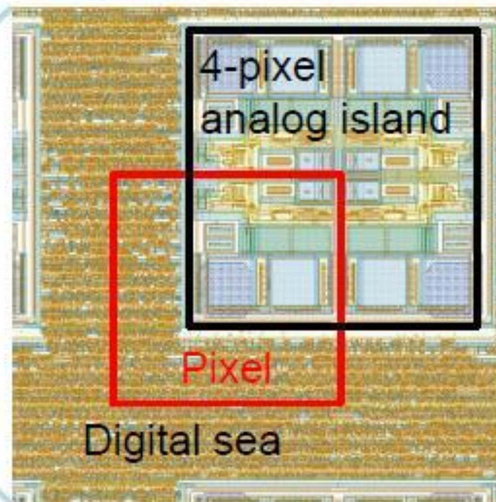
– 64x64 matrix, 50x50 μm^2 pixel

– Put into effect the following RD53 WG proposals:

- *Top level* → digital on top hierarchical flow, modular approach (4x64 pixel cores), analog islands
- *Architecture* → distributed latency buffering architecture (2x2 pixel region optimized for higher hit rates)
- *Analog* → "differential" front end



FE65_P2 prototype chip layout,



Pixel region with digital sea and

submitted end of September 2015, delivered by the foundry in December 2015

Small-Scale 65 nm CMOS chip: CHIPIX65

CHIPIX65 Demonstrator

(CHIPIX65 Italian INFN collaboration)

– 64x64 matrix, 50x50 μm² pixel

Top level → digital on top hierarchical flow, analog islands

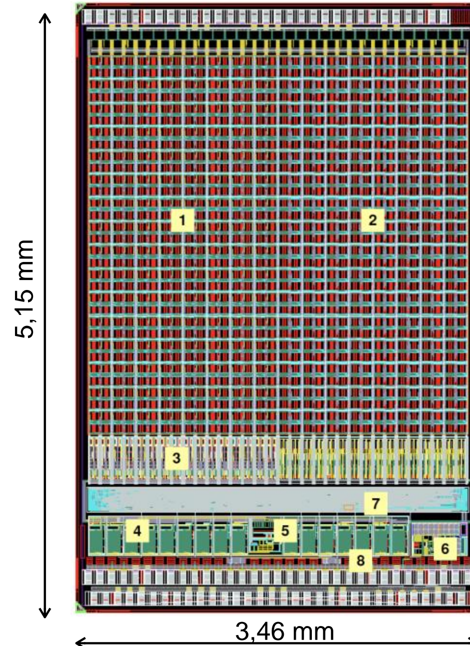
Analog → integration of 2 different flavors (synchronous and linear)

Architecture → centralized latency buffering architecture (4x4 pixel region)

Simulation and verification → VEPIX53 framework

IP → implementation of a set of tested RD53 IP blocks (bandgap, DAC, serializer...)

CHIPIX65 demonstrator

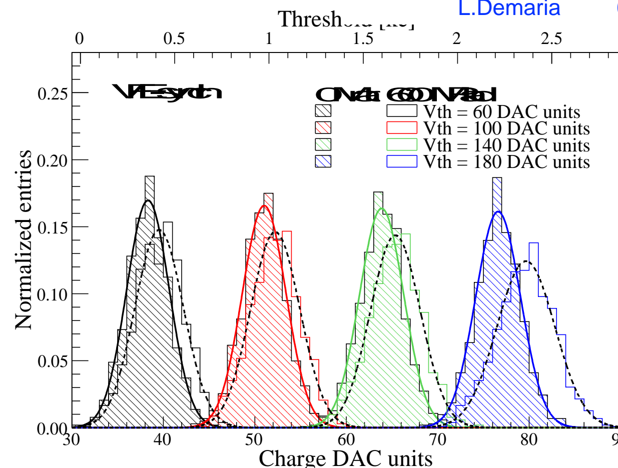


1) (32x64) pixels with Synchronous FE architecture
2) (32x64) pixels with Asynchronous FE architecture
3) replicated Bias Cells with current mirrors
4) 10-bit biasing DACs
5) Bandgap voltage reference
6) 12-bit monitoring ADC
7) readout/configuration digital block and High-speed Serializer at the chip periphery
8) SLVS transmitters/receivers and I/O cells

submitted: 5/7/2016
Arrived: 26/9/2016

L.Demaria 65nm development in CHIPIX65/INFN AIDA-2020 - Desy 15/06/2016 2

submitted July 2016, delivered at the end of September 2016.



- Low threshold possible, **250-300e-** for bare chip
- The **auto-zeroing** is working well
- The measurements have been repeated after a TID = 600 Mrad has been reached with X-ray irradiation at -20°C with the chip in working conditions. **The irradiated chip is still fully operational**
- For thresholds below 1 ke-, which is the region of interest, the increase of the dispersion with radiation is below 10%

65 nm CMOS radiation hardness studies

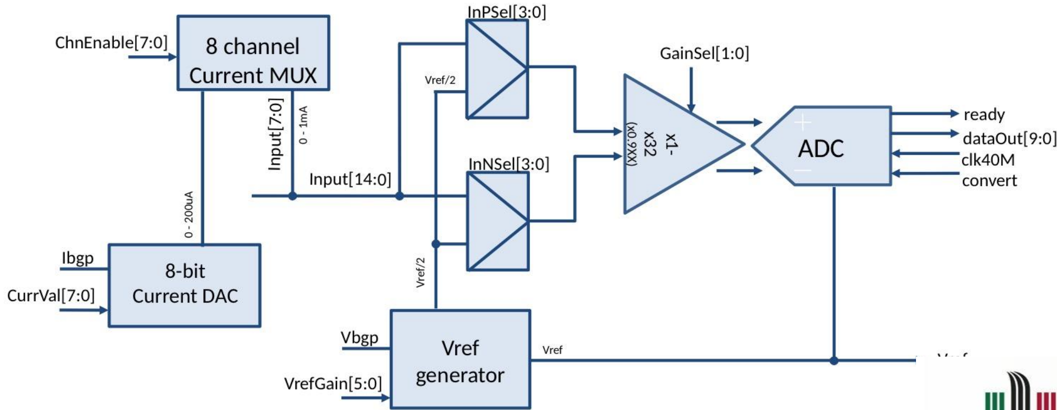
CPPM

- 65 nm process qualified for 500 Mrad TID
  - Limited leakage current
  - A strong drive loss for small size PMOS devices and damage increases with temperature
  - RD53 Front end chip (pixel environment)
    - Avoid the use of narrow or short transistors for analog design
    - Corner Models developed for 200 Mrad and 500 Mrad and used to characterize digital cells
    - DRAD chip designed by CERN group indicates which digital libraries can be used
    - The temperature effect can be avoided and delayed by keeping cold: -20°C for 5 years and keeping unbiased at room temp for few months
- SEU tolerant latches for pixel and global configurations were designed and tested
- Operating conditions (bias, temperature) must be kept under accurate control to ensure that the chip remains functional at extremely high TID
- Using large transistors in analog circuits, analog parameters (noise, threshold dispersion, transfer characteristics,..) are moderately affected (10 – 20%)

65 nm CMOS blocks

Developments in TSMC 65 nm
lpGBT – analog signals monitor

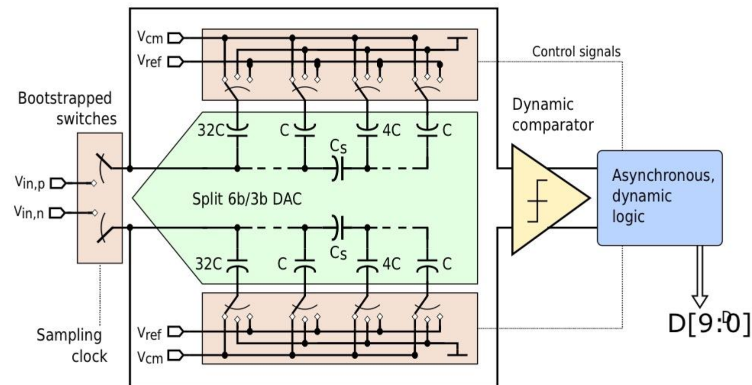
All important blocks designed: 10-bit ADC, variable gain (x1,x8,x16,x32) instrumentation amplifier, 1V Vref generator, 8-bit current DAC, etc...



LpGBT was completed and fabricated in 2018.

In the WP4 network, a lot of design effort was focused on the development of 65 nm IP blocks for RD53 A and for other chips for HL-LHC, ILC,...

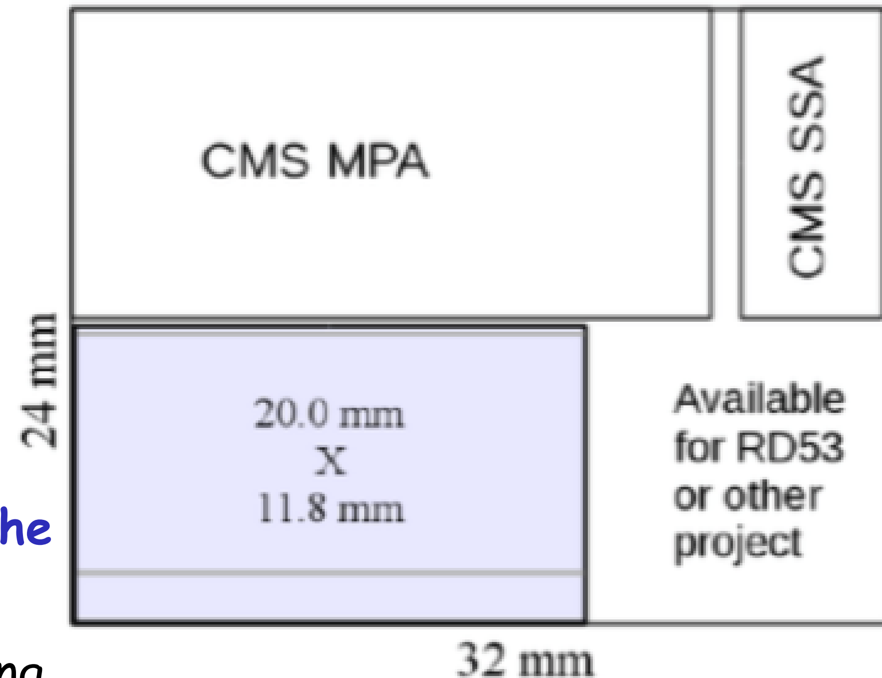
Developments in TSMC 65 nm
Fast ultra-low power 10-bit SAR ADC



Few different flavours (MIMcap, MOMcap, switching shemes) of 8-channel ASICs with fast (50-100MSps), ultra-low power 10-bit and 12-bit SAR ADCs were designed and fabricated in 2018 and tested

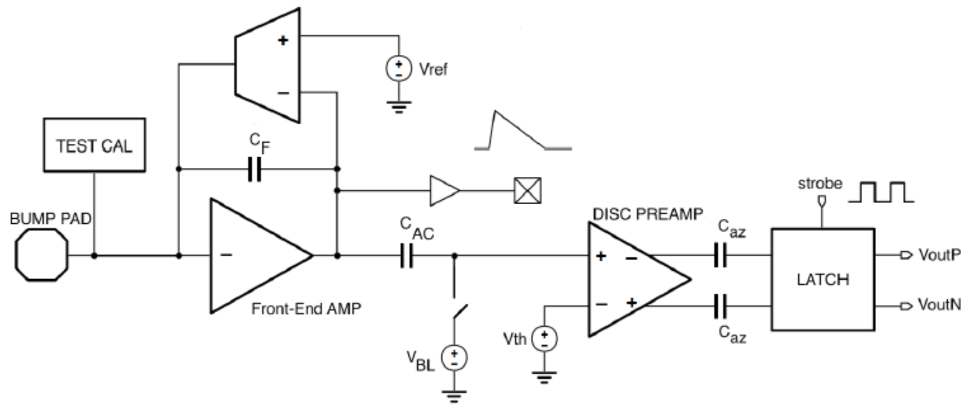
RD53A - Large Scale prototype

- WP4 supported the efforts of the RD53 collaboration leading to the submission of the RD53A chip in an engineering run
- 400 x 192 pixel, 50 μm x 50 μm pixel, 20 mm x 11.8 mm chip
- Goal: demonstrate in a large format IC
  - suitability of 65nm technology (integration of mixed-signal circuits in small pixel cells inside a large-scale chip)
  - high hit rate: 3 GHz/cm^2
  - trigger rate: 1 MHz
  - Low threshold operation with chosen isolation strategy and power distribution
  - Tolerance to 500 Mrad TID
- Not intended to be a production chip
  - contains design variations for testing purposes (with 3 different versions of the analog front-end)
  - wafer scale production enabled prototyping of bump bonding assemblies with realistic sensors in new technology

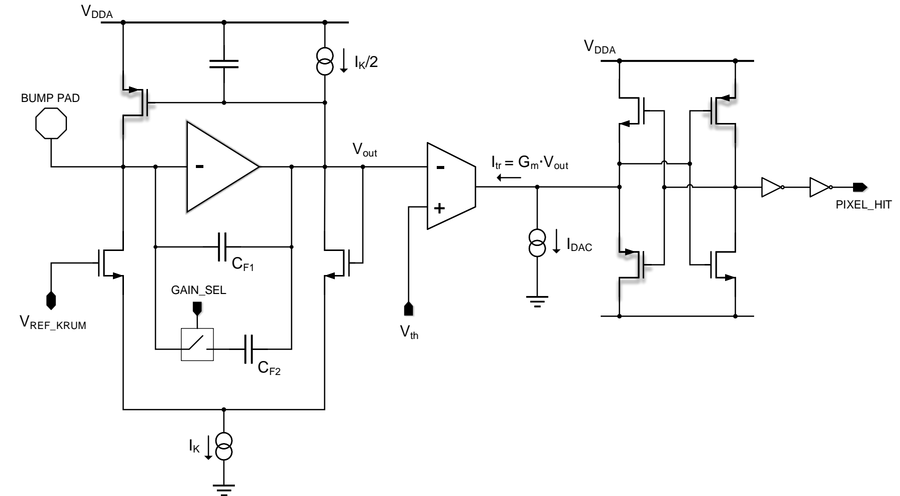


The 3 analog front-ends in RD53A

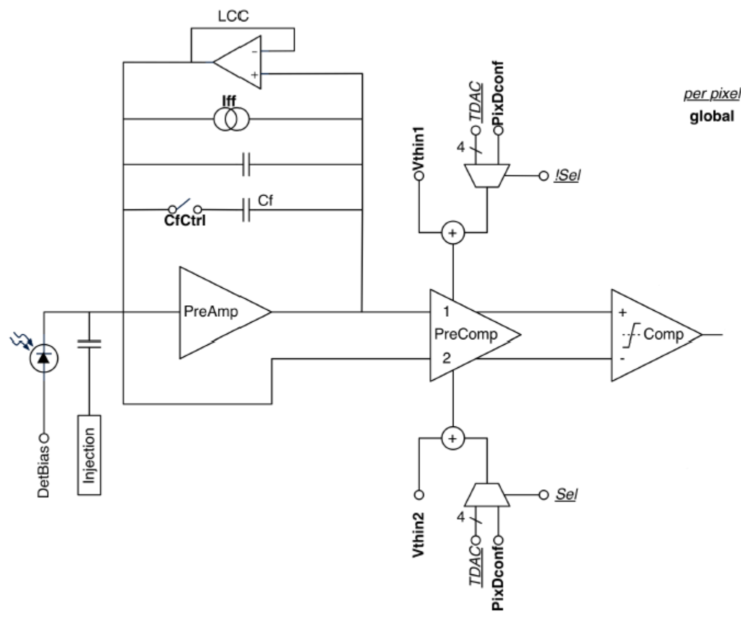
Synchronous AFE



Linear AFE



Differential AFE

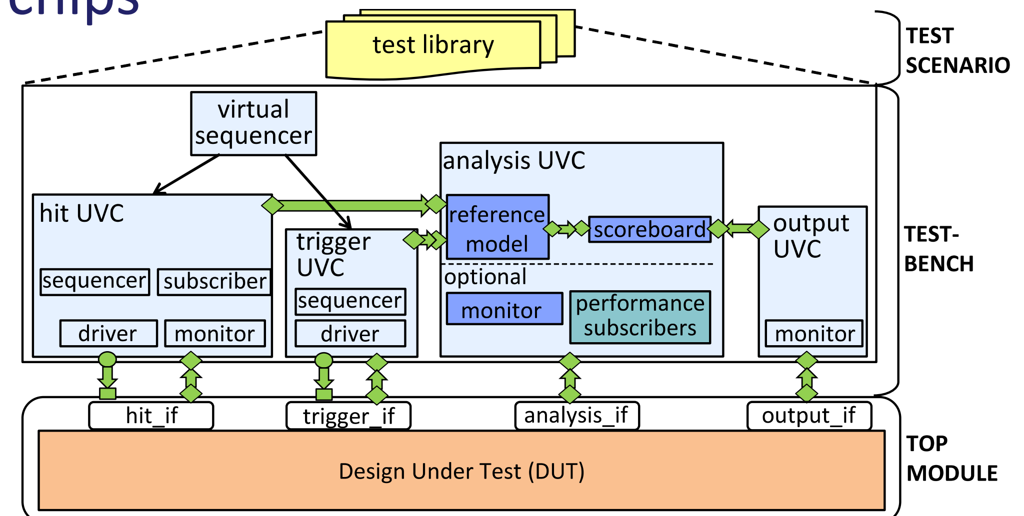


- Evaluation of various design choices for the front-end stages
- Constraints for noise, power, speed, silicon area, immunity to digital interferences had to be taken into account in the analog blocks (preamplifier, discriminator,…)

Simulation and verification of the digital architecture

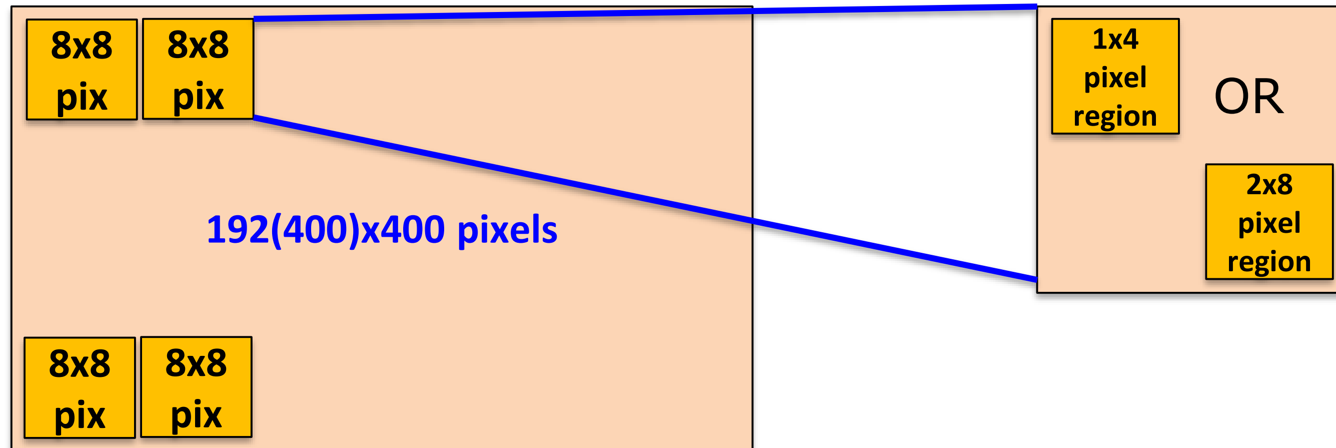
For the most complex chip developed by our community, a huge work was carried out for the simulation and verification of digital readout architecture

- **Verification Environment** for **PIXel** chips (*VEPIX53*) for:
  - **Modularity**, **reusability** of same testbench:
    - different tests
    - multiple design stages
    - different designs/design blocks



Simulation and verification of the digital architecture

- **Basic layout unit**: 8x8 digital Pixel Core → synthesized as one digital circuit

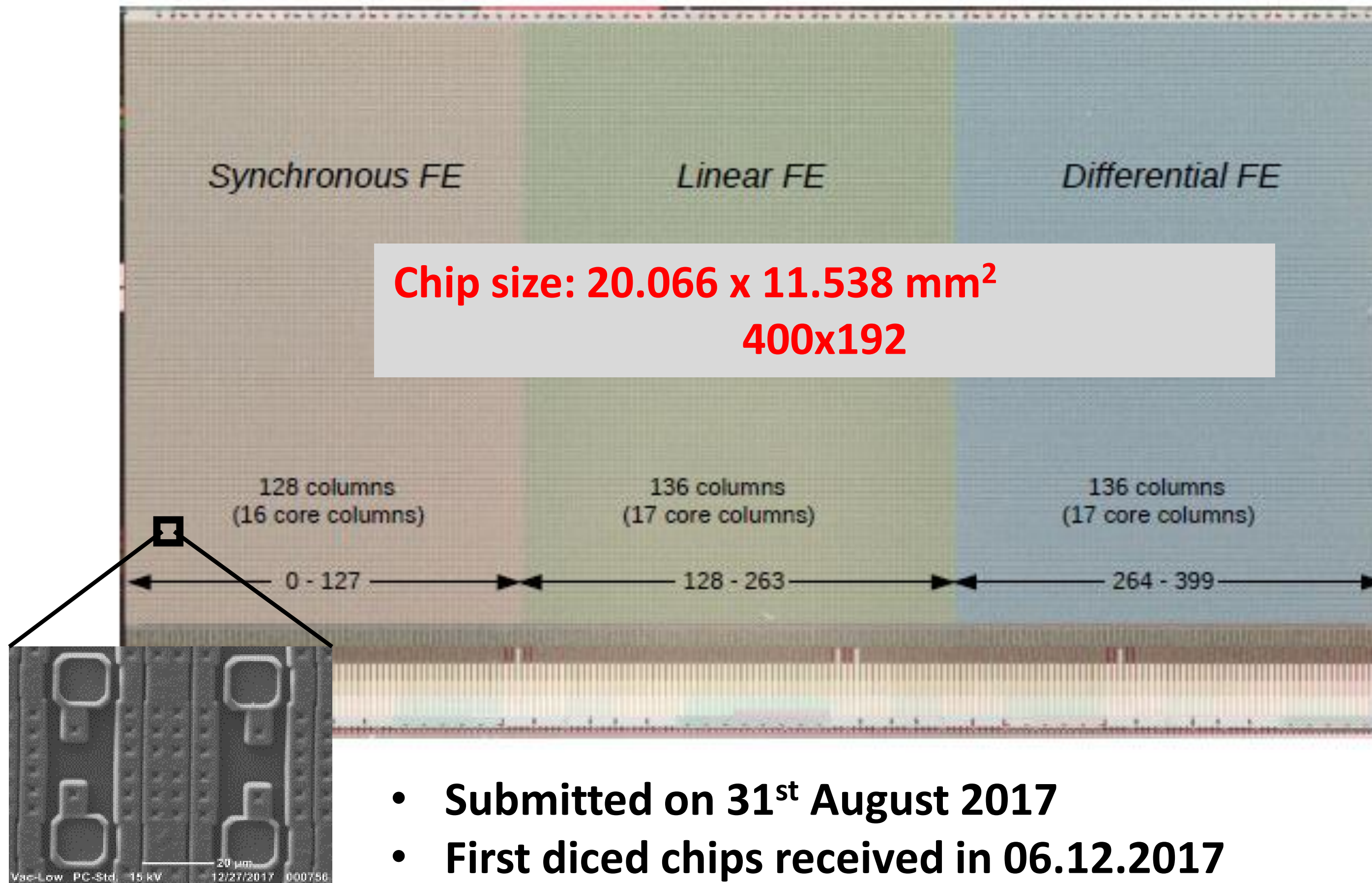


- One Pixel Core contains multiple Pixel Regions and some additional arbitration and clock logic
- Pixel Regions share most of logic and trigger latency buffering

Distributed Buffering Architecture (FE65_P2 based):
- distributed TOT storage

Centralized Buffering Architecture (CHIPIX65 based (4x4)):
- centralized TOT storage
- Integrated with Synch FE

RD53A



RD53A core design team

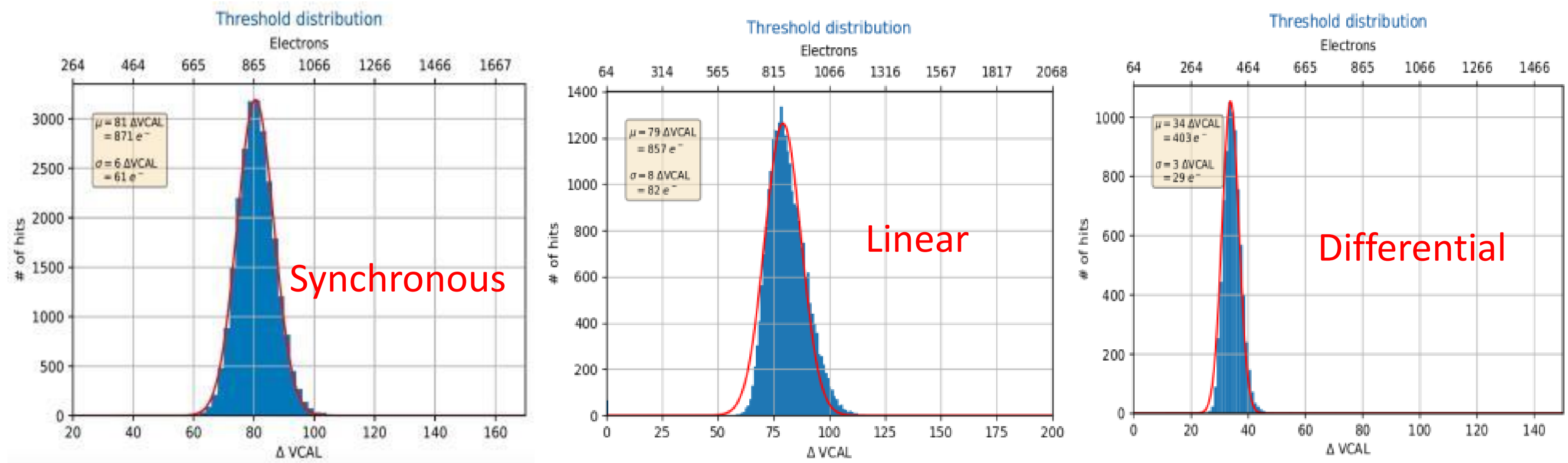
- Flavio Loddo (Bari)
- Tomasz Hemperek (Bonn)
- Roberto Beccherle (INFN PI)
- Elia Conti (CERN)
- Francesco Crescioli (Paris)
- Francesco De Canio (INFN BG-PV)
- Leyre Flores (Glasgow)
- Luigi Gaioni (INFN BG-PV)
- Dario Gnani (LBNL)
- Hans Krueger (Bonn)
- Sara Marconi (CERN / INFN PG)
- Mohsine Menouni (CPPM)
- Sandeep Miryala (FNAL)
- Ennio Monteil (INFN TO)
- Luca Pacher (INFN TO)
- Andrea Paternò (INFN TO)

- **Submitted on 31st August 2017**
- **First diced chips received in 06.12.2017**
- **Total transistor count: 310M (x2 for final)**
- **First bump-bonded chip test: April 2018**

Chips have been made available to users (beam tests by the AIDA2020 sensor workpackage)

Characterization of analog front-ends

All Front-Ends are **operational and can be operated at low threshold**



These results provide a nice demonstration of the possibility of designing high performance analog front-end circuits in sub-100 nm CMOS technologies

Noise and threshold

RD 53A

Each FE design has following characteristics:

- Noise – affects minimum achievable threshold
- Threshold dispersion – affects energy resolution

We measure mean and threshold dispersion after tuning

- Bare chip – no sensor
- Cold (-20C and -8.6C)
- Measured at four current consumptions per pixel: 3μA, 3.5μA, 4μA, 5μA

ENC [e]

Front-end	3μA	3.5μA	4μA	5μA		Average
Differential	39	38	45	46	→	**42**
Linear	70	65	70	65	→	**68**
Synchronous	81	77	79	75	→	**78**

Tuned threshold dispersion [e]

Front-end	3μA	3.5μA	4μA	5μA		Average
Differential	27	31	35	38	→	**33**
Linear	77	78	78	80	→	**78**
Synchronous	84	82	74	75	→	**79**

There is little variation in threshold dispersion and noise with current consumption.

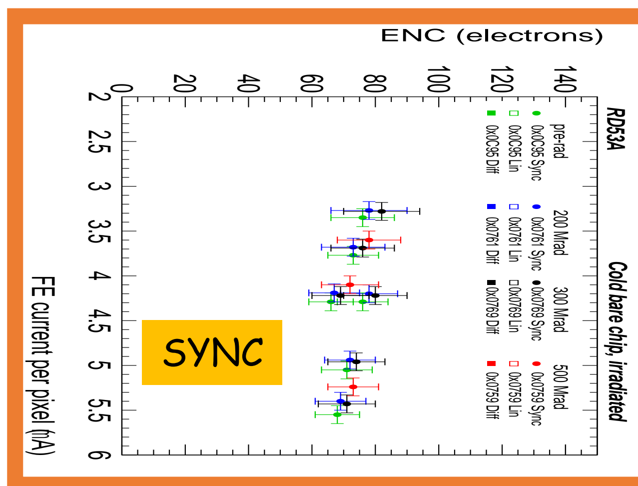
There are no strict requirements on these characteristics, and the results are deemed acceptable.

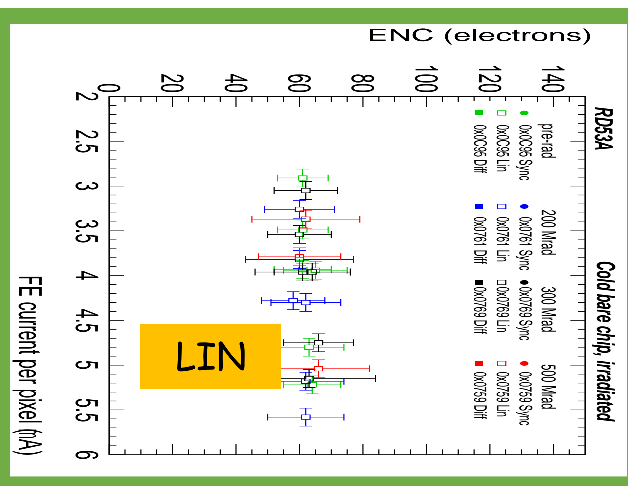
UNIVERSITAS BERGENSIS

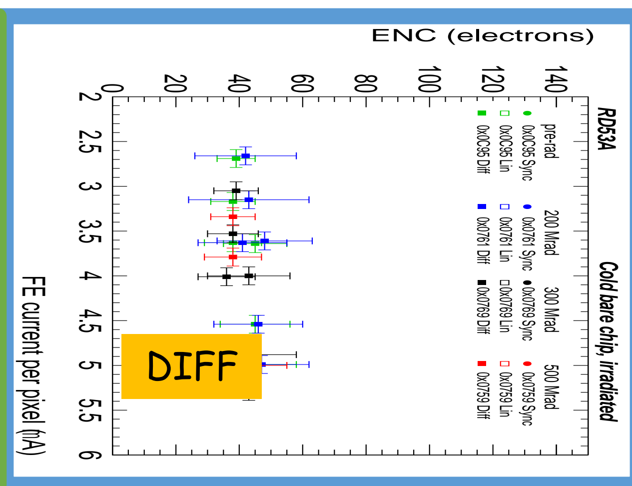
Analog FE characterization after irradiation

- Irradiation with X-rays @c old, RD53A powered and tested/readout continuously
- Very good results - chip works, all three AFEs operated with **low thresholds**
- **Noise** for different current settings (for 0, 200, 300, 500 Mrad)

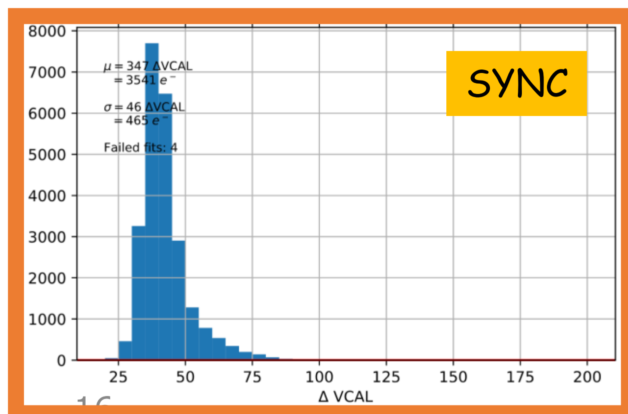
A. Dimitrievska, RD53A talk, VCI 2019

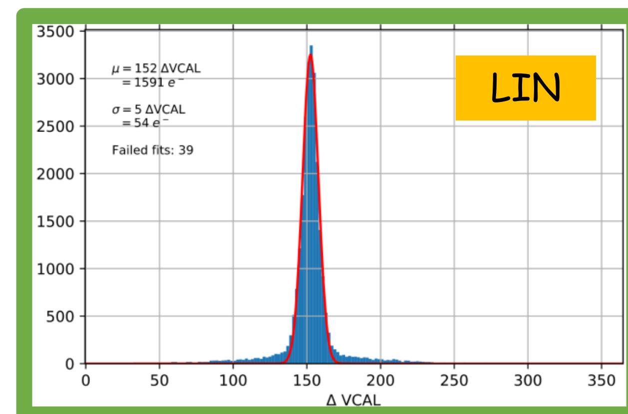


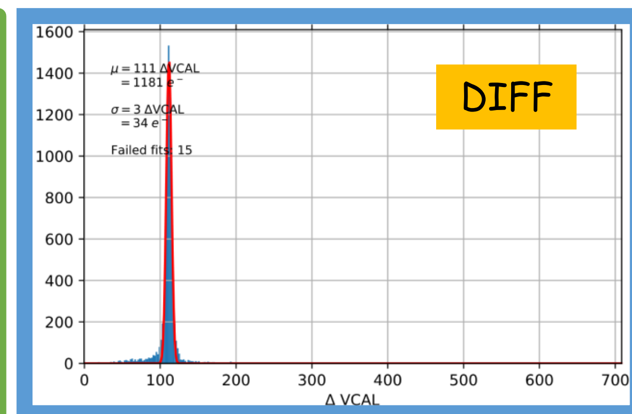




- **Threshold** distribution after 1 Grad irradiation of a bare chip







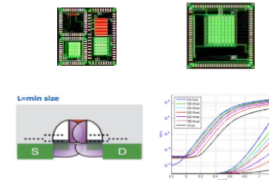
NOTE: sigma from Gaussian fit, not RMS from data

From RD53A to RD53B: development of the next generation readout chips for the ATLAS and CMS experiments at the HL-LHC

RD53 timeline

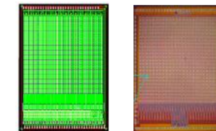
2013

Building blocks: Analog FEs, IPs
Digital Architecture
Verification environment
Complex Chip Integration
Radiation characterization of the CMOS 65 nm



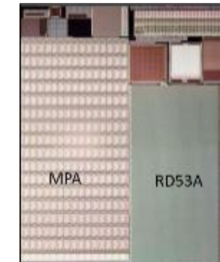
2015

Small demonstrators (64x64 pixel matrix)
FE65P2
CHIPIX65-FE0

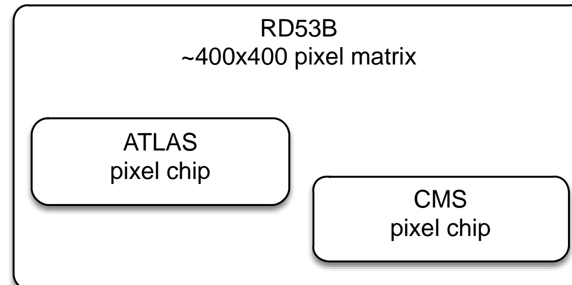


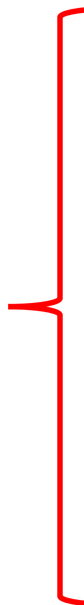
2017

RD53A large scale prototype
400x192 pixel matrix



2020





supported by AIDA2020

From RD53A to RD53B

- The **success of RD53A** is the baseline for the design of the pixel readout chips of CMS and ATLAS at the HL-LHC
- **RD53B** is the common design framework for the design of the final production pixel chips for ATLAS and CMS
- **One common design team**
- Two submissions of the RD53B design with different **matrix sizes** and **analog front-ends**
- **After a very detailed review process, a choice was made for the analog FE by ATLAS (Differential) and CMS (Linear)**
- **The pixel array size is a parameter** in the design, controlling how many identical **8x8 Pixel Cores** are arrayed in x and y → **same netlist**
- All the common and specific requirements implemented in a unique architecture → **no difference in the chip bottom or in the core design**
- The specific requirements will be enabled/disabled by chip configuration and/or hard-wired setting
- Use the same IP blocks implemented in RD53A demonstrator, with improvements where needed

From RD53A to RD53B

- **Additional features** implemented in RD53B (list not exhaustive)
  - Bias of edge and top "long" pixels
  - 6-to-4 bit dual slope ToT mapping
  - 80 MHz ToT counting
  - ATLAS 2-level trigger support
  - Power saving ~20%
  - Improved design for testability
  - TMR for pixel configuration
  - Optimal data formatting and compression

ATLAS/CMS main differences in requirements

	RD53B-ATLAS (ITkPix v1)	RD53B-CMS (CROC v1)
Pixel array size	**20x19.2 mm^2 (400 x 384)**	**21.6x16.8 mm^2 (432 x 336)**
Trigger	1 level: 1MHz, 10us 2 level: L0: 4MHz, 10us, L1: 600KHz, 25us	1 level: 750 kHz, 12 us
Distance to the beam → Hit rate	r = 4 cm	r =3 cm

The ATLAS version of the chip was submitted on March 18, 2020 (the CMS chip is scheduled in summer 2020).
This is a major milestone for an activity that was very effectively supported by AIDA2020.

WP4.3: Deliverable chip in 130 nm

CNRS-IPNL, CNRS-OMEGA, DESY, AGH-UST

- Development of high speed, low noise, large dynamic range ASICs for calorimeter readout and high speed timing measurements (detectors of WP13 and WP14)
- Initial goal was to evaluate and select a 130 nm SiGe process
- However, the TSMC 130 nm CMOS process proved to be able to achieve the performance required by the new LHC fields of application (ATLAS HGTD and CMS HGCAL) and was chosen to realize WP4.3 designs.
- This technology has been qualified by CERN for adequate radiation hardness and simulation results showed good performance
- Better synergies with Task 4.2 (65 nm CMOS) and encompasses a broader community.

Process evaluation

- Two SiGe 130 nm BiCMOS processes were targeted (STMicroelectronics and Tower Jazz) and the design kit was obtained from STM.

- Extensive simulations have been carried out in STM, studying two main designs, one for ATLAS LAr calorimeter upgrade (requiring very low noise) and the other for high speed RPCs of WP13 (requiring GHz bandwidth for picosecond measurements).

- In both cases, the performance was not significantly better compared to regular CMOS, despite the the excellent transconductance, because of a worse parallel noise or of the base spreading resistor.

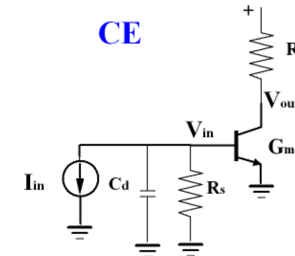
- 4 chips submitted in MPW 130nm CMOS (May&Dec 2016)
  - LAUROC : Liquid Argon Upgrade Read Out Chip (ATLAS)
  - HGCAL TV1 : Test Vehicle 1 for CMS HGCAL
  - ALTIROC : Atlas LGAD Timing ROC for ATLAS HGTD
  - HGCAL TV2 : test vehicle 2 for CMS HGCAL

Choice of 130 nm CMOS

CE in SiGe 130nm and in TSMC 130 nm

Ωmega

- Broad Band amplifier CE configuration
- Same current (Ic=700 µA), same Rf=4K, vdd=1.2V
- Higher gain with SiGe but larger noise due to rbb'



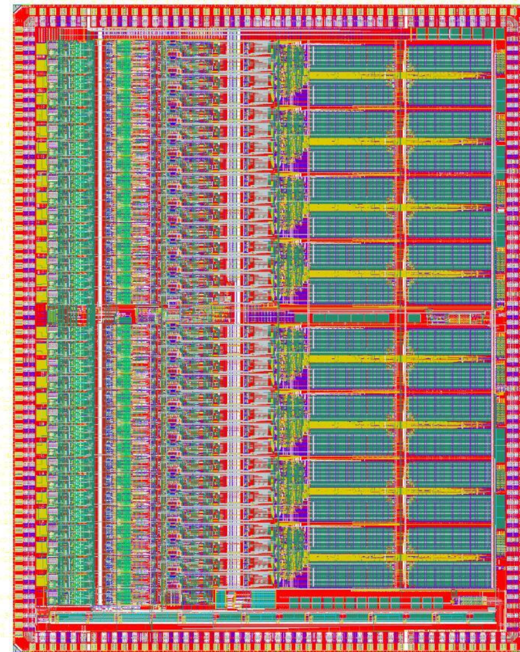
	CE 10pF TSMC 130 nm	**CE 10pF SiGe 130nm Trans size= 20**
td=10ps Qin=Iin.td= 100µA.10ps=**1fC** $V_{in} = \frac{Q_{IN}}{C_d} = \frac{I_{IN} t_d}{C_d}$ Iin Cd width=td	out=3.7mV tr=220ps BWa=1.6 GHz rms=1.3 mV S/N=2.8 σj=220ps/2.8=78 ps	out=8.95 mV tr=176 ps BWa= 2GHz rms=3.14mV S/N=2.85 σj=176ps/2.85=60 ps
td=1ns and tr_ampli=td CL=100fF Qin= 1µA.1ns=**1fC**	out=3.52mV(CL=100fF) tr=1.1ns BWa=440MHz rms=0.66mV S/N=5.3 σj=1100ps/5.3=206 ps	out=7.5mV (CL=110fF) tr=1.1 ns BWa=440MHz rms=1.4 mV S/N=5.4 σj=1.1ns/5.4=204 ps

The main deliverable for WP4.3: HGROC

HGCROCV1

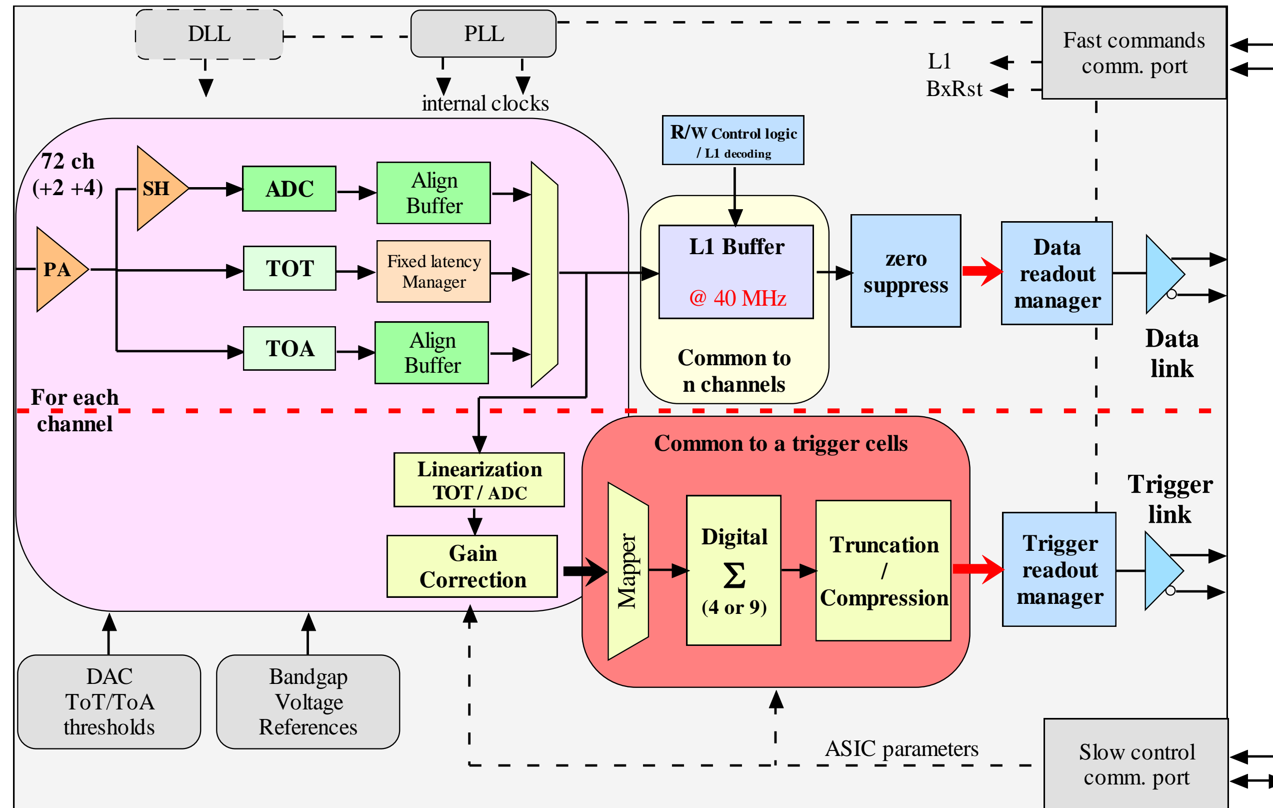
- Large dynamic range chip for calorimeter/sipm/rpc measurement

- 32 ch
- 7x5 mm² 224 pads
- 8 blocs of 4 ch + digital
- Analog on top
- Bias, DLLs, CKs in the middle
- DACs, REFs at the bottom
- Analog and digital probes
- Bias accessible on pads
- All stages switchable ON/OFF
- Slow control separated
- 1.28 Gb High speed e-links
- Submitted 26 July 2017
- Arrived end October and now under test



MPW submission end of July 2017, received October 2017

HGROCv1: Large dynamic range chip for calorimeter/SiPM/RPC measurement



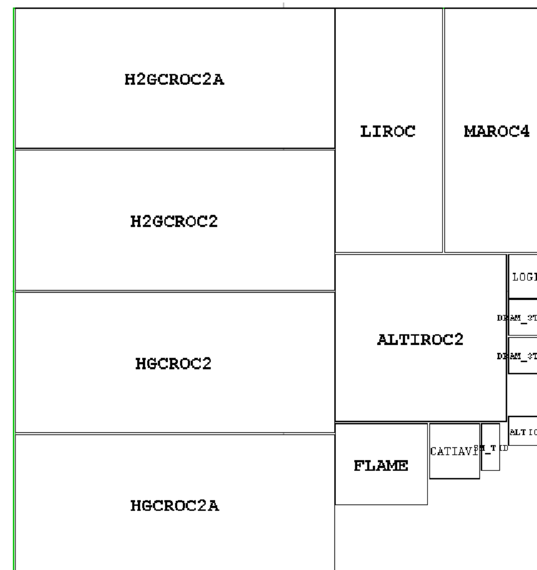
Major milestone and deliverable of WP4: HGCROC1 chip working well

- Excellent analog performance : low noise, low jitter
- But ADC dominated by digital noise
- Power too large in SRAM => new DRAM

TSMC 130 nm CMOS engineering run

- Fabrication engineering run TSMC 130 nm in Feb 2019
  - 14 wafers, 20 000 chips, Cost ~300 k€
  - sharing ATLAS/CMS/AIDA/
  - Chips for « imaging »calorimetry : HGCROC (OMEGA+AGH+CEA+CERN) , FLAME (AGH) and CATIA (CEA)
  - Chips for picosecond timing : ALTIROC (OMEGA+IFAE+SLAC+SMU)

chip	resp	exp
HGCROC2	OMEGA	CMS
HGCROC2A	OMEGA	CMS
H2GCROC2	OMEGA	CMS
H2GCROC2A	OMEGA	CMS
LIROC0	OMEGA	R&D
MAROC4	OMEGA	VALO
ALTIROC1_V2	OMEGA	ATLAS
FLAME_V1	AGH	ILC
DRAM_V2	CERN	CMS
DRAM_V3	CERN	CMS
CATIA_V1	IRFU	CMS
ALTIC	LPCF	ATLAS
LOGIC130	LPCF	ATLAS
SM_TID	CERN	IRRAD



HGCROCv2 overview

Overall chip divided in two symmetrical parts

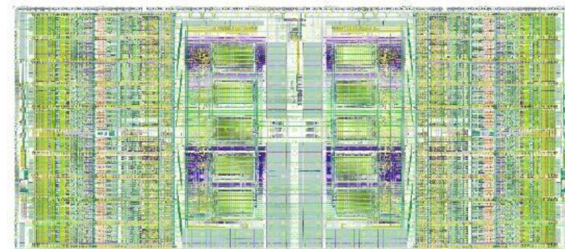
- 1 half is made of:
  - 39 channels: 18 ch, CM0, Calib, CM1, 18 ch (78 channels in total)
  - Bandgap, voltage reference close to the edge
  - Bias, ADC reference, Master TDC in the middle
  - Main digital block and 3 differential outputs (2x Trigger, 1x Data)

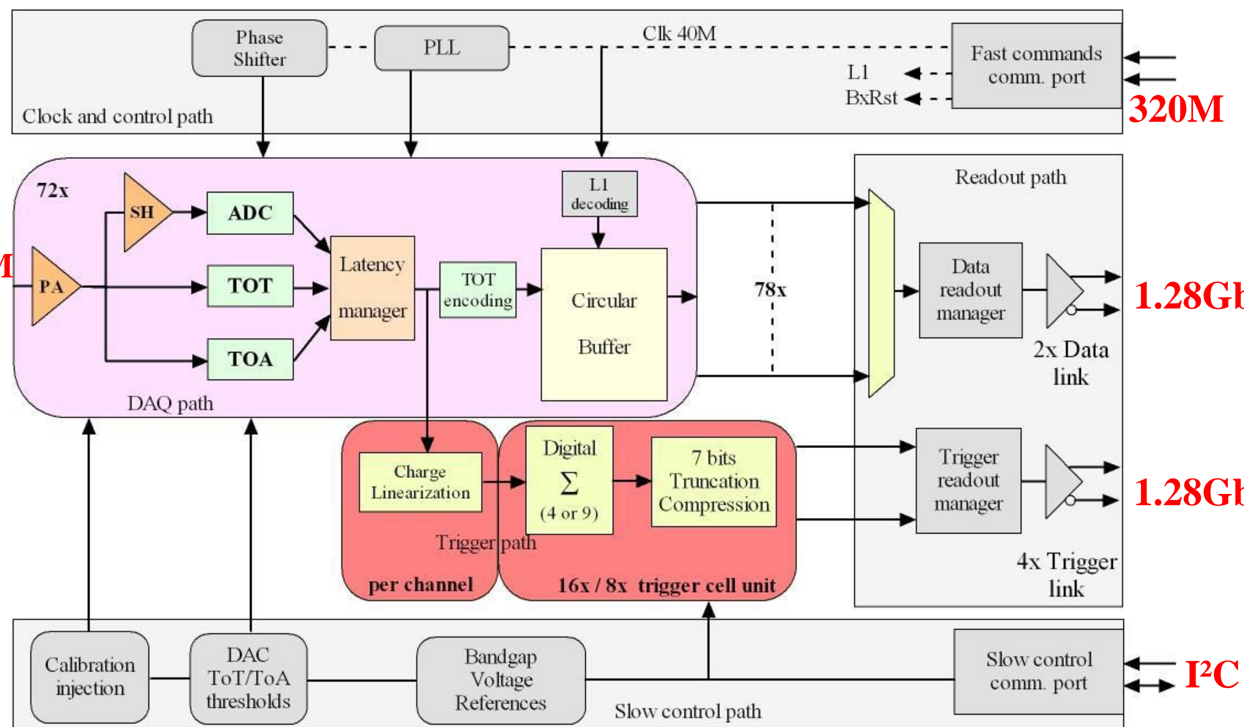
Measurements

- Charge
  - ADC (AGH): peak measurement, 10 bits @ 40 MHz, dynamic range defined by preamplifier gain
  - TDC (IRFU): TOT (Time over Threshold), 12 bits (LSB = 50ps)
  - ADC: 0.2 fC resolution. TOT: 2.5 fC resolution
- Time
  - TDC (IRFU): TOA (Time of Arrival), 10 bits (LSB = 25ps)

Two data flows

- DAQ path
  - 512 depth DRAM (CERN), circular buffer
  - Store the ADC, TOT and TOA data
  - 2 DAQ 1.28 Gbps links
- Trigger path
  - Sum of 4 (9) channels, linearization, compression over 7 bits
  - 4 Trigger 1.28 Gbps links





Control

Fast commands

320 MHz clock and 320 MHz commands

A 40 MHz extracted, 5 implemented fast commands

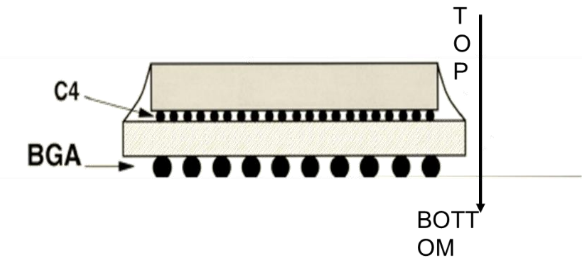
I2C protocol for slow control

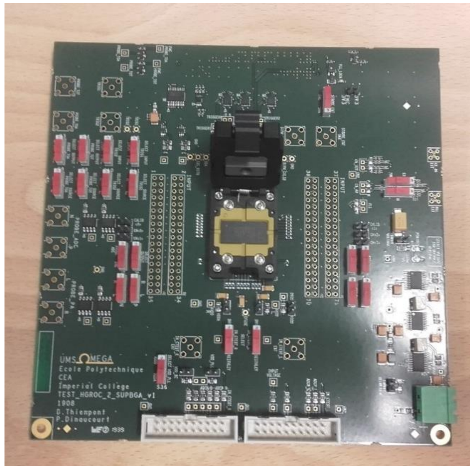
Ancillary blocks

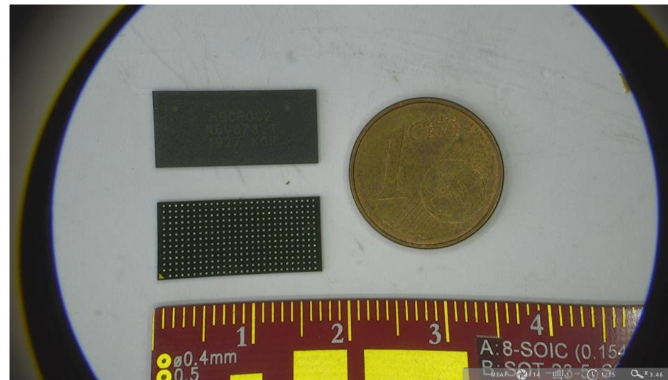
Bandgap (CERN)

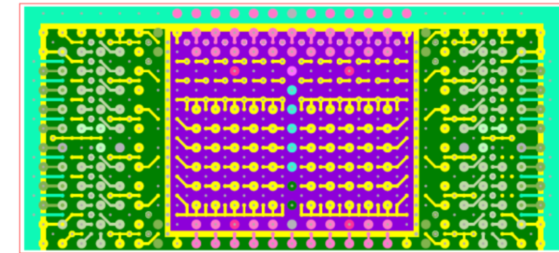
Packaging and testing

- Custom BGA package fabricated by JCET in Taïwan/South Korea
  - Substrate designed at OMEGA
  - Flip chip assembly : much better powering/grounding solved digital noise of V1
  - Full wafers processed by JCET
  - Excellent quality record and professional handling
  - Custom socket developed by NESTEK (Korea)
  - Larger pitch BGA under study for SiPM



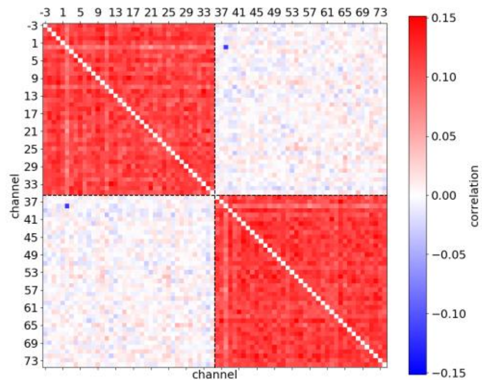




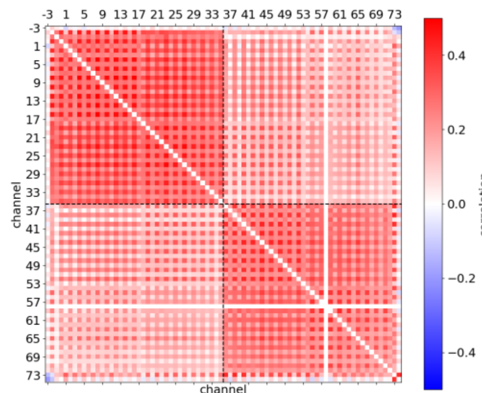


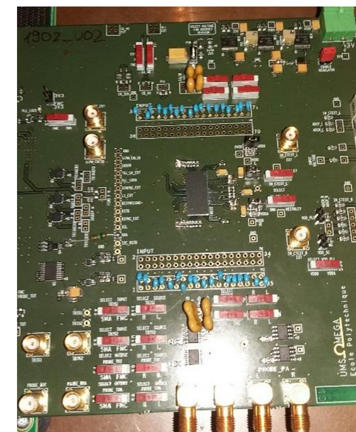
Pulse shapes

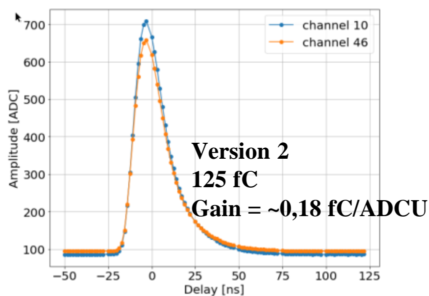
Flip-Chip board

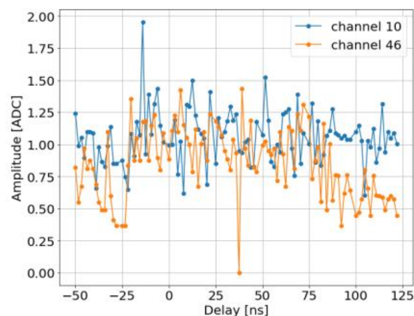


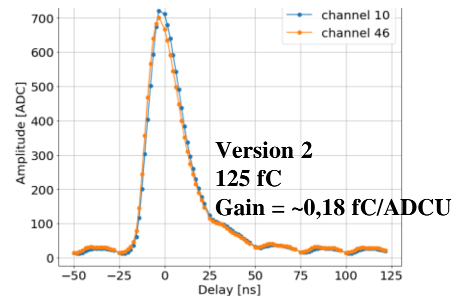
BGA board

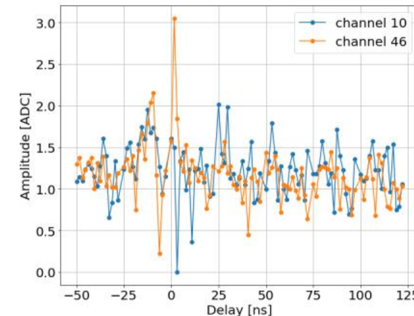










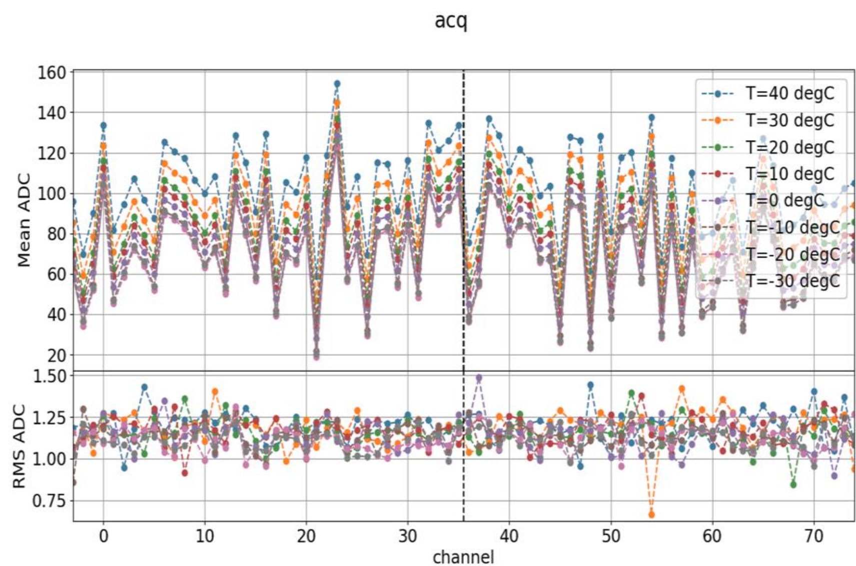


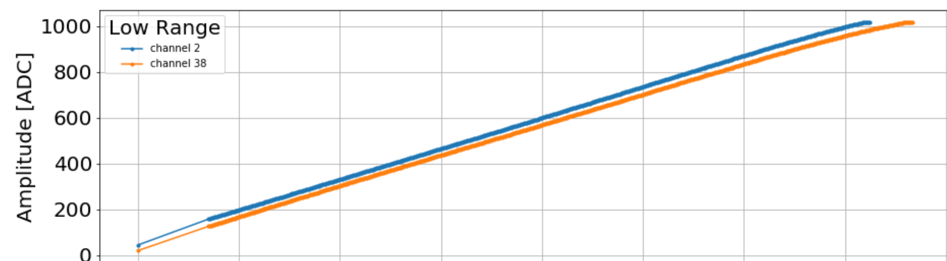
FlipChip
- No digital coupling on preamp inputs
- w/o sensor capacitance, noise = ~1 ADC (0,22 fC)
- Power : 10 mW/ch

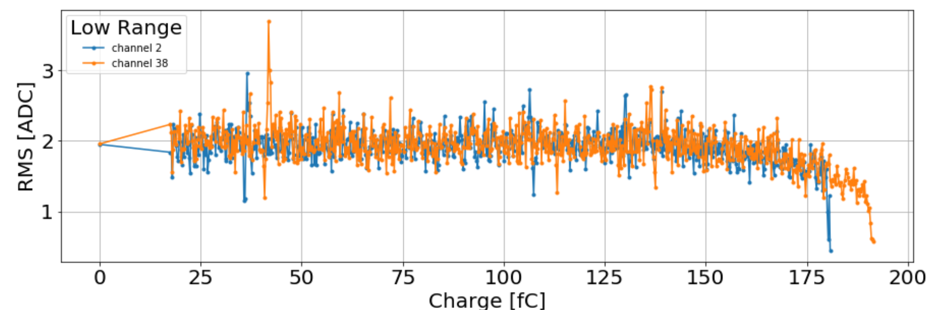
BGA
- Digital coupling on preamp inputs (20 ADC; 3,6 fC)
- w/o sensor capacitance, noise = ~1,25 ADC (0,27 fC)
- Yield > 80% (preliminary)

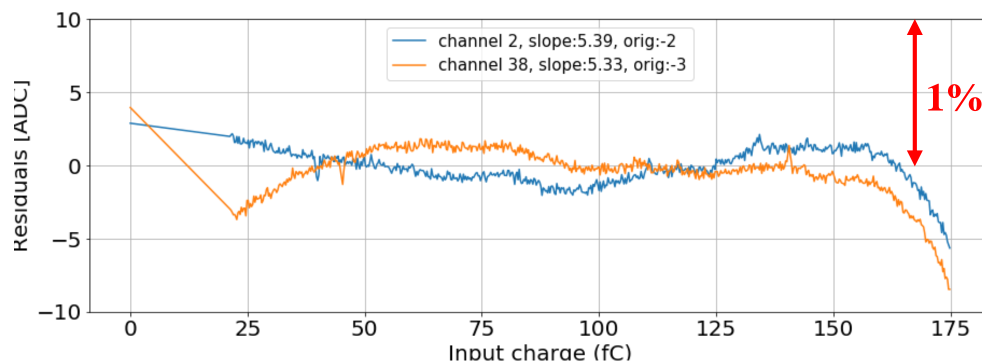
Charge ADC : linearity

- 10b/40 MHz/1 mW SAR ADC Krakow design
- Two 10b-DAC to globally set the pedestal to the desired level
- 5b-DAC to reduce dispersion per channel
- Good linearity in-between +/- 1%
- Noise 1-2 ADC counts depending on Cd



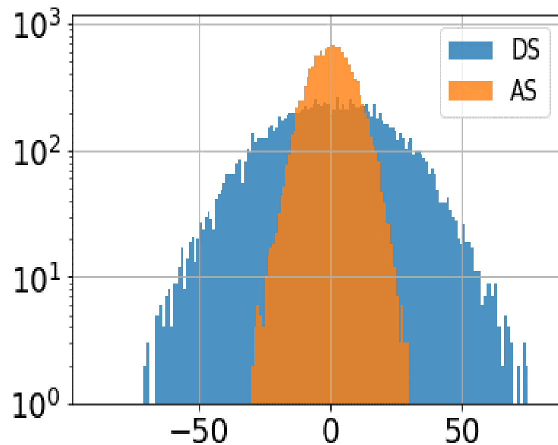


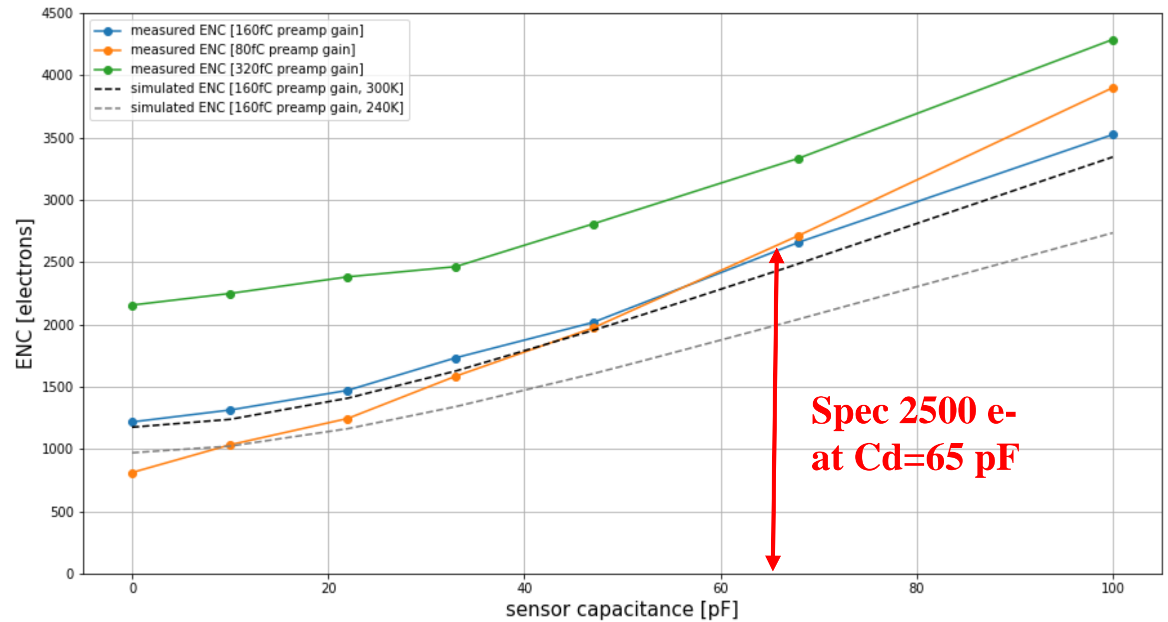




Noise

- Flip chip configuration has allowed to remove dominant digital noise of V1
- Series noise extracted as e_n = 0.7 nV/√Hz and C_{PA} = 12.6 pF
- Coherent noise extracted by comparing direct and alternate sums on n channels (n = 72): $DS = \sum ped[i]\ ;\ AS = \sum(-1^i)ped[i]$
  - Incoherent noise $IN = rms(AS)/\sqrt{n}$
  - Coherent noise CN = $\sqrt{var(DS) - var(AS)}/n$
  - Coherent noise fraction : CNF = CN / IN
  - **FlipChip, CNF = 5%. BGA, CNF = 10%**





SiPM version : KCU105-DAQ and Tileboard @DESY |M. Reinecke et al.]

DAQ setup with HGCROC testboard (Omega, LLR) at DESY

- Omega testboard with HGCROCv2 (SiPM version) arrived at DESY.
- H2GCROC2(SiPM version) = HGCROC2 + input current conveyor (Uni Heidelberg design)
- 2.5 V input stage for overvoltage adjustment

Conveyor + preamp stage

ADC path

Need minor adaptation compared to HGCROC for Si

coarse current compensation

Fine current compensation

6-bit DAC

V_{dac}

VDD=2,5V

IN

GND=0V

0,2 0,1 0,05 0,025

Tunable mirror from 0 to 0,4

+/-I_{dac}

R_f

C_f

C_{f_comp}

C_d=5;10;20pF

RtR ampli

7K 0,7K

7,7K

10-bit ADC AGH Cracow

V_{th_tot}

TDC 50ps

TOT path

Identical to HGCROC for Si

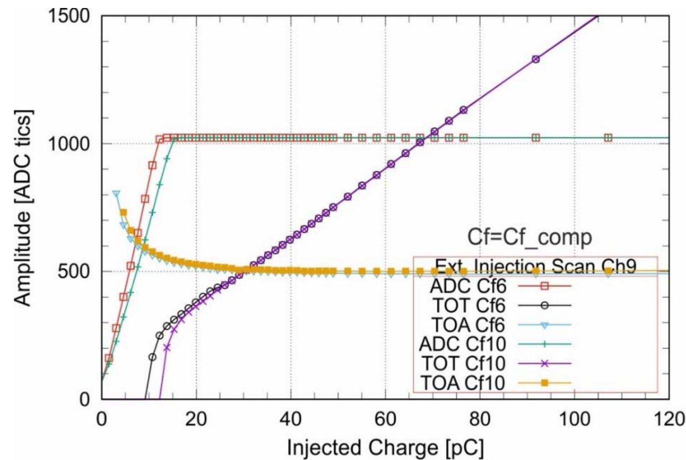
V_{th_toa}

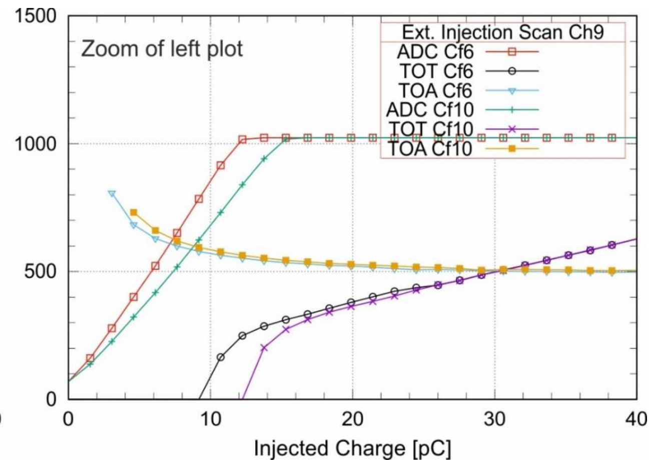
TDC CEA-IRFU 24-12ps

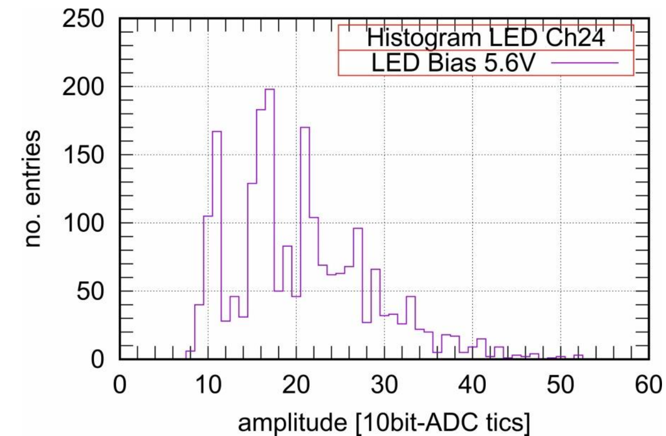
TOA path

Identical to HGCROC for Si

TB1: Ext. Charge Inj. - Dynamic Range



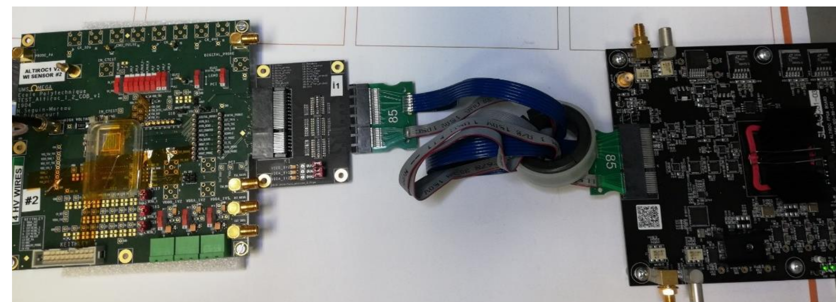


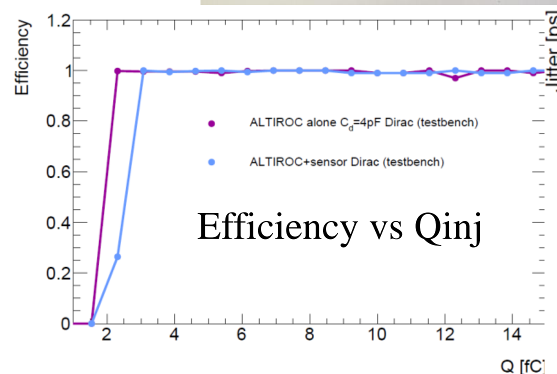


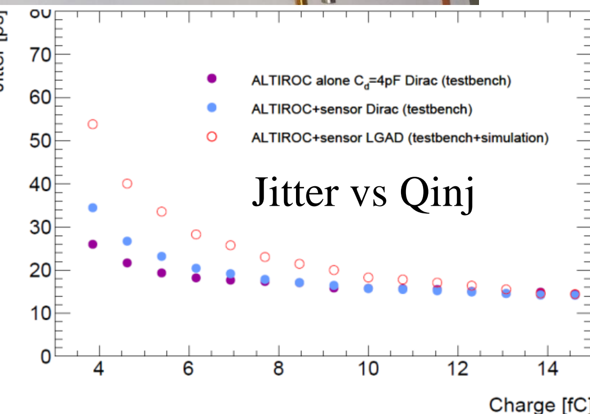
- TOT offset changed (Tot_vref from 432 to 370) to have overlap with ADC.
- (Small) non-linearities in ADC and TOT at ~30pC.
- Dynamic range as expected: TOT (12bit) – 300pC aimed. Problem: At 120pC and 100pF ac-coupling, input voltage pulse is 1.22V. Input DACs at 1.59V. We have to test if higher charges trigger HGCROCv2 protection diodes.
- Still preliminary measurements…
- Default for other gain parameters: Rf=1, Cd=4, ConvGain=4.

ALTIROC

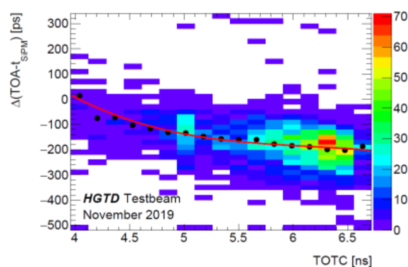
- Test Chip for ATLAS HGTD : MIP timing with LGAD pixels 5x5 of 1.3*1.3 mm ^{2}
  - Collaboration OMEGA, SLAC, SMU
  - Excellent chip performance : 25 ps @ 10 fC testpulse
  - Testbeam in august and november 2019
  - TDR : march 2020



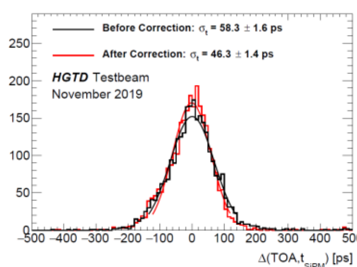




Testbeam

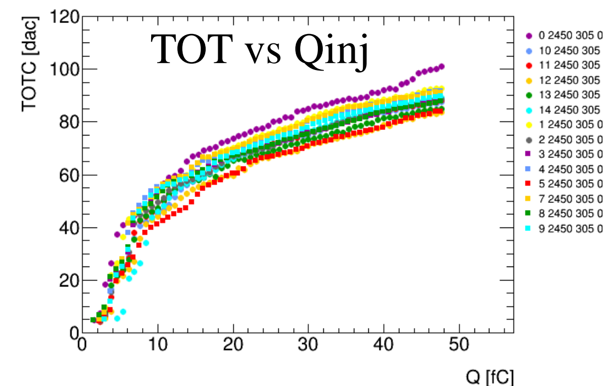


(a)



(b)

Figure 6.15: (a): TOA variation as a function of the TOT. (b): Time difference between LGAD+ALTIROC and the Quartz+SiPM system before and after time walk correction.



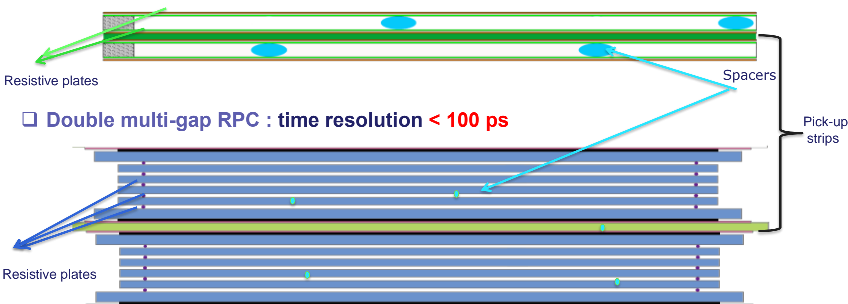
130 nm CMOS blocks and chips

A high-resolution Vernier Ring Oscillator TDC in TSMC 130 nm CMOS for CMS MG-RPC

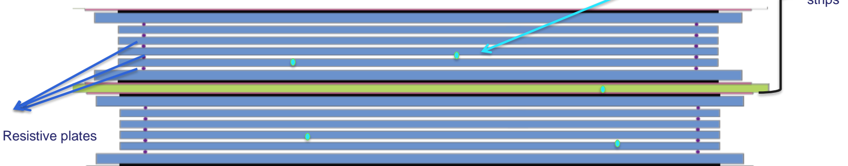
Mokrane DAHOUMANE

Fast-Timing detectors (AIDA-WP13)

❑ **Double single-gap RPC : time resolution < 1ns**



❑ **Double multi-gap RPC : time resolution < 100 ps**

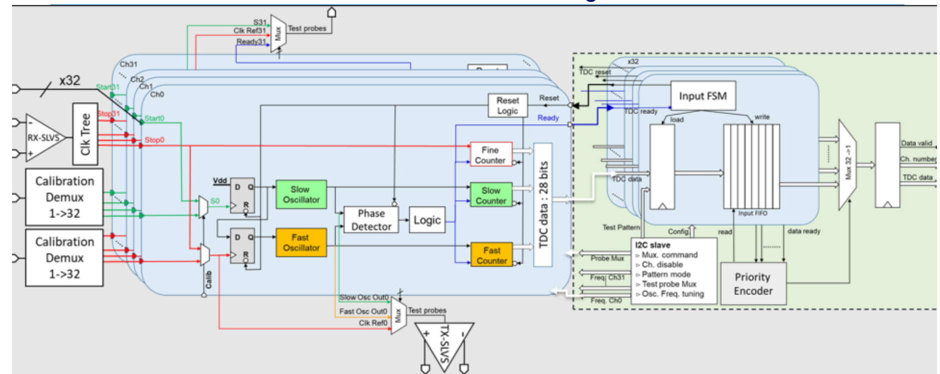


The readout electronics should not degrade the detector resolution

Requirements

- Nominal LSB = 20 ps, tunable
- Time resolution < 2 ps rms
  - the sum of all noise types other than quantization noise (lsb/√12)
- The TDC dynamic range measurement : from 1 ns to 10 ns depending on :
  - TDC reference clock frequency (1GHz, 100 MHz)
- Low power consumption (total power (FEE+TDC) < 3 mW/channel)
- TSMC130nm process.

CRONOTIC2* : block diagram

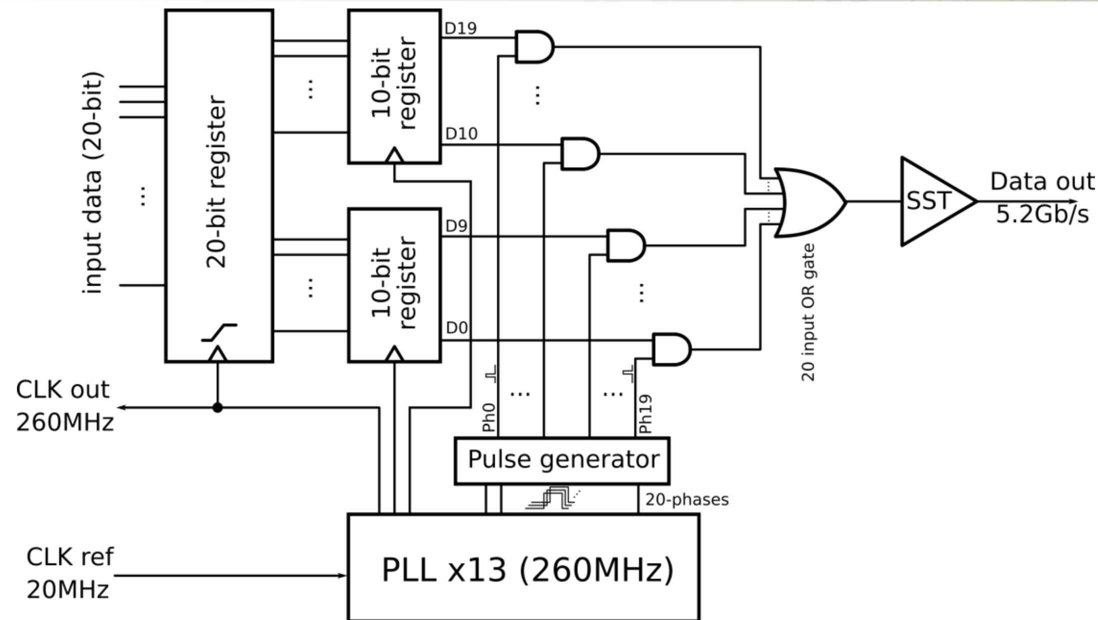


- 32 TDC channels in parallel
- SLVS receiver, SLVS transmitter and clock distribution network
- Acquisition/calibration mode selection logic
- Test probes of internal critical nodes
- Data processing unit with a maximum readout clock <160 MHz

* CRONOTIC : **C**ms **R**pc mu**ON** detec**O**r **T**dc **I**ntegrated **C**ircuit

130 nm CMOS blocks and chips

Developments in TSMC 130 nm
FLAME - fast serializer & transmitter



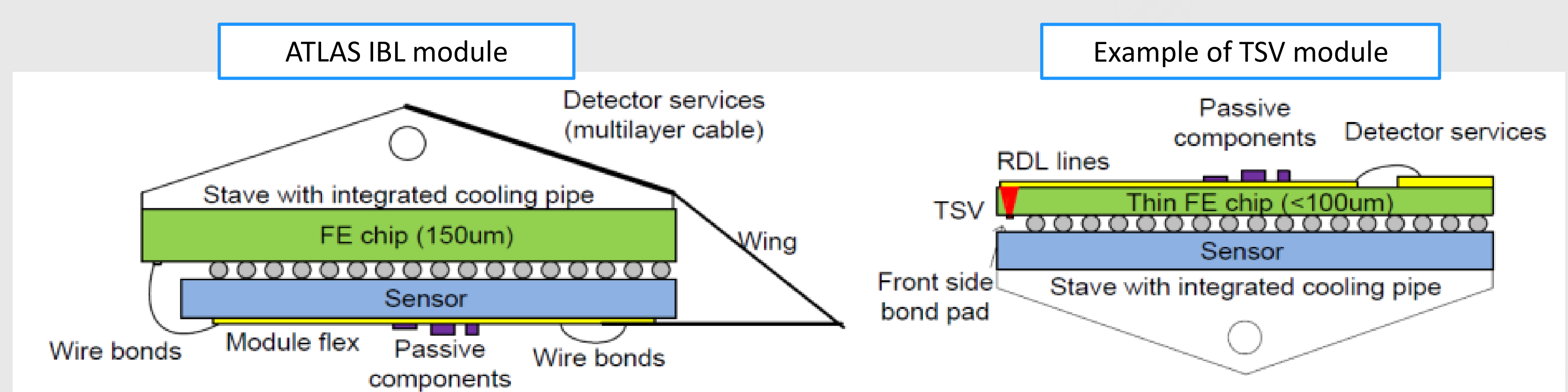
Fast (3-9 Gb/s), ultra-low power (<20mW@5.2Gb/s) serializer plus transmitter, based on multi-phase PLL and SST driver, was designed

WP4.4: Interconnections and TSV

(CERN, INFN-GE, INFN-PV, INFN-PG, CNRS-CPPM, CNRS-LAL, MPG-MPP, UBONN, UNIGLA)

- Produce through-silicon vias (TSV) on wafers with pixel readout chips
- Connect chips with TSV "via last" to detectors from WP7
- Open the way to the adoption of 3D integration technologies in the design of pixel detector systems, with important advantages in terms of pixel form factor, readout speed, reduction of dead areas and of material budget.

- Modules with TSV can be used for the outermost detector layers at the HL-LHC to provide full detector coverage over the large area



Selection of TSV technology

WP4 groups have been working with two different technology providers for Through-Silicon Vias in 130 nm CMOS FE-I4 pixel readout chips:

- IZM **(Bonn)**
- CEA-LETI **(Glasgow, MPI, LAL, CERN)**

The plan was to test processes for peripheral TSVs on the 130 nm FEI4 chip, and apply them to the 65 nm RD53A chip

- Allow for 4 side buttable modules
- Enable wafer-to-wafer assembly
- Remove wirebonds for greater module robustness

The RD53A chip was designed so that it is "TSV enabled" (i.e. , compliant with TSV design rules); this involves the peripheral bonding pad regions

TSVs and RDL with ATLAS FEI4 FE chips: CEA-LETI process

- Project started with CEA LETI on TSV-last process in FE-I4 chips
  - Connect chip M1 metal layer from front to back of chip via TSVs
- Front side processing with either UBM only or bumps
  - UBM only → solder on sensors
  - Bumps → UBM on sensor
- Back side processing ReDistribution Layer
  - Specific FE-I4 layout for laser soldering, same specs as Medipix
  - Pad layout to compensate thermal stress during re-flow after flip-chip (demonstrated to work in previous project between Glasgow and LETI)

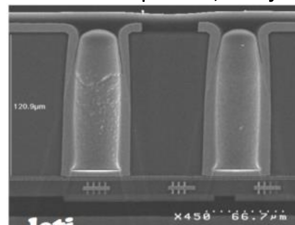
Wirebond less TSV enabling technologies

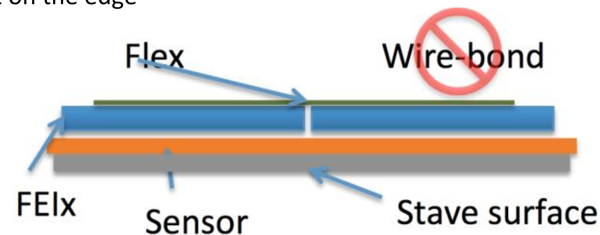
TSV-last + RDL

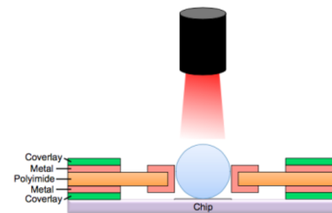
- TSV connect chip M1 from front to back of chip
  - TSV aspect ratio 2:1
- RDL distributes FEI4 connections over full chip surface.
  - Do not need fine-pitch connections.
  - Power can be brought to chip at several places , not just on the edge

Direct laser soldering: flex to FEIx

- Thin 2-layer Al flex
- No glue layer needed
- Connections are solder 1-by-1, module stays at RT
- Re-workable

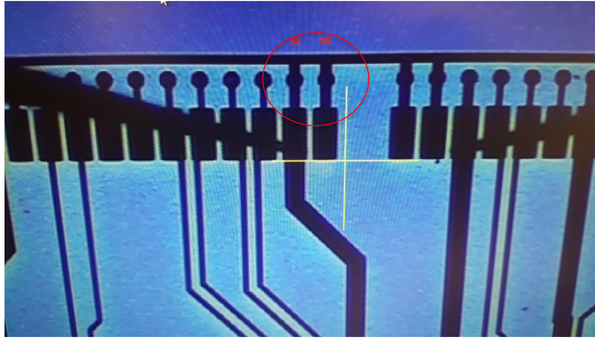






First wafer test results

- Wafer level testing started in Jan 2017
- Soon realised that there was an RDL error



- VDDD line connected to GND bus
  - Error during translation of RDL design to wafer design software
  - Chip not testable
- Probed all power lines and currents reasonable
  - TSVs connected to M1 and isolated from wafer
- Wafers retuned to LETI for FIB
  - Only central die edited due to FIB reach
  - Error corrected
  - Tested on probe – no shorts!

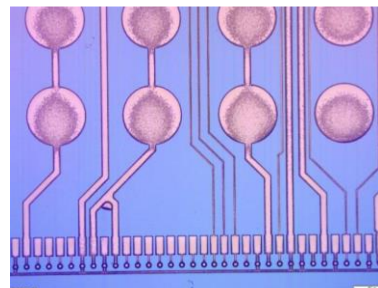
Several problems with TSV and RDL processing confirmed that the via-last technology is not straightforward

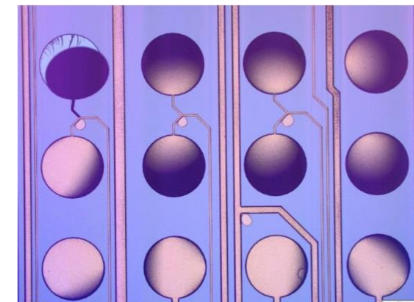
Poor process yield probably due to problems associated with the metal backside redistribution layer (RDL) and with contacts between Through-Silicon Vias and the RDL itself.

Eventually, after a second unsuccessful run of FE-I4 wafers, this activity was stopped by CEA-LETI

First RDL results

- Excessive copper applied
  - Aim was to reduce TSV resistance
  - 6-8 µm requested c.f. standard thickness < 5 µm
- Caused delamination of large RDL laser solder pads
  - Pulling away underlying oxide layer as well
  - 1 of the 3 wafers not so bad and useable for module building
- TSV contact on front side metal : low and repeatable contact between 2 ground TSVs
  - 6 Ohm including RDL line and probe resistance

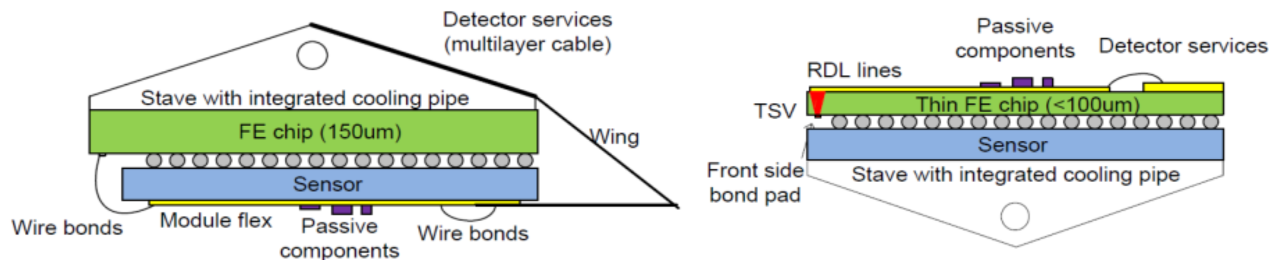




UNIVERSITÄT BONN SI LAB Silizium Labor Bonn Fraunhofer IZM

Advanced Through Silicon vias for Pixel Detectors

F. Hügging, N. Owtscharenko, N. Wermes (U Bonn)
T. Fritzsch, O. Ehrmann, K. Zoschke (Fraunhofer IZM)

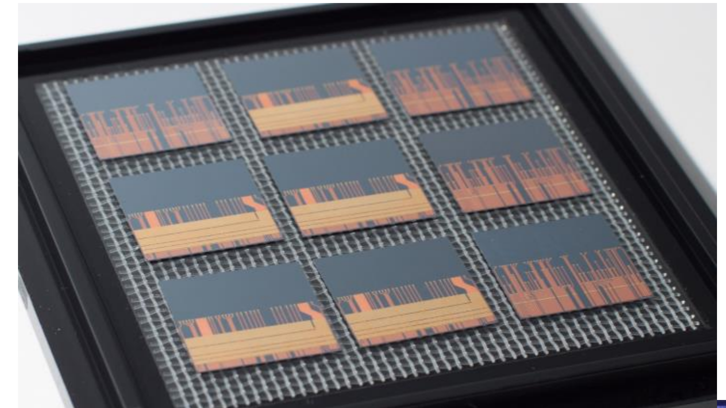


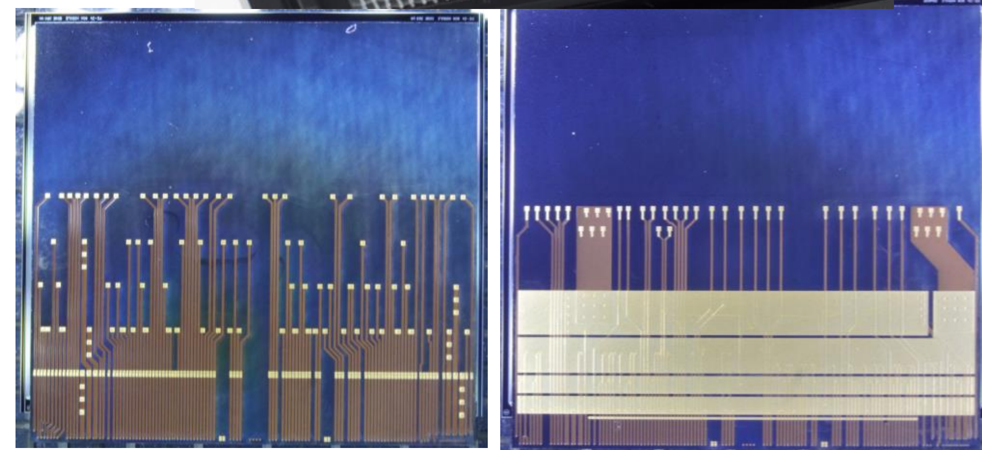
- **TSVs** + wafer thinning + aligned bonding are the key technical elements for a 3D extension of electronics integration -> eminent field of industrial research
    - denser packaging - lower power - larger I/O bandwidth - more functionality at lower cost
- **Promise** for pixel detectors → more compact modules with active area maximization, no wire bonds, and 4-side abuttable (X-ray), use backside for wiring (RDL) → **joint interest Bonn - IZM**
- **Needs/challenges** which both partners profit from
    - large length and relatively large aspect ratio (length/diameter) TSVs with reliable fabrication yield
- Goal: **develop pixel modules for HL-LHC** employing TSVs in a via-last process (after CMOS process) achieving a high yield (≥ 80%) on thinned wafers (down to 80 µm)

Bare chips with TSVs (Bonn, IZM)

On test wafers, measured values of TSV resistance (about 15 mΩ for individual TSV) and capacitance (about 40 fF in a first wafer and about 120 fF in a second one) appear adequate for peripheral TSV, also in the case of I/O digital lines operated at a moderate frequency (160 Mb/s).

- 3 FE-I4 Wafers have been successfully processed with TSV and 2 different RDL types:
  - Simple 1 layer RDL just copying the WB pad frame with the Cu used for the TSV filling
  - 2 layer RDL connecting all WB pads for the power nets: VDDD, DGND, VDDA, AGND. Used the Ni/Au layer for the pads

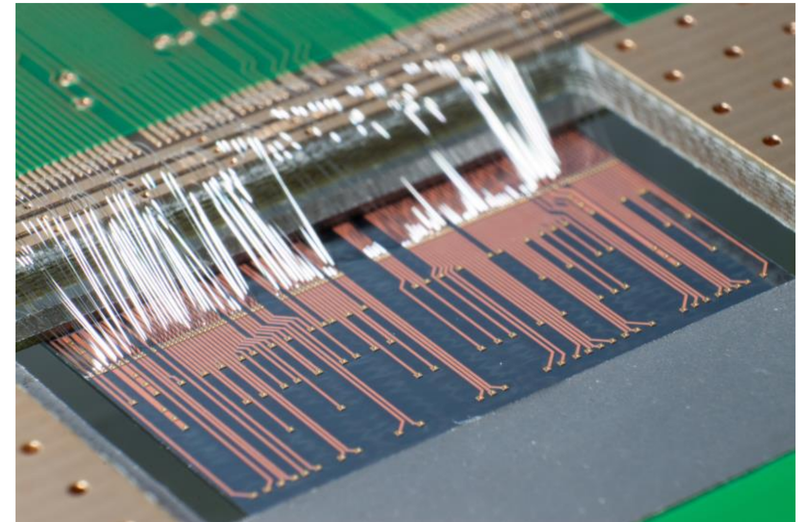


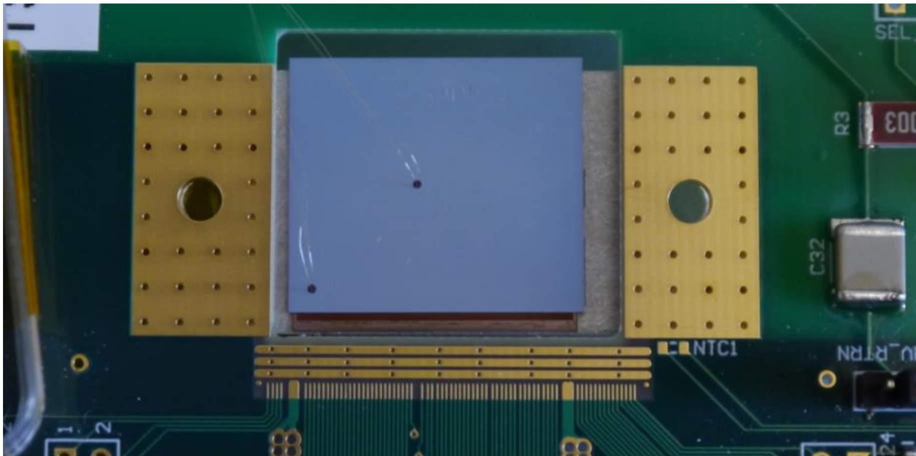


- Performance in terms of noise, threshold dispersion and data transmission similar to standard FE-I4 chips.
- On average, at 2000 electrons threshold, Equivalent Noise Charge about 120 e rms

Pixel modules with TSVs (Bonn, IZM)

- 8 modules with sensors have been built:
  - Assembly onto MPG HLL planar sensor (thanks to A. Macchiolo from MPI)
  - Sensor wafers have deposited with SnAg solder bumps



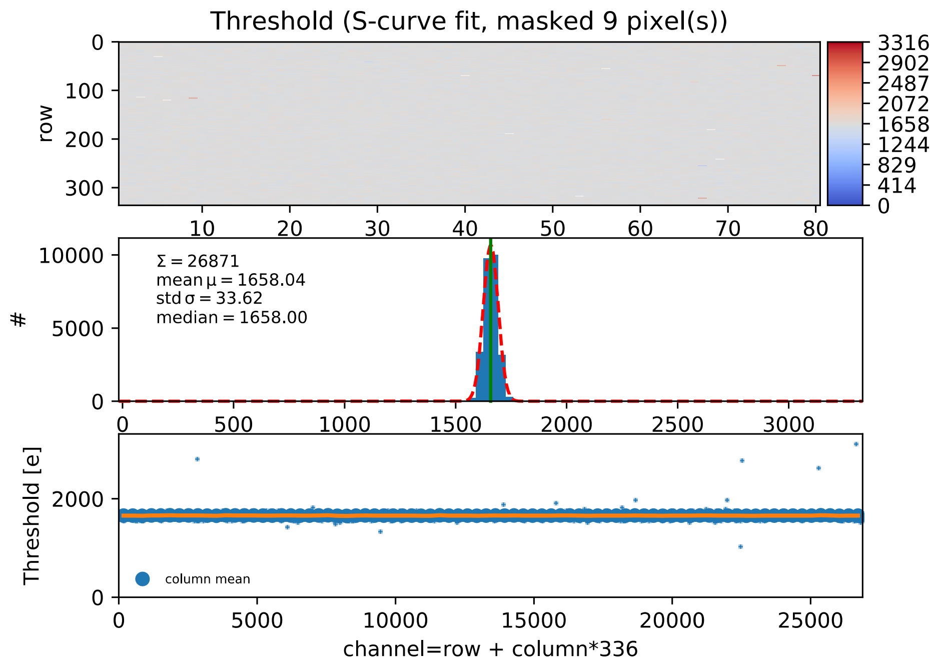


Cross section of module with 80µm thick ATLAS FE-I4 backside TSV ROC

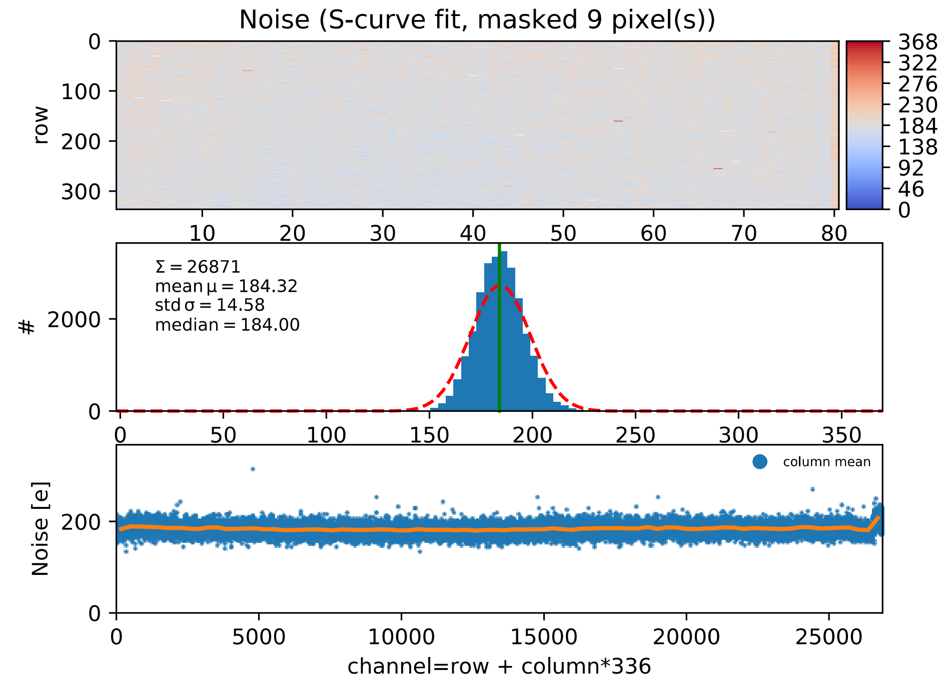
Modules with TSVs: Results

- 2 modules have been tested, both working nicely
  - Very good bump connectivity, one module shows a few disconnected pixel at one edge (maybe handling issues during BB)
  - Noise is about 180e$^-$ at 1650e$^-$ threshold with a dispersion below 40e$^-$

Tuned threshold, 60V



Noise, 60V



The excellent outcome of this activity provides a **demonstration of the feasibility of pixel modules where TSV technology is used to improve the detector performance** in terms of reduced material budget, increased active area, and improvement of assembly and handling.

TSV deliverable

The original plan of WP4 Task 4.4 envisaged to apply TSV processing to 65 nm CMOS wafers with the RD53A pixel readout chip

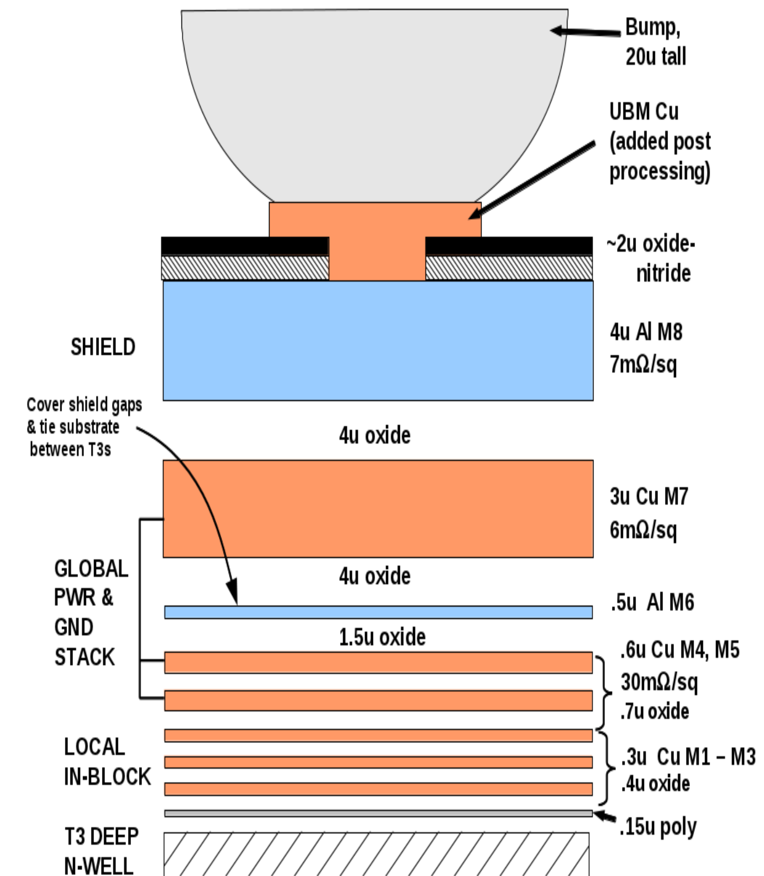
The RD53A chip was developed following the correct design rules for TSVs in its peripheral regions.

Wire bonding pads in RD53A are compatible with TSV fabricated with a backside etching process, such as the one already successfully tested in 130 nm CMOS wafers with the FE-I4 chip.

However, the **130 nm and 65 nm CMOS node share similar process features as far as TSV processing is concerned.**

Peripheral wire bonding pads have all metal layers from M1 to the actual aluminum pad. Peripheral TSV for I/O interconnection can be etched across the silicon substrate reaching the lowest metal levels (M1-M3) in the stack, which are then internally connected to the thicker upper metals and finally to the bonding pad.

It is then reasonable to assume that TSV processing in a 65 nm wafer will give the same results that were found in 130 nm wafers.



TSV deliverable

The excellent results achieved by UBONN with pixel modules and FE-I4 chips provide a demonstration of the feasibility of TSV and of the related processing steps in 100 nm-scale CMOS pixel readout chips.

These results can be the basis for future designs of advanced pixel detector modules using nanoscale CMOS readout chips.

The extension of this study to 65 nm CMOS wafers was deemed to be unnecessary, considering that the 130 nm CMOS technology and the 65 nm one are very similar as far as TSV processing is concerned.

AIDA WP4 deliverables

- D4.1 CMOS 65 nm engineering run *(availability of the run with the "ATLAS/CMS" and CLICPIX pixel chips)* (CERN)

  M36 (April 30, 2018) ACCOMPLISHED

- D4.2 BICMOS SiGe engineering run *(availability of run with SiPM calorimeter-WP14 and gas detectors-WP13 chips)* (CNRS)

  M36 (April 30, 2018) ACCOMPLISHED

- D4.3 Through Silicon Vias production *(fabrication of TSV in wafers of deliverable 4.1)* (INFN)

  M54 (October 31, 2019) ACCOMPLISHED

AIDA WP4 milestones

MS4.1	Architectural review of deliverable chips in 65nm run	M14 (accomplished)
MS4.2	Final design review of 65nm	M30 (accomplished)
MS4.3	Test report of deliverable D4.1	M46 (accomplished)
MS4.4	Selection of SiGe foundry	M14 (accomplished)
MS4.5	Final design review of deliverable chips in SiGe run	M30 (accomplished)
MS4.6	Test report of deliverable D4.2	M46 (accomplished)
MS4.7	Selection of TSV process	M14 (accomplished)
MS4.8	Final design review of deliverable D4.3 (TSV in 65nm)	M30 (accomplished)
MS4.9	Test report of deliverable D4.3	M58 (accomplished)

WP4 summary

- WP4 has achieved deliverables and milestones for chips in 130 nm and 65 nm CMOS; these chips were made available to other AIDA2020 WPs and are intensively used for sensor R&D and qualification

- Networking and collaborative projects were effectively supported by WP4 for the development of chips for HEP experiments

- The feasibility of Through-Silicon Vias in 100-nm scale CMOS wafers was demonstrated, fulfilling WP4 plans; the future application of these techniques will depend on a reliable access to industrial 3D integration technologies

- Future advances in HEP detector performance will rely on the progress of microelectronic technologies; the complexity of design and testing in advanced CMOS generations needs to be supported by our community, as it was done by AIDA2020