

Muon ECS Upgrade*



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Abstract

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1 Introduction

The Muon detector of the LHCb experiment, after the ongoing major upgrade, will be composed of only 4 stations (instead of the previous 5) which will comprise 1104 multi-wire-proportional-chambers (MWPC) with more than 100000 readout channels.

- In the nECS all ELMB will disappear;
- The CAN BUSES will be replaced by the bi-directional and very fast GBT links;
- So far the WCC-OA communicated with the CAN by means of the OPC server (the WCC-OA being a client);
- The hardware link was provided by the SYSTEC interface (connected to control PC via USB lines);
- The latter will be replaced by SOL-40 boards mounted onboard of the control PC;
- The OPC server will be replaced by a DIM server running on the SOL-40 FPGA.

Instead of current OPC communication protocol, we are going to use DIM (the one used for the TELL1 in current system). A DIM server will run on the SOL-40 and WinCC-OA projects will be DIM-clients (instead of OPC-clients). There will be:

- a component for low-level functions called fwGBT;
- a fwHw component, which allows us to describe the boards, in terms of I2C registers for example;
- a tool that creates the datapoint types (and then datapoints);

The boards can be described either via a user interface or via XML files.

2 Detector Description

The Muon detector is composed of four rectangular stations, M2-M5, with a projective geometry pointing to the interaction point (IP), so with dimensions scaling linearly with distance from the IP. Each station is made of 276 MPWCs, of different dimensions divided, in turn, in 4 regions: R1-R4, with increasing distance from the beam axis. In total the Muon detector comprises 16 different types of MWPCs: M2R1 ... M5R4 for a total of 1104 MWPCs.

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 The detector readout electronics consists of a Front End Board (FEB) that includes amplifier, shaper, discriminator and logical signal combination stages (by means of two custom asics, the CARIOCA and the DIALOG), directly connected to the MWPC chambers and the off detector electronics placed on the Muon towers.

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 nODE: The signals coming from the DIALOG are processed in the new Off Detector Electronic (nODE) boards. The nODE manages up to 192 input channels and it is based on a radiation tolerant custom ASIC, the nSYNC, which integrates all the required functionalities: clock synchronization, bunch crossing alignment, data hits production, time measurements, zero suppression algorithm for the TDC data, histogram capability and buffers. Four optical unidirectional up-link, using GBTx and Versatile link components, are used for the communication with the back-end electronics (TELL 40 boards) and 1 optical bidirectional link is used for the TFC/ECS interface.
 nSB/nPDM

3 Communication scheme

3.1 Front-End electronics

The nSB will control, via 12 I2C lines, the FEB (Front End Boards) on the chambers (up to 6 FEB/line). Via eLINKs on a custom backplane, each nPDM will communicate with several nSB each one containing one GBT-SCA and each nPDM will communicate with one SOL40 as shown in Fig. 1.

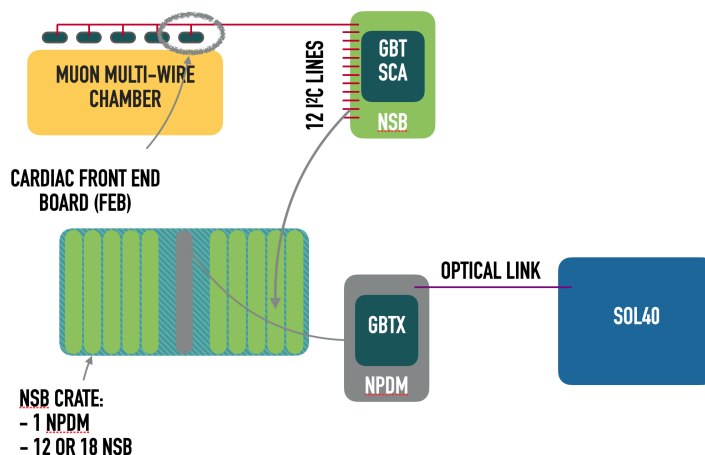


Figure 1 Front-End electronics communication scheme.

Chambers will be on 4 Muon Station (M2-M5), subdivided in 4 Quadrants and 2 Sides as shown in Fig. 2.

We will have 8 crates, for a total of 120 nSB and 8 nPDM as shown in Table 2.

Each Station will have the same number of Chambers with different granularities: i.e. with different number of FEB as shown in Table

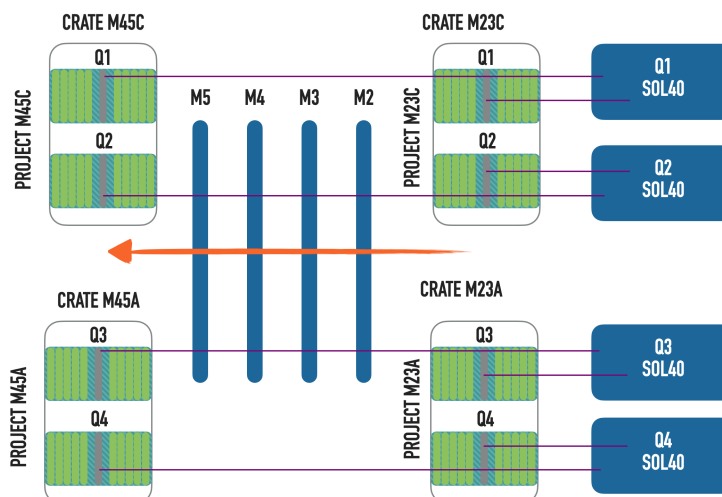


Figure 2 Front-End electronics communication scheme.

Crate	nSB	nPDM
M23Q1A	18	1
M45Q1A	12	1
M23Q2A	18	1
M45Q2A	12	1
M23Q3C	18	1
M45Q3C	12	1
M23Q4C	18	1
M45Q4C	12	1
Tot	120	8

Table 1 Number of new Service Boards and Pulse Distribution Module per Crate.

Station	Number of ch	Number of FEB
M2	26496	1656
M3	25960	1560
M4	18432	1152
M5	18432	1152
Tot	89320	5520

Table 2 Number of new Service Boards and Pulse Distribution Module per Crate.

3.2 Off Deetector electronics

To manage the needs of the LHCb-MUON apparatus we'll use a total of 148 nODE. Each quadrant will be served by 37 nODE, placed in several crates. So, from the ECS point of view, we'll need a total of 148 fiber links (up and down) toward the 4 GBT-SCA (one per quadrant).

3.3 Low Voltage and cooling system

We keep DCS the same as now for LV, HV and cooling systems on M2-M5. All WINCC-projects should be modified in term of removing M1. For the Low Voltage supply there will be 16 MARATONs (two per Rack)

- 8 for the Cardiac Board supply;
- 8 for Front-End and Off-Detector board supply.

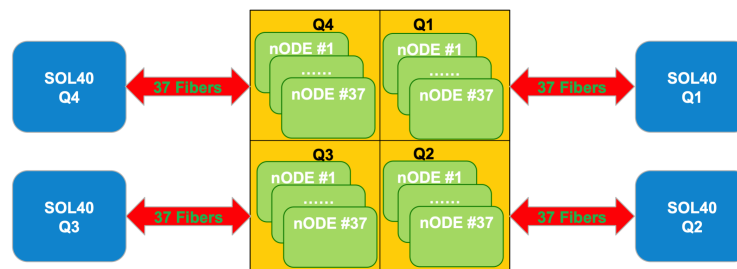


Figure 3 Off Detector electronics communication scheme.

For proper cooling of Low Voltage supplies in the Racks will exploit water cooling for MARATONS and air cooling (there will be one big turbine per side sucking air from inner regions). Water leak systems will be installed in all 8 racks.

3.4 High Voltage power supply

The high voltage to MWPC will be provided by two different systems:

- **CAEN HV for R1-R2 regions:** D3: 2 mainframes and 2 48V PS + CARBON PS; Cavern: 4 EASY3000 crates (2 per side, placed in M4M5 Racks in Q2 and in Q3) with installed 18 (9 per side) A3535P boards (32chs); Control: 2 CCPCs (OPC-servers) - 2 WINCC-projects (1 per side) Remove HV-GEM project;
- **PNPI HV for R3-R4 regions:** D3: 2 MATSUSADA PS, 1 HVM control unit, 2 crates with 16 (8 Masters per side) MASTERS (8chs); Cavern: 112 RDB boards (36 chs each), 2 crates per Rack (8 per side) Control: 2 CCPCs (OPC-servers) - 2 WINCC-projects (1 per side)

4 Hierarchy

5 Hardware Infrastructure

6 Front End Electronics

There will be 4 projects [M23A, M45A, M23C, M45C]: 2 managing 1608 FEB; 2 managing 1152 FEB; For a total of 5520 FEB with 93 registers (1B) per FEB: 48 readout only; 45 Bytes to be configured; nSB 180 1B regs and nPDM 40 1B regs;

6.1 Pulse Distribution Modules

6.1.1 Data Point Structure

6.1.2 Libraries and Function structures

6.1.3 High level panels

6.2 Service Boards

7 Off Detector Electronics

8 High Voltage System Control

9 Low Voltage System Control

10 Tell40 Control

11 Conclusion

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