AIDA-2020 WP5: Trigger(/timing/tagging) Logic Unit

After AIDA-2020 ?

David Cussans, 28/April/20

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Documentation

- New publication
  - https://doi.org/10.1088/1748-0221/14/09/p09019 “The AIDA-2020 TLU: a flexible trigger logic unit for test beam facilities” , JINST
- Open Hardware project “AIDA-2020 TLU”
  - https://ohwr.org/project/fmc-mtlu
  - Hardware design files
  - Firmware source code
  - User manual
  -

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TLU Production

- New hardware version
  - Minor bug fixes (saves effort hand-patching)
  - Three PCBs produced.
    - Delivery due 29 April
    - Only basic test facilities available (in a domestic setting)
    - Verify design for production run
      - See Lennart Huth

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TLU Firmware

- Bug fixes/Enhancements waiting testing:
  - Firmware took trailing (not leading) edge of negative going pulses
    - Active edge now selectable
      - Needs extra register in EUDAQ
  - Firmware only recorded 5-bits of fine-grained (1.28GHz) time-stamp
    - Wrap-around of 25ns master clock possible.
    - Now records 8-bits of find-grained time-stamp. Should allow wrap-around to be resolved
  - Bugs found by Jens Kroger
  - Hopefully Bug-fixes will be tested soon
- Planned enhancement:
  - Each TLU has a unique ID chip and EEPROM. Intended to provide MAC address and storage for IP address.
  - Firmware to add a soft-core microprocessor to set IP address (interaction by USB UART) half written then work halted. Hope to complete work this year.
- Possible enhancement – use external RAM to increase time-stamp/trigger-information buffer depth (4096 → 4M)
  - Does anybody want this?

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AIDAInnova TLU

- Aim: (tens of) Picosecond Timing
  - EUDET TLU – Precision ~ 100ns
  - AIDA/AIDA-2020 – Precision ~ 1ns
- Use external TDC chip
  - PicoTDC ?
- ADC for time-walk correction?
- ~ 8 inputs
- >= 4 “DUT Interfaces

  Move away from HDMI → Display Port

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