

AIDA²⁰²⁰

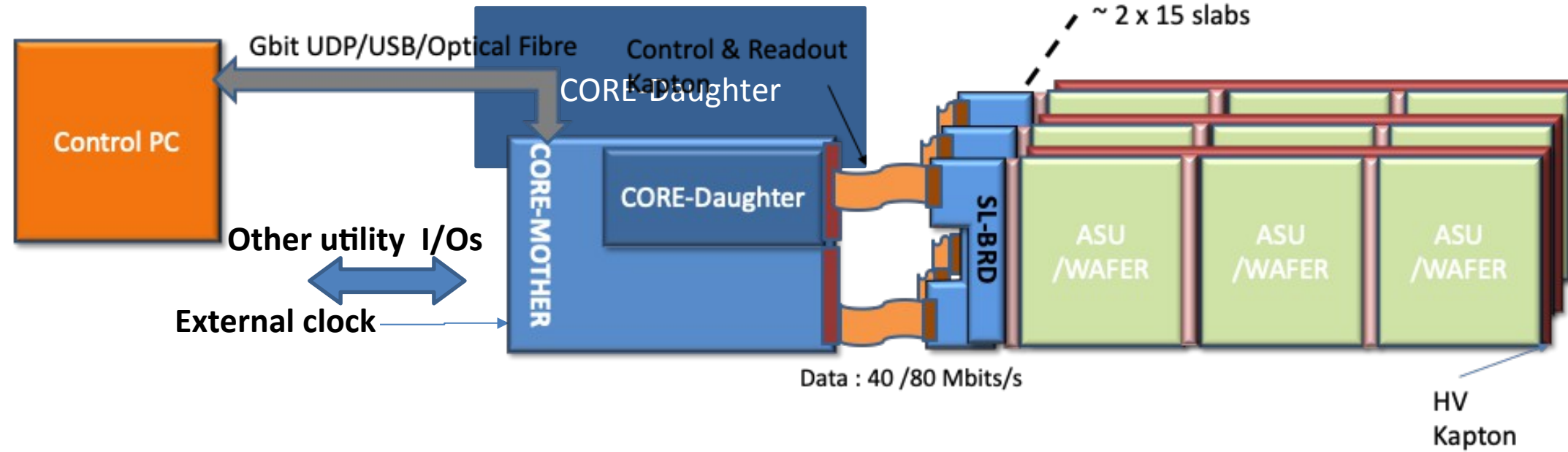
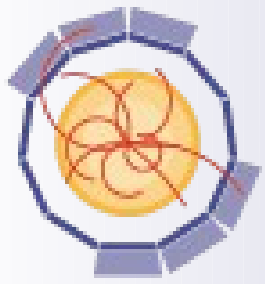
Advanced European Infrastructures for Detectors at Accelerators

Elements of CALICE/WP14 SiW Ecal readout and rough plans for the future

R. Pöschl based on work by Jihane Maalmi, Dominique Breton, Jimmy Jeglot, Adrian Irlles (and Jiri Kvasnicka)



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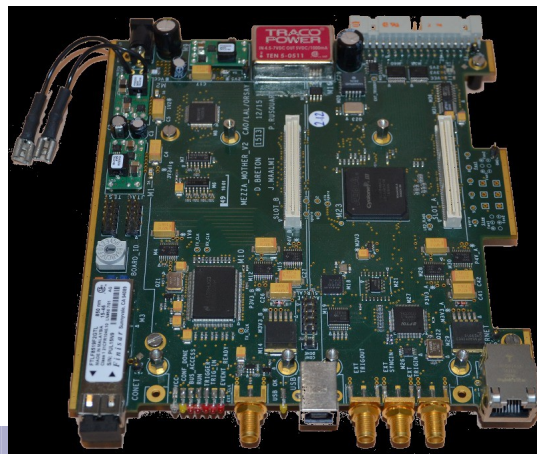
CORE Module/Mother/Daughter : Control and Readout
 SL-BRD : Interface board to Slab

**External clock and Utility I/Os : possibility to be synchronised with other systems!
 i.e. TLU**

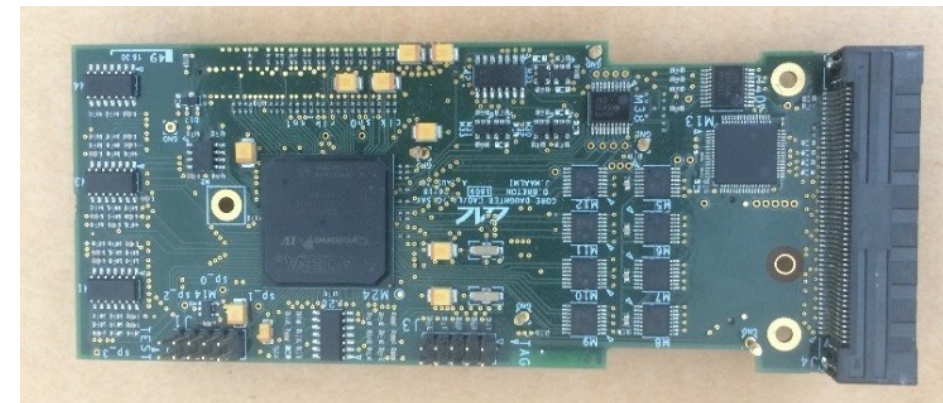
The « magic box » CORE Module

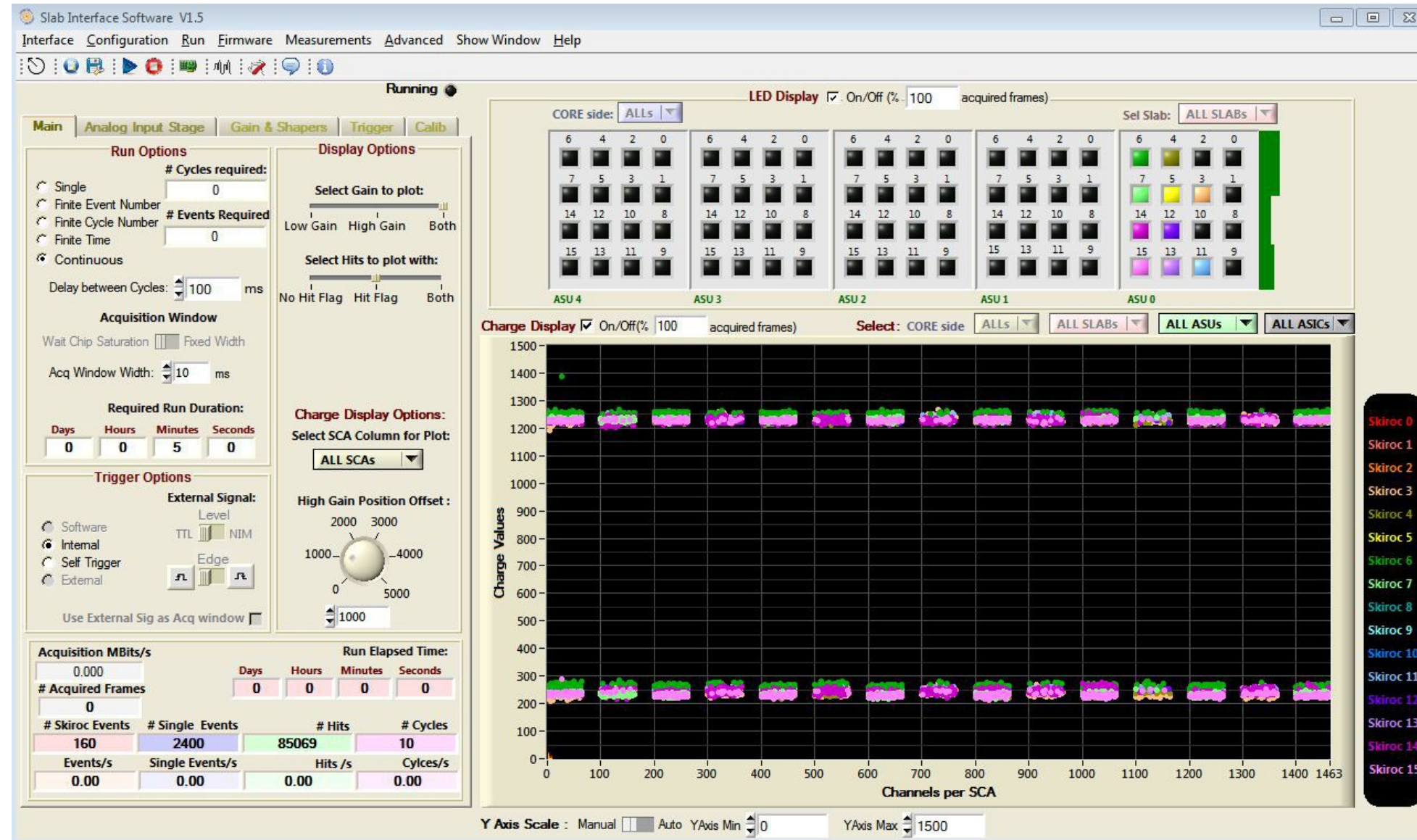
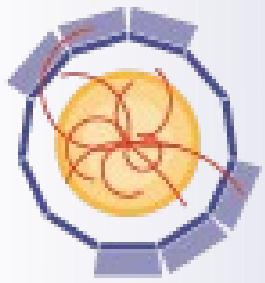


CORE-Mother



CORE-Daughter





- The Software can handle the communication through FTDI connector or through **CORE Module**.
- It handles the **whole detector module**:
 - **Two sides with 15 SLABs each.**
 - **Each slab with up to 5 ASUs.**
- It written in **C** under **Labwindows CVI**
- Advanced measurements can be performed Online such as threshold scans...
- The C-functions that handles the communication (readout and configuration) can be used as a library with any other program that handles C-language.

- ECAL stack will/does comprise around 15-20 layers in 2020
- Need to make standalone tests but at a very early stage also first exercises with e.g. AHCAL to prepare combined testbeams
 - First tests on synchronisation between detectors with separate data streams (was planned for March 2020)
 - Then « full » combined running using EUDAQ for data acquisition
 - Not difficult says Adrian but needs to be done, did not have priority for March but is in the planning
- At one point we will for sure want to take data with telescopes
 - => usage of TLU, signals can be received via CORE Module
 - Interaction with other systems is inherent to system design !!!!
- Details need to be worked out by experts but we clearly envisage to make use of the tools developed in WP5