AIDA2020 Project
Wp7 IMB-CNM Activities

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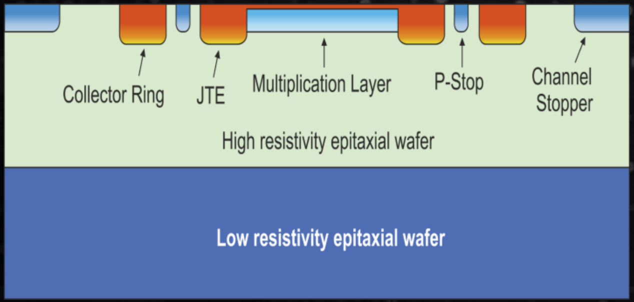
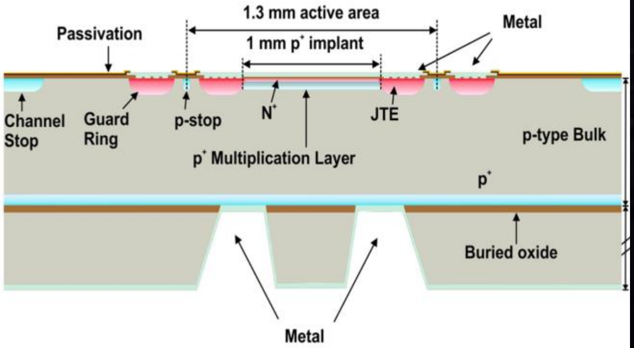
Fabrication Processes

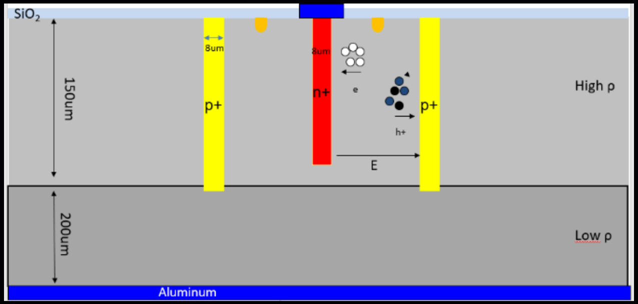
- LGAD
  - Run 11748. AIDA2020 v1
    - 4”, 35/50+300 µm thick Si-Si. 14 Wafers
    - N⁺-Layer do not overhang Multiplication Layer
    - High Leakage current due to a problem in the multiplication layer periphery



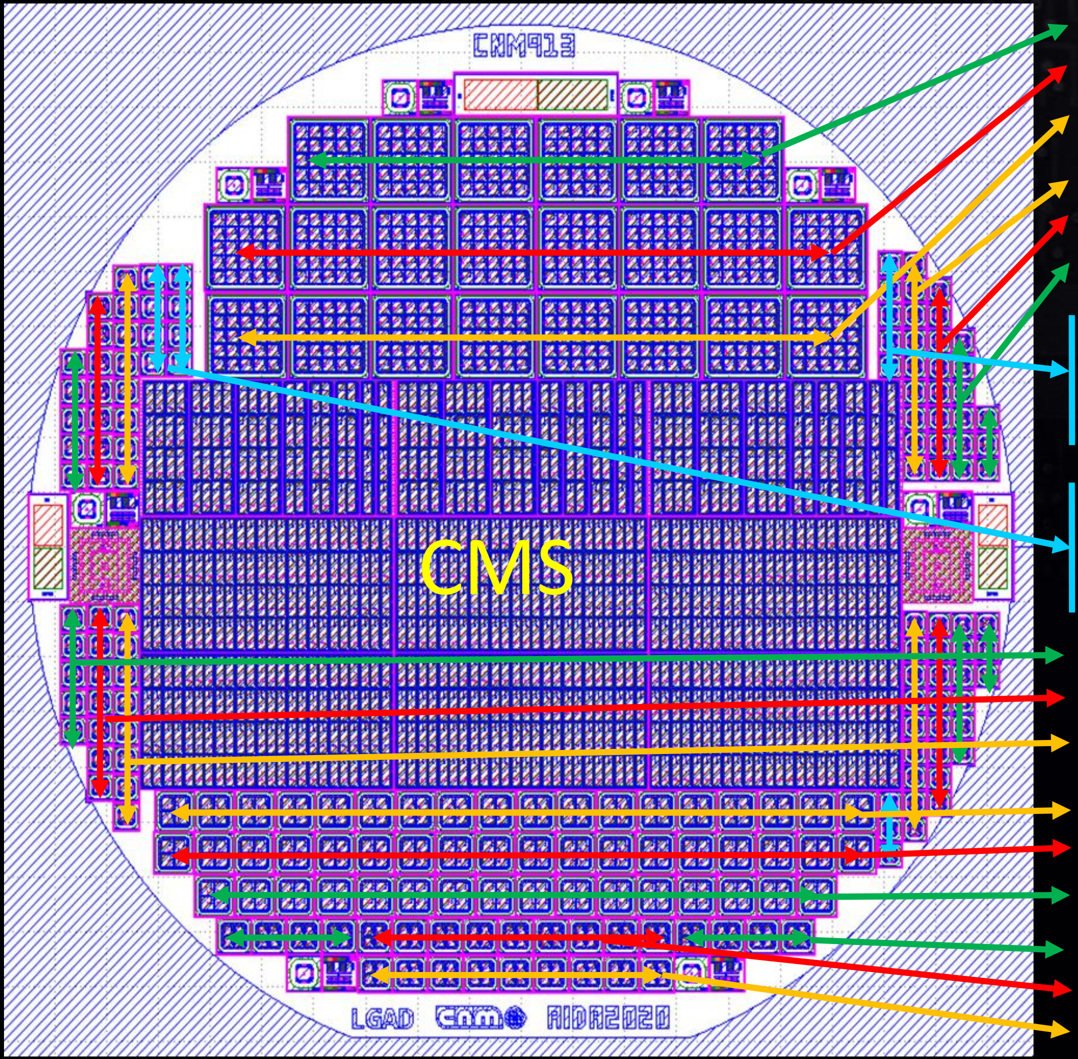
  - Run 12916. AIDA2020 v2
    - 4”, 50+300 µm thick Si-Si. 4 Wafers
    - N⁺-Layer overhang Multiplication Layer
    - Low Leakage current
  - Runs 11486 & 13002. 6 inch Thin LGADs
    - 6”, 50+1+300 µm thick SOI. 7 Wafers
    - 6”, 55+525 µm thick EPI. 4 Wafers



  - ATLAS/CMS Common Run
    - AIDA2020v2 design in 6 inch SOI & Epitaxial wafers
- 3D
  - Run 11119. **3D-SS**, RD53A, AIDA2020
    - 4”, 150+200 µm thick Si-Si. 8 Wafers



LGAD. AIDA2020. Runs 11748 & 13002



ATLAS 5x5, 1.3 mm, IP 37
ATLAS 5x5, 1.3 mm, IP 47
ATLAS 5x5, 1.3 mm, IP 57

LGAD Pad, 1.0 mm, IP 57
LGAD Pad, 1.0 mm, IP 47
LGAD Pad, 1.0 mm, IP 37

PiN Pad, 1.0 mm, IP 37
PiN Pad, 1.0 mm, IP 47
PiN Pad, 1.0 mm, IP 57

PiN Pad, 1.3 mm, IP 37
PiN Pad, 1.3 mm, IP 47
PiN Pad, 1.3 mm, IP 57

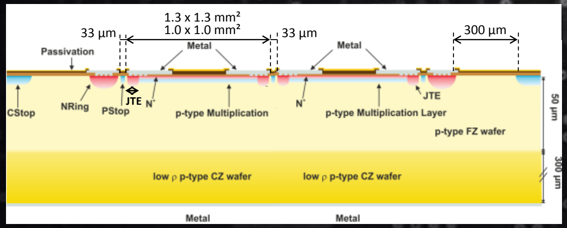
LGAD Pad, 1.3 mm, IP 37
LGAD Pad, 1.3 mm, IP 47
LGAD Pad, 1.3 mm, IP 57

ATLAS 2x2, 1.3 mm, IP 57
ATLAS 2x2, 1.3 mm, IP 47
ATLAS 2x2, 1.3 mm, IP 37

ATLAS 2x2, 1.0 mm, IP 37
ATLAS 2x2, 1.0 mm, IP 47
ATLAS 2x2, 1.0 mm, IP 57

LGAD. AIDA2020 v1. Run 11748

- LGADs for ATLAS & CMS Timing Layers
  - 4 inch, 35/50+300 μm thick Si-Si. 14 Wafers
  - N⁺-Layer do not overhang Multiplication Layer (do not overlap JTE diffusion)
  - We use three different implantation dose values for the multiplication area (2,3,8,9 low; 4,5,10,11 medium; 6,7,13,14 high)
  - Wafer 1 integrates PiN diodes only
  - Wafers 3,5,7,9,11,14 do not use temporary metal and they have been tested on-wafer using some single pad devices to evaluate the fabrication process quality
  - We have use temporary metal on wafers 1, 2, 4, 6, 8, 10, 12, 13, only
  - High Leakage current due to a problem in the multiplication layer periphery



Without Temporary Metal

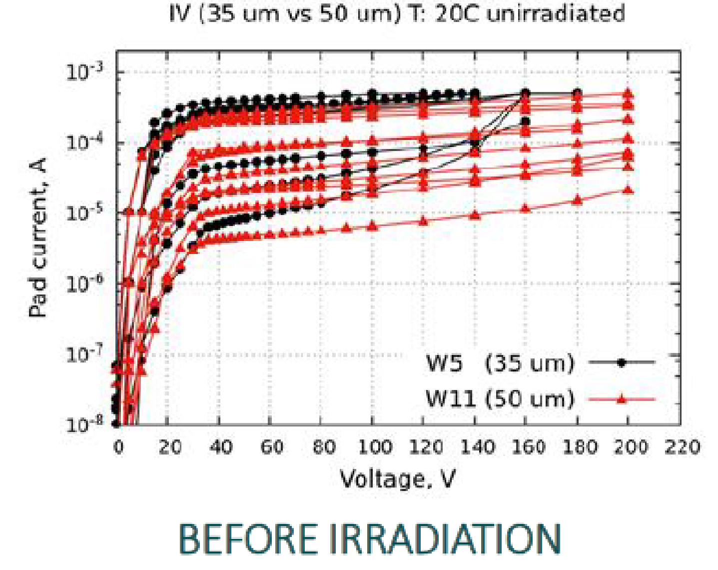
Wafer	Thickness	Dose
3	35 μm	Low
5		Med
7		High
9	50 μm	Low
11		Med
14		High

With Temporary Metal

Wafer	Thickness	Dose
1	35 μm	PiN
2		Low
4		Med
6		High
8	50 μm	Low
10		Med
12		Med-High
13		High

LGAD. AIDA2020 v1. Run 11748

- LGAD have high leakage currents (≈mA) but pin diodes are working well (nA)
- Current is not generated in the bulk, all other parameters are OK (gain, breakdown voltage, capacitance, depletion voltage of the multiplication layer, surface current, etc.)
- High current due to a mistake in the N$^+$ mask level design that was implemented in all devices (no in pins). The reason was to try to increase the JTE performance
- IFCA work show that leakage current decreases with irradiation and the detectors can be operated normally
- New N$^+$ mask level design to avoid this problem

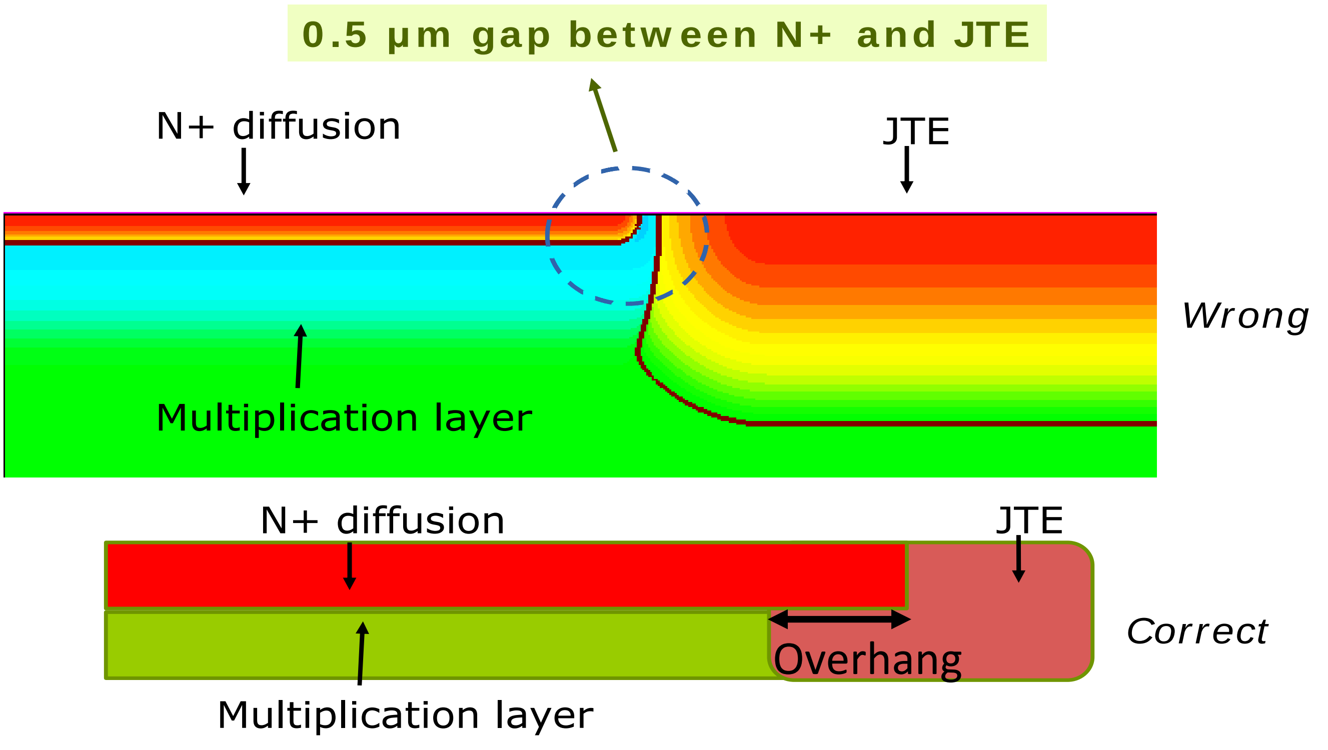


BEFORE IRRADIATION

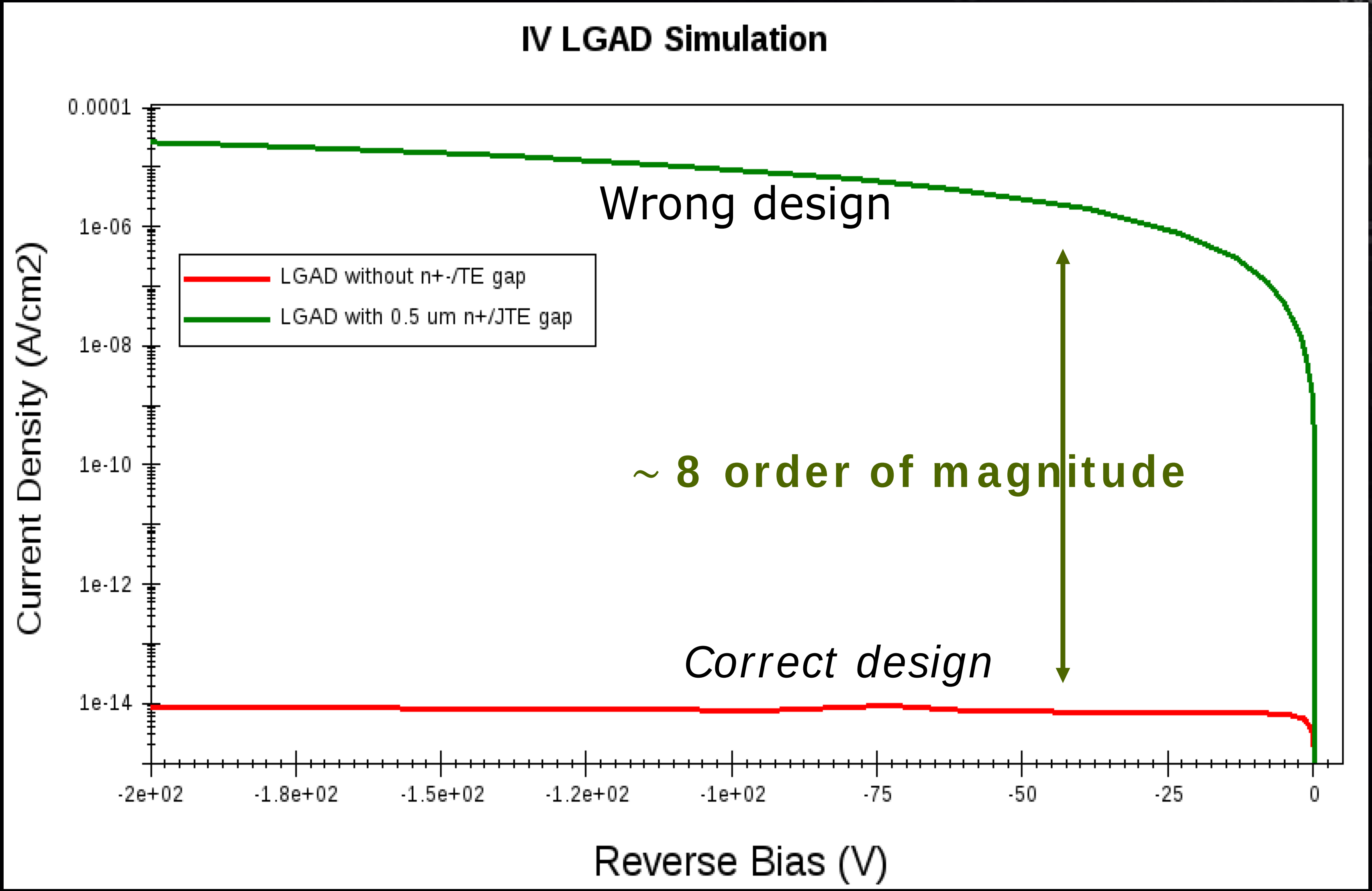
Ivan Vila. TREDI 2019. Trento. February 2019

LGAD. AIDA2020 v1. Numerical Simulations

- If we reduce the overlap between the N$^+$ and JTE diffusions on the multiplication layer, the doping in that area might not be compensated, inducing a parallel p-type resistor that connect the anode with the cathode

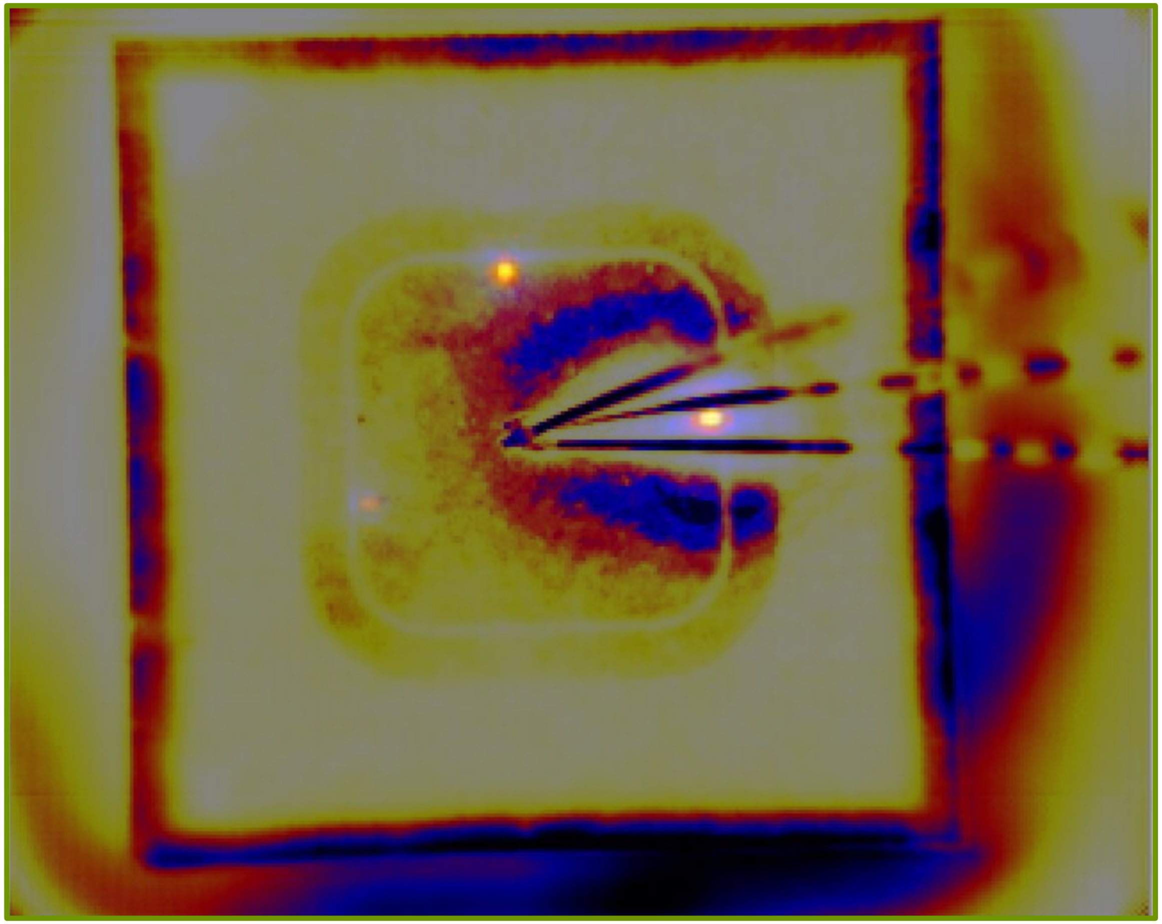


LGAD. AIDA2020 v1. Numerical Simulations



LGAD. AIDA2020 v1. Thermographic Measurements

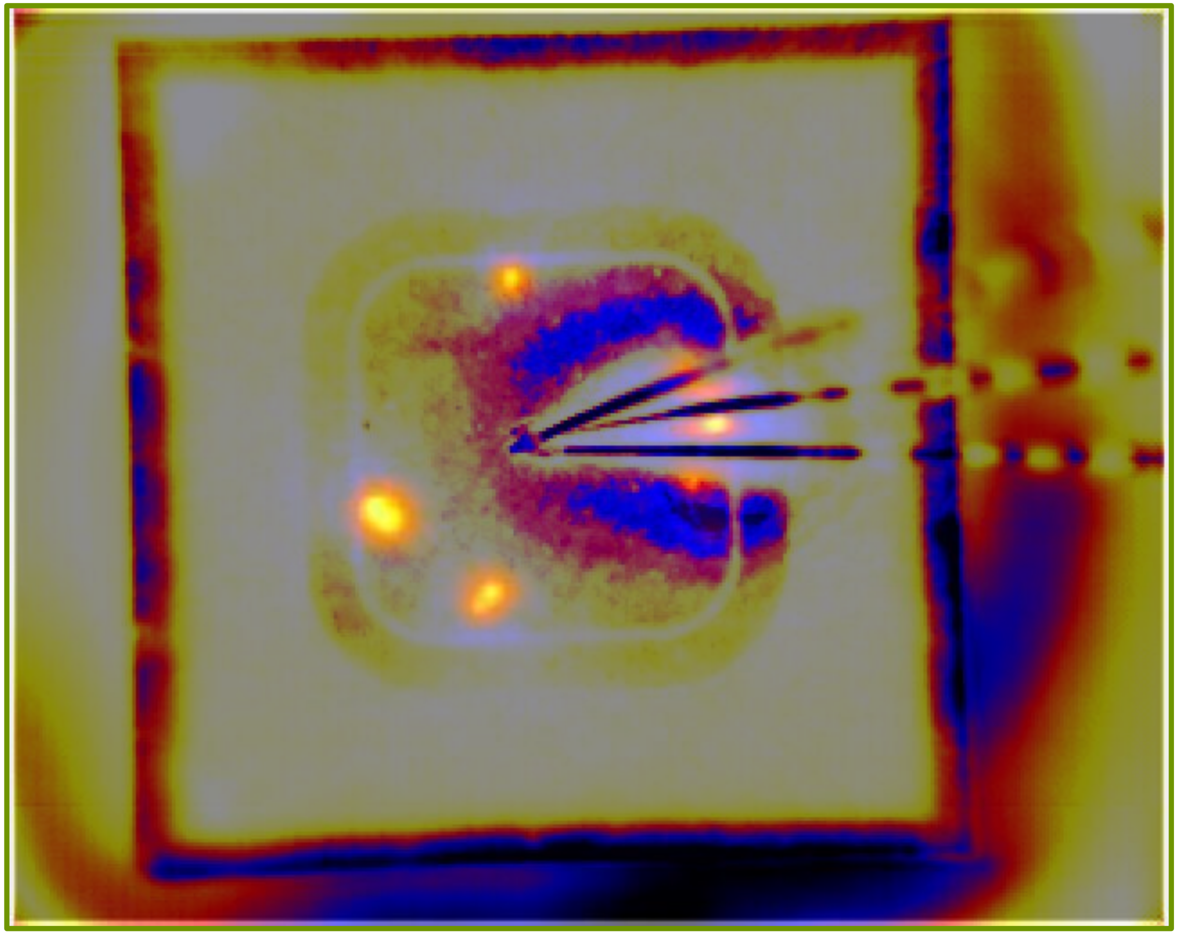
Location of hot spots @ V_{AC} = 20 V



Amplitude image superimposed to average image

LGAD. AIDA2020 v1. Thermographic Measurements

Location of hot spots @ V_{AC} = 150 V

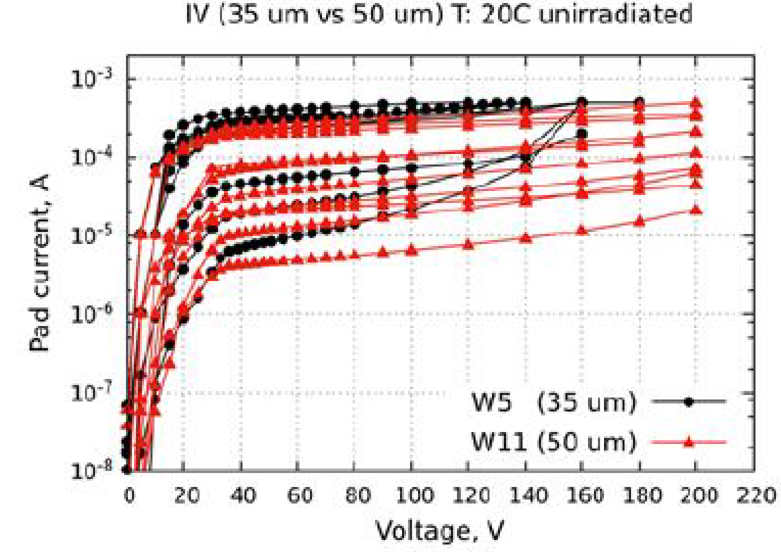


Amplitude image superimposed to average image

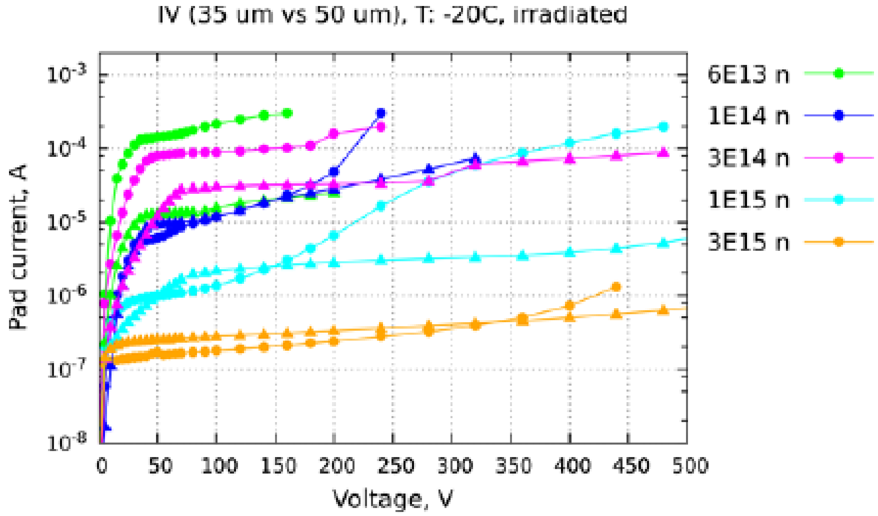
LGAD. AIDA2020 v1. I-V Measurements. Irradiation

- LGAD have high leakage currents (≈mA) but pin diodes are working well (nA)
- Leakage current decreases with irradiation and the detectors can be operated normally (IFCA Santander)
- Originated at LGAD periphery (JTE structure)

Ivan Vila. TREDI 2019. Trento. February 2019



BEFORE IRRADIATION



AFTER IRRADIATION

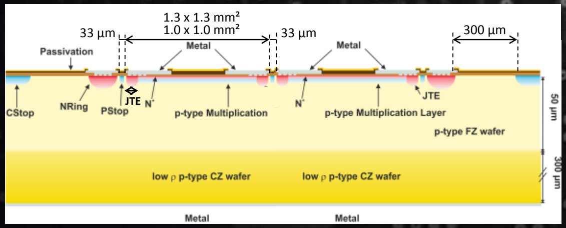
LGAD. AIDA2020 v1. Samples Distribution

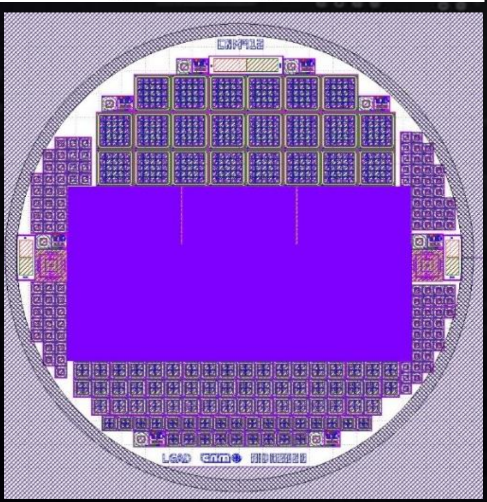
- ATLAS Institutes
  - Wafers Diced: 6.50 % of samples
  - 105 samples/wafer: 630 total
  - Samples distributed by Joern Lange
  - ATLAS 5x5, 2x2 modules (1.3, 1.0)
  - LGAD samples (1.3, 1.0)
  - PiN samples (1.3, 1.0)

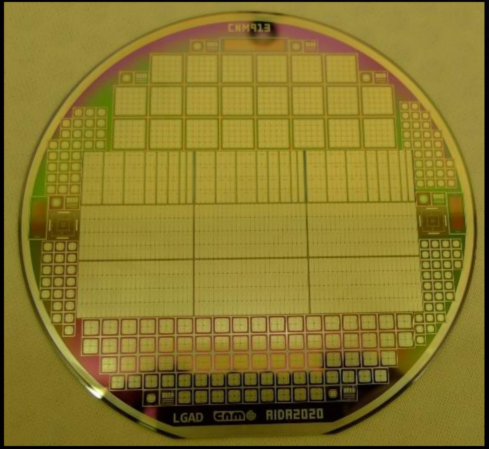
- CMS Institutes
  - Wafers Diced: 6.50 % of samples
  - Samples distributed by IFCA
  - CMS 4x24, 4x4, 4x2, 4x1 modules: 45
  - LGAD samples (1.3, 1.0): 100
  - PiN samples (1.3, 1.0): 31

LGAD. AIDA2020 v2. Run 12916

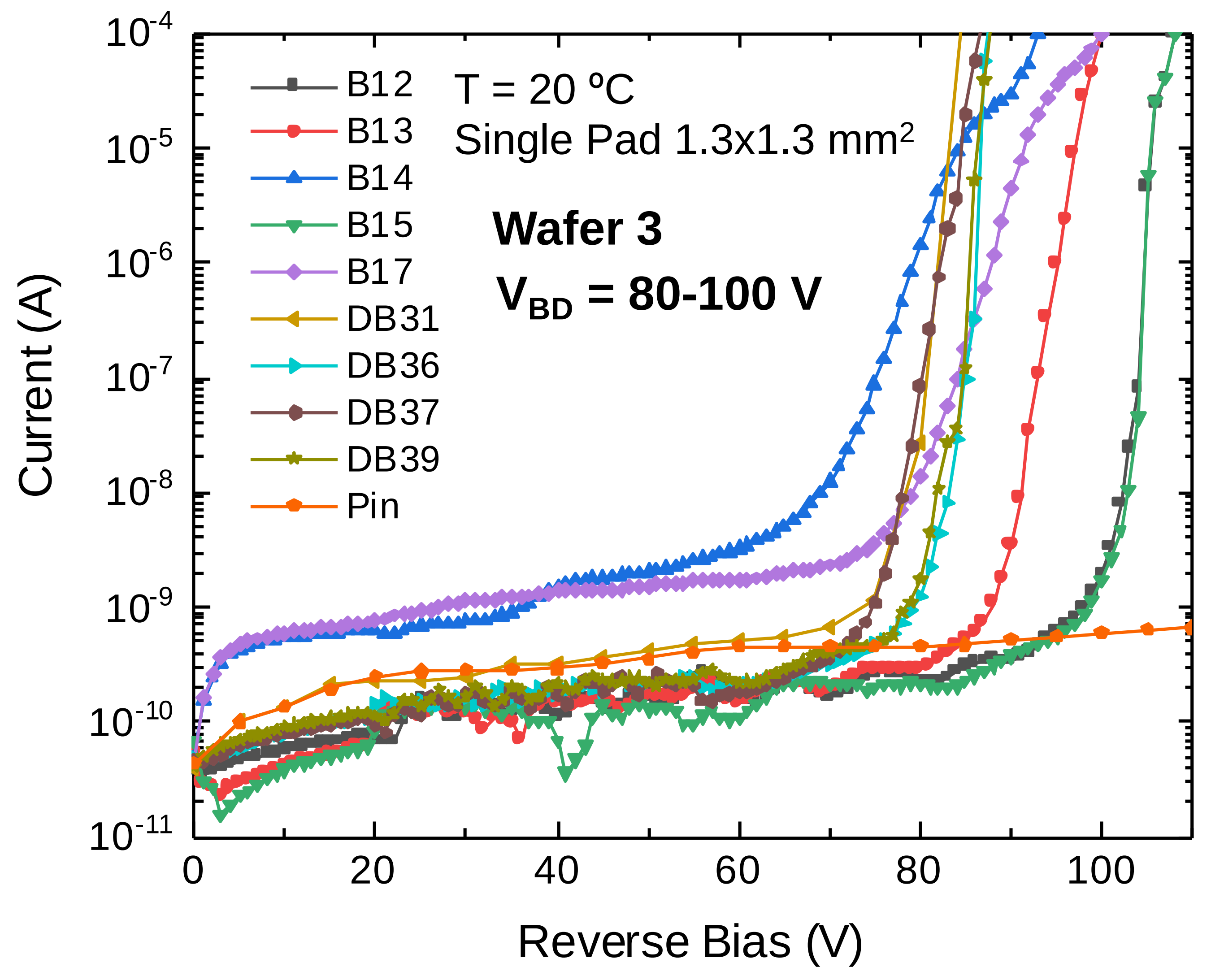
- LGADs for ATLAS & CMS Timing Layers
  - 4 inch, 50+300 µm thick Si-Si. 4 Wafers
  - N⁺-Layer overhang Multiplication Layer until the JTE end
  - We use only one implantation dose and energy value for the multiplication area (medium dose, low energy)
  - We have use temporary metal on all wafers
  - Wafers have been tested on-wafer using some single pad devices to evaluate the fabrication process quality
  - Low Leakage current
  - IV/CV measurements on wafer (preliminary)
  - 5x5 and 2x2 arrays are being measured (preliminary)



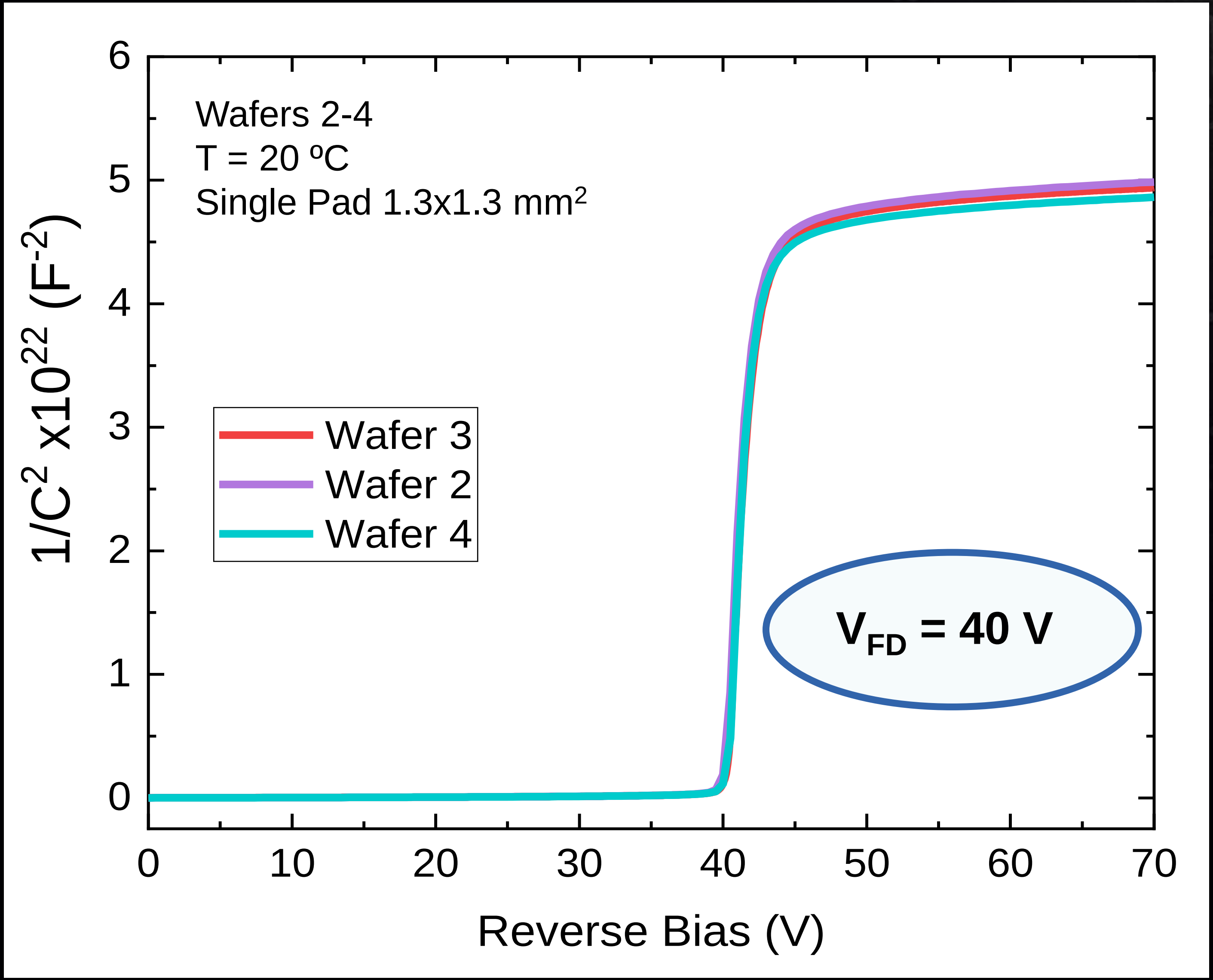




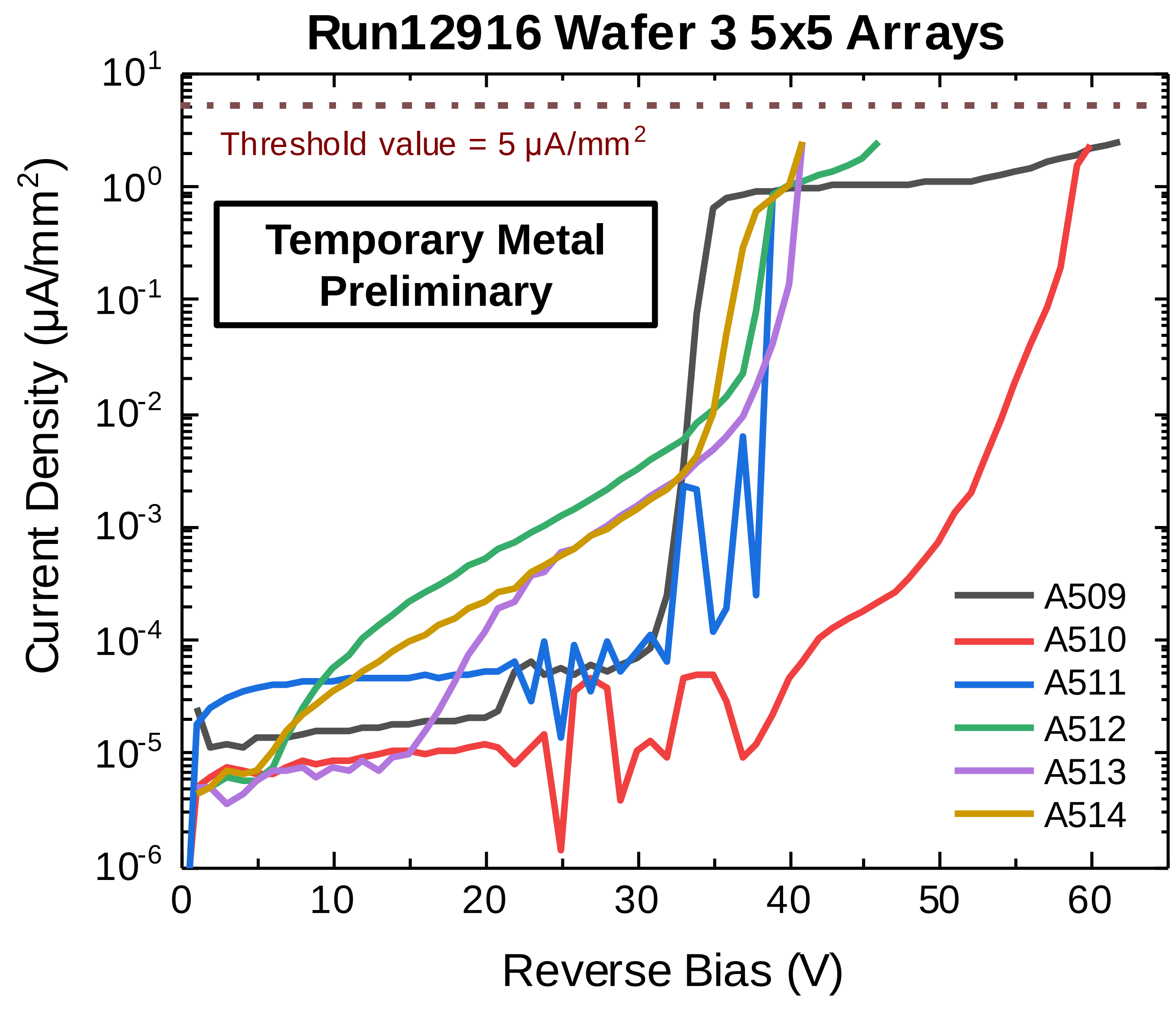
LGAD. AIDA2020 v2. Electrical Characterization



LGAD. AIDA2020 v2. Electrical Characterization

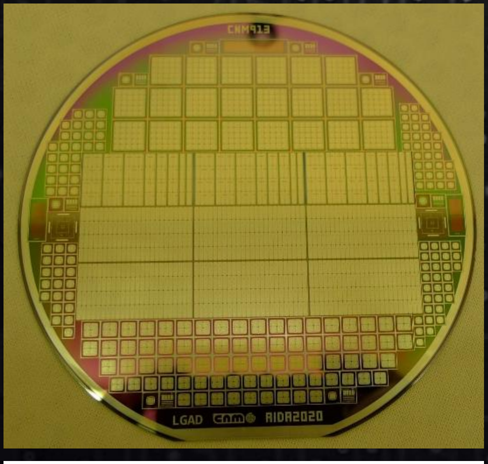


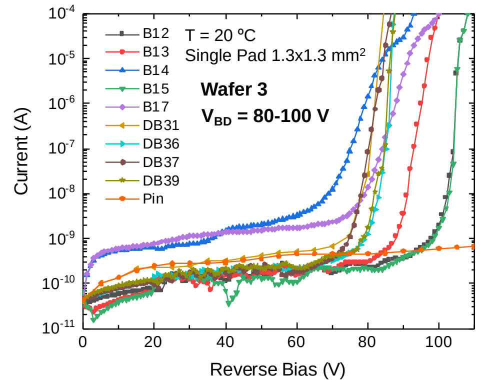
LGAD. AIDA2020 v2. Electrical Characterization

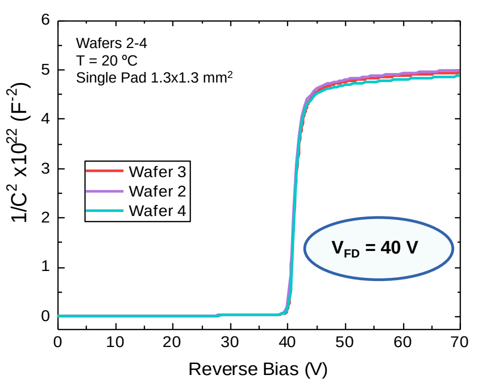


LGAD. AIDA2020 v2. Run 12916

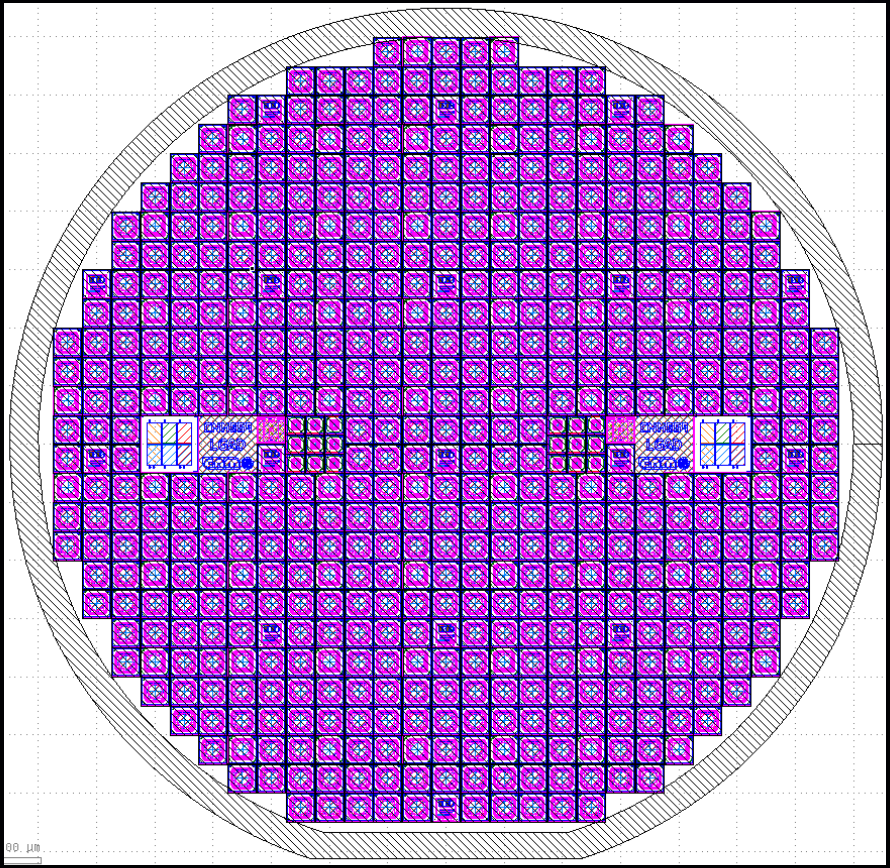
- Conclusions
  - Preliminary measurements in terms of I-V and C-V
  - Leakage current values are the expected (0.1-1 nA)
  - Voltage breakdown and full depletion close to high dose value (change in drive-in process)
  - Gain estimation shows a value around 15
- Future Work
  - Dice the devices and sent them to irradiation campaigns
  - TCT measurements: gain studies
  - Electrical characterization of 2x2 and 5x5 arrays
  - Wafers 2-4 (with Temporary Metal Layer)
    - Modules I(V) and C(V) Characterization
    - Yield

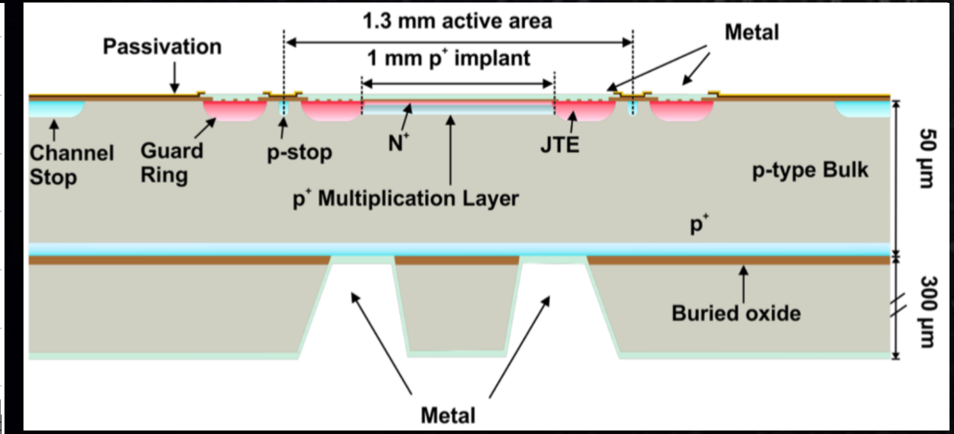


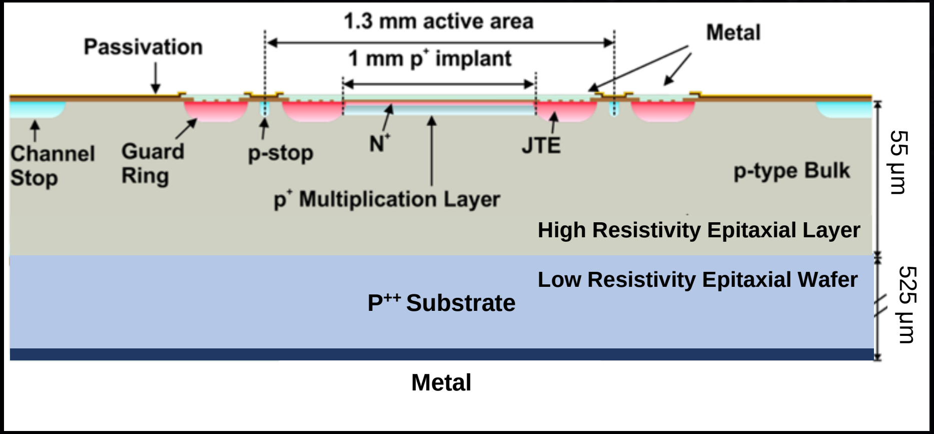




Runs 11486 & 13002. 6 inch Thin LGADs



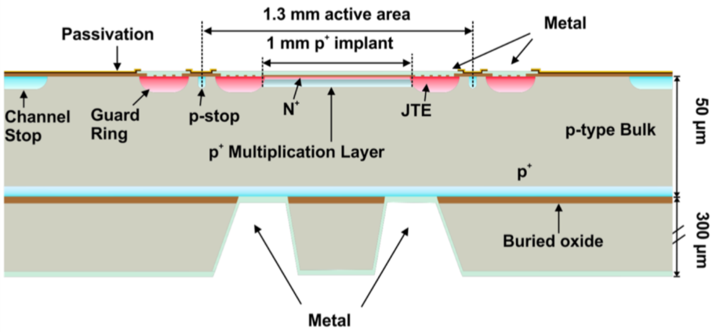




Run 11486. 6” Thin LGAD v1. SOI Wafer. 6LG1

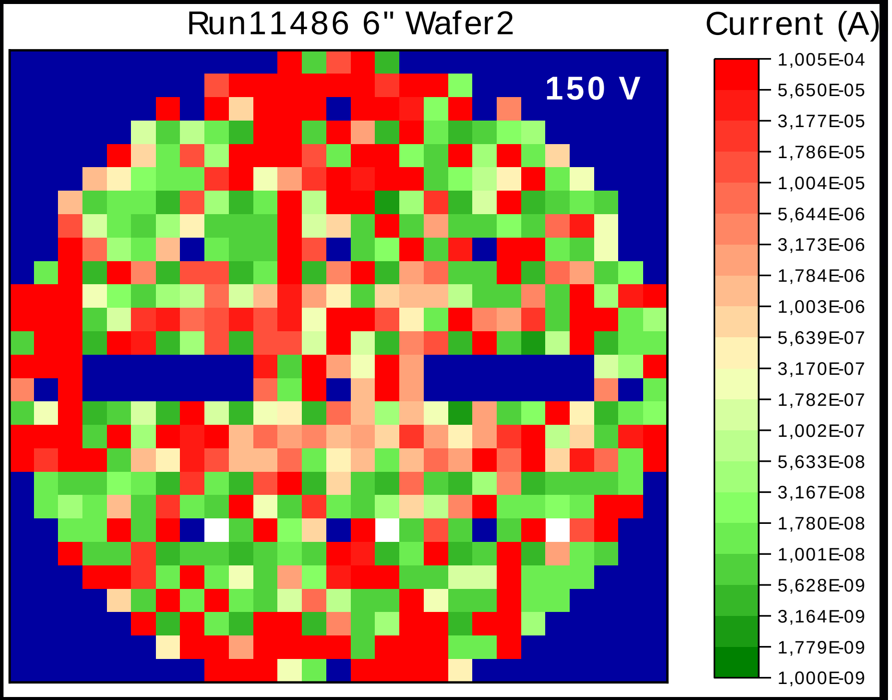
- 1.3x1.3 mm^2 LGAD Pad Devices (Active Area)
- 6 inch, 50+1+300 µm thick SOI wafer
- 7 Wafers: 5 wafers available, 2 wafers broken (W4, W6)
- We use different Implantation Dose and Energy values for the multiplication area
- N$^+$-Layer overhang Multiplication Layer until the JTE end (like AIDA2020 v2 design)
- Wafer mapping: 586 devices

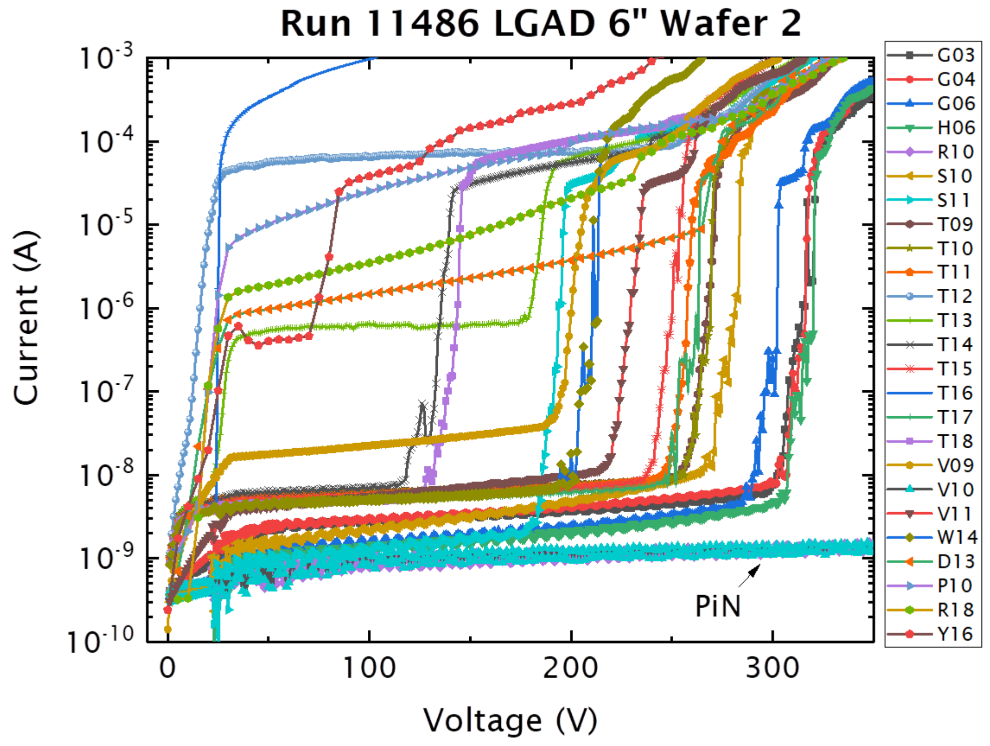
Wafer	Dose (at/cm^2)	Energy (keV)
1	Low	Low
2	Med	Low
3	High	Low
4	Med	Med
5	High	Med
6	Low	High
7	Med	High



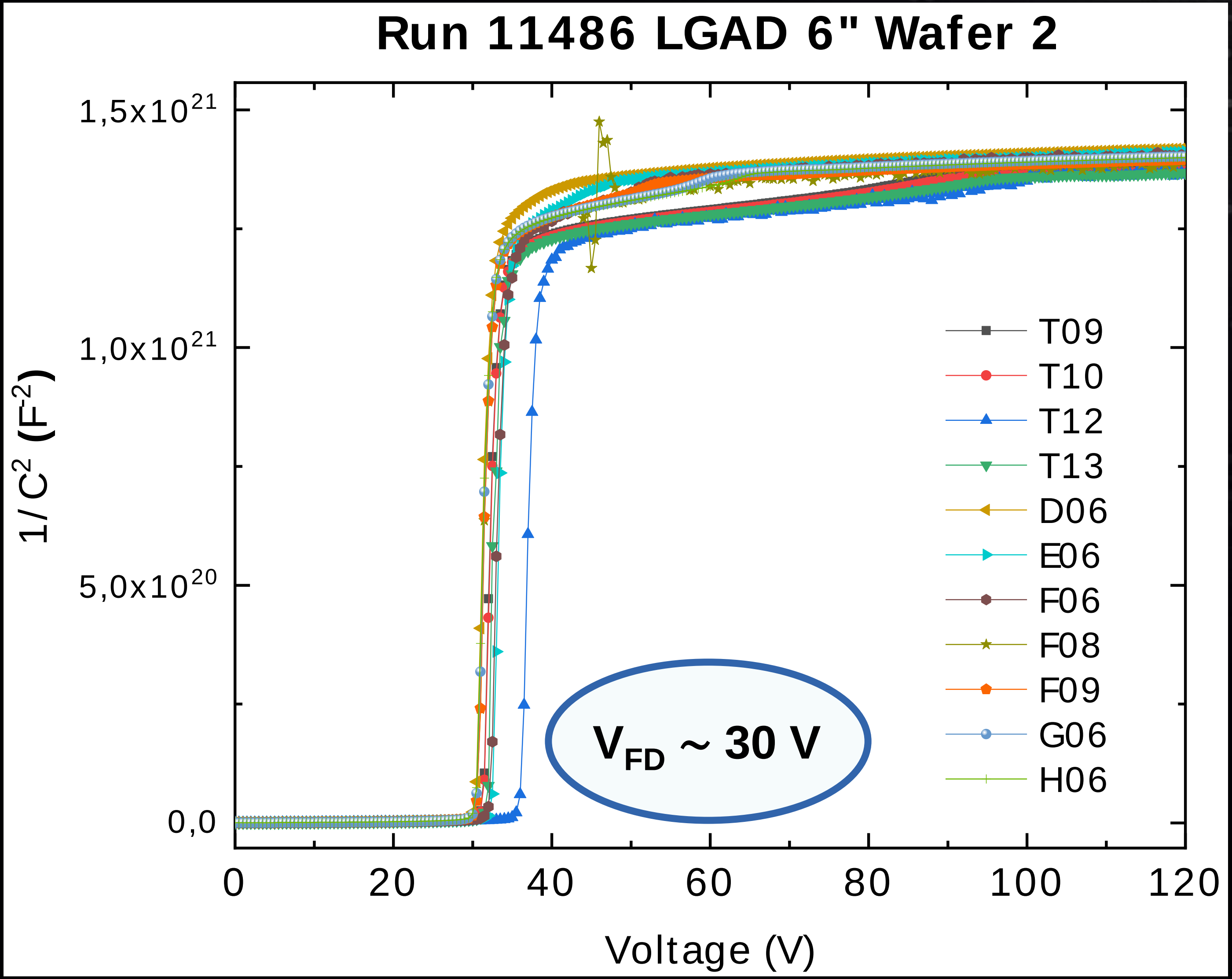
Run 11486. 6” Thin LGAD v1. SOI Wafer. 6LG1

- I-V on Wafer 2 (Med Dose - Low Energy)





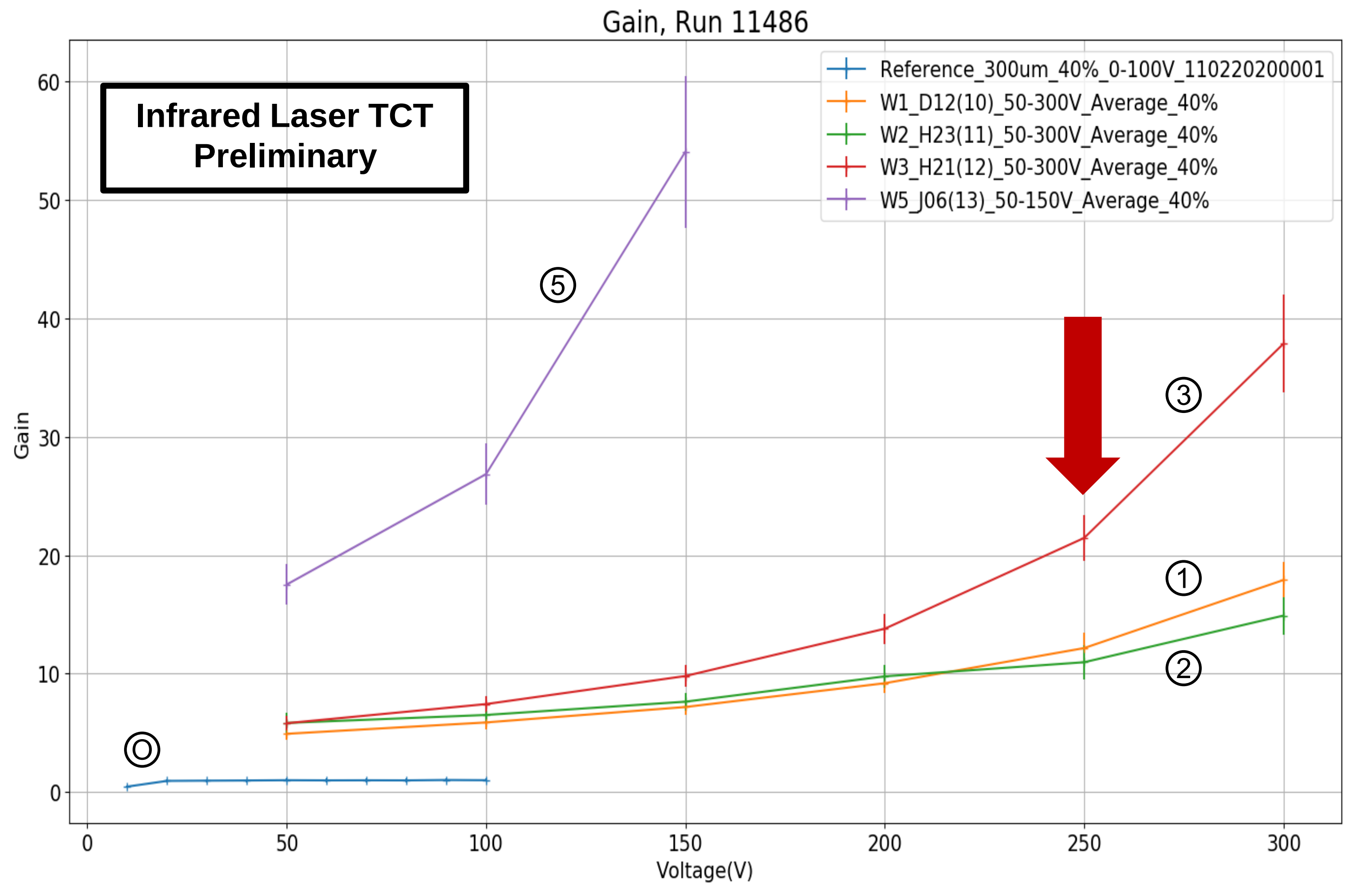
Run 11486. 6” Thin LGAD v1. SOI Wafer. 6LG1



V_{FD} ~ 30 V

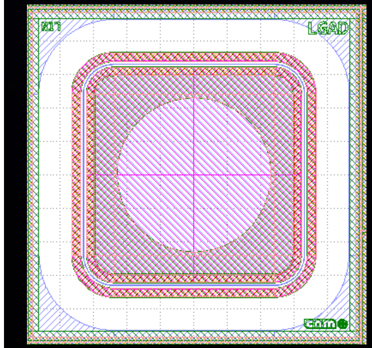
Run 11486. 6” Thin LGAD v1. SOI Wafer. 6LG1

- Infra Red Laser TCT. Wafer 3. Gain: 10 @ 150V, 20 @ 250V



Wafer	Dose (at/cm^2)	Energy (keV)
1	Low	Low
2	Med	Low
3	High	Low
4	Med	Med
5	High	Med
6	Low	High
7	Med	High

Pad diodes



Run 11486. 6” Thin LGAD v1. SOI Wafer. 6LG1

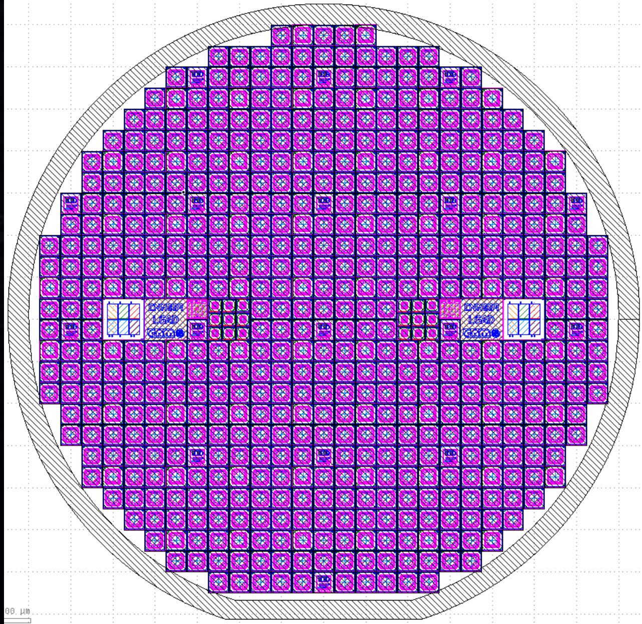
- Some devices have been already sent to irradiation campaigns

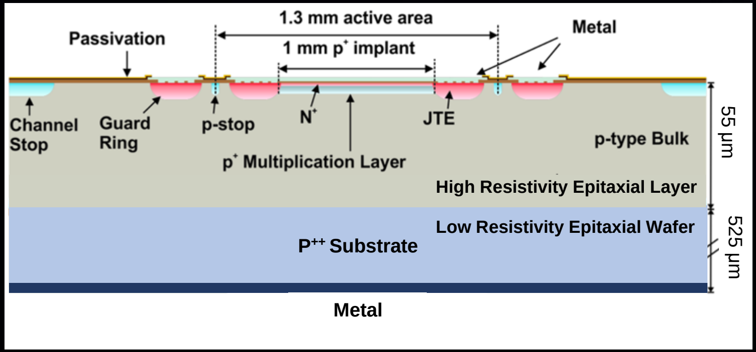
Institution / Research Centre	Wafer
IFAE (Barcelona)	2,3
CERN (Geneva)	2,3
SCIPP (Santa Cruz)	3
STFC RAL (Oxford)	3
IFCA (Santander) + CNA (Sevilla)	2,3,5

- CERN preliminary measurements (M. Moll group) shows that samples from this run do not show “Pop Corn” issue

Run 13002. 6” Thin LGAD v2. EPI Wafer. 6LG2

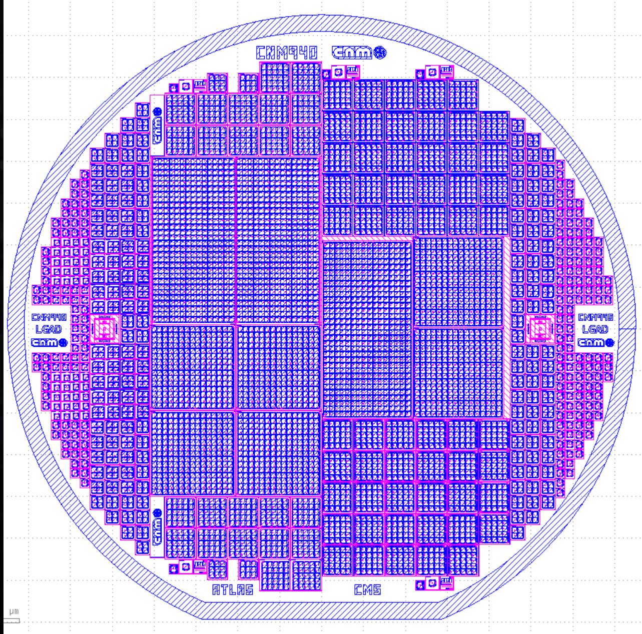
- Same mask set as Run 11486 (6LG1)
- 1.3x1.3 mm^2 LGAD Pad Devices (Active Area)
- 6 inch, 55+525 µm thick EPI wafer
- 4 Wafers. Same 6LG1 Technological Process
- We use three implantation dose and one energy value for the multiplication area (med, med/high, high)
- N$^+$-Layer overhang Multiplication Layer until the JTE end (like AIDA2020 v2 design)
- Wafer mapping: 586 devices
- Run in Process (44/88 steps)





6” Thin LGAD v3. ATLAS/CMS Run. 6LG3

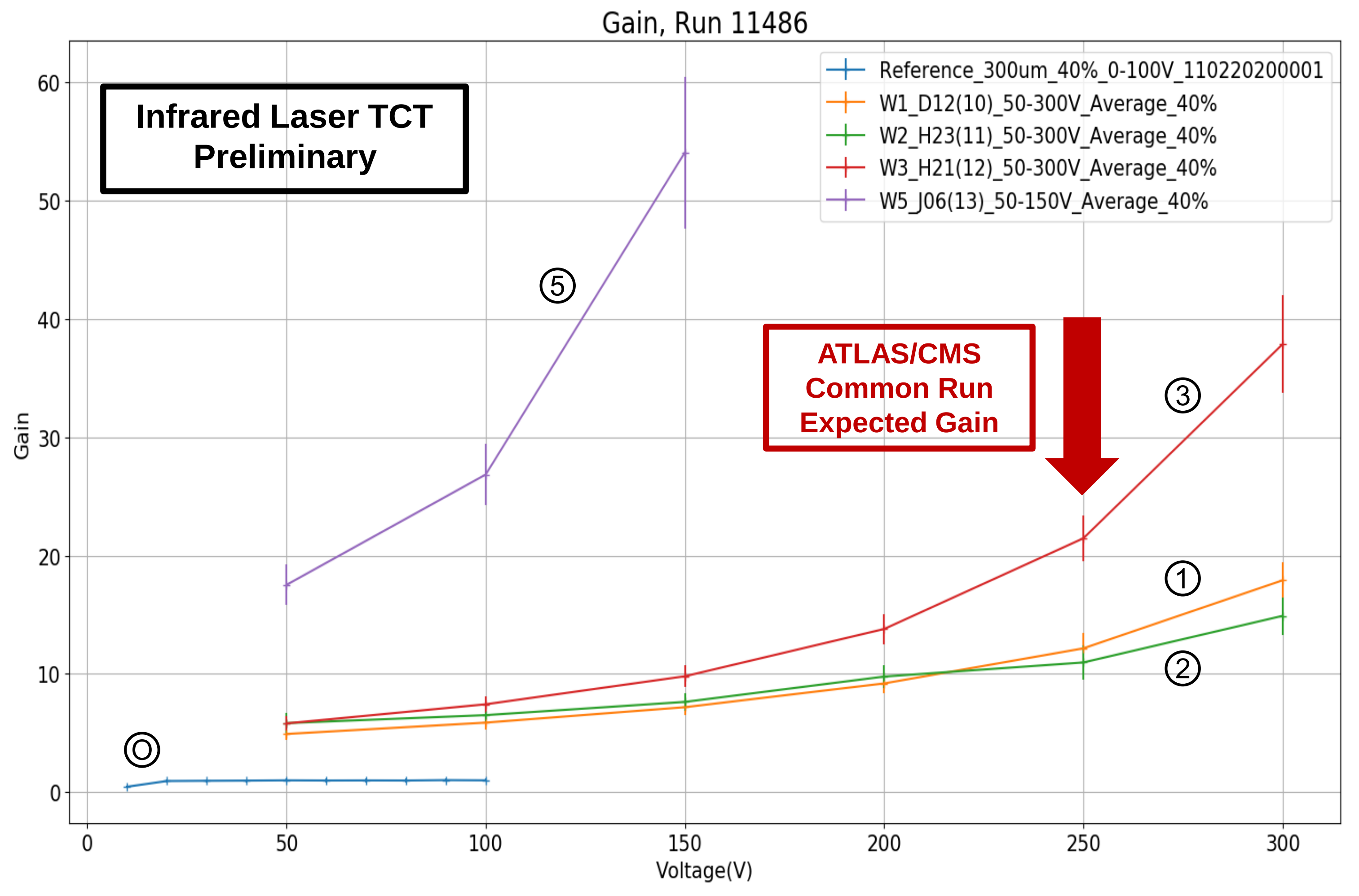
- New run using 6”, 50+(1)+300 µm thick, SOI and Epi-Wafers
- Layout proposed by ATLAS-HGTD and CMS-ETL
- Timing detectors with Pad and Array designs
- Change standard Slim Edge to 500 µm (called SE5)
- 3 Inter-Pad Gaps: 37, 47, 57 µm (corresponding to JTE 5, 10, 15 µm), called IP37, IP47, IP57
- Same positions of large probe pads for common probe card between HPK+CNM
- 35-50 µm thick Si-Si wafers were purchased in January 2018 but the wafers haven't arrived by now (IceMosTech)
    - Expected delivery: Second quarter of 2020
- Work in progress. End of the fabrication process expected by the end of 2020?



- ✓ **1x** CMS_1.3x1.3_16x32_IP57
- ✓ **2x** CMS_1.3x1.3_16x16_IP57
- ✓ **28x** CMS_1.3x1.3_5x5xN_IP57
- ✓ **15x** CMS_1.3x1.3_5x5_IP57
- ✓ **9x** CMS_1.3x1.3_5x5_IP47
- ✓ **3x** CMS_1.3x1.3_5x5_IP37
- ✓ **1x** PiN_1.3x1.3_5x5_IP57/47/37
- ✓ **32x** CMS_1.3x1.3_2x2_IP57/47
- ✓ **5x** PiN_1.3x1.3_2x2_IP57/47
- ✓ **48x** CMS_1.3x1.3_1x1_IP57/IP47
- ✓ **16x** PiN_1.3x1.3_1x1_IP57/47

6” Thin LGAD v3. ATLAS/CMS Run. 6LG3

- Expected Gain: 10 @ 150 V, 20 @ 250 V (6LG1, Wafer 3)

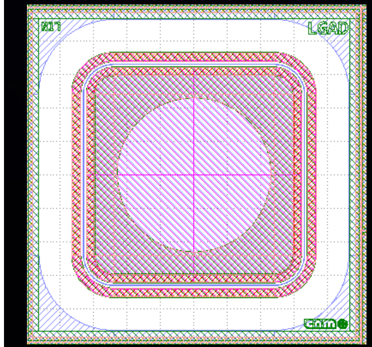


Infrared Laser TCT Preliminary

ATLAS/CMS Common Run Expected Gain

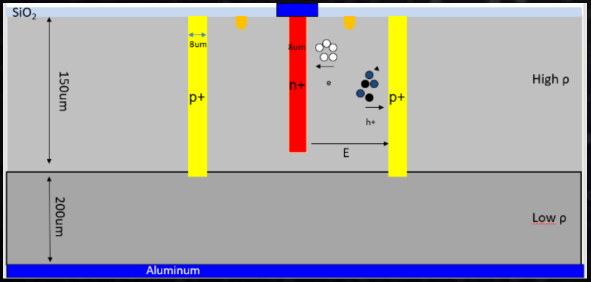
Wafer	Dose (at/cm^2)	Energy (keV)
1	Low	Low
2	Med	Low
3	High	Low
4	Med	Med
5	High	Med
6	Low	High
7	Med	High

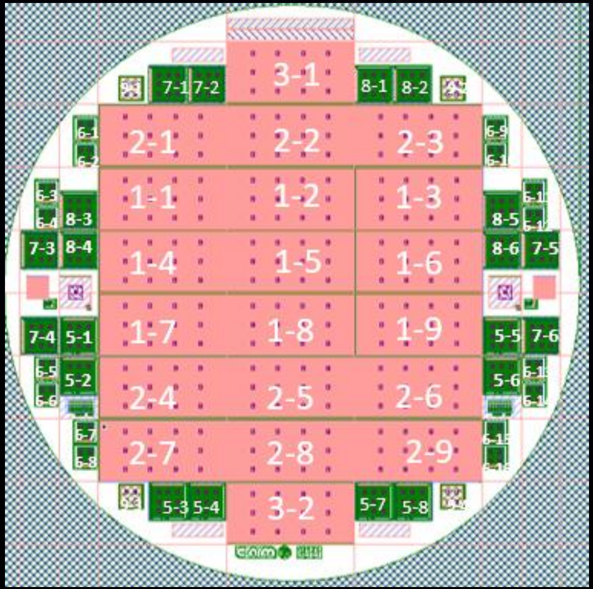
Pad diodes



3D-SS. AIDA2020. RD53A. Run 11119

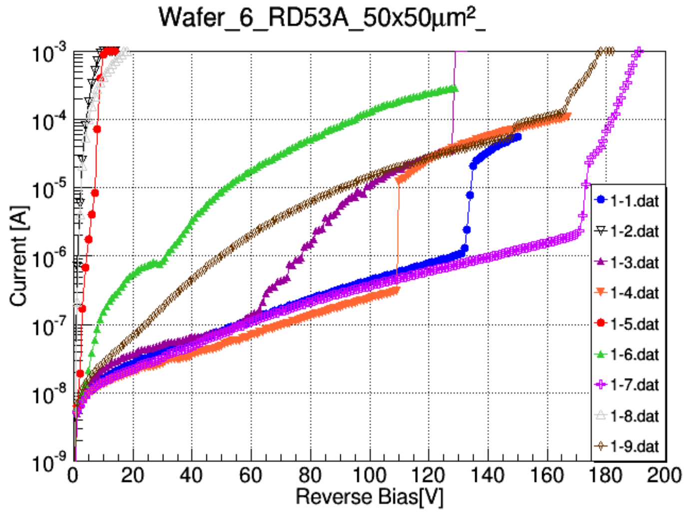
- Single Side process on Si-Si wafers (8)
  - 150 µm active thickness, 200 µm handle wafer, 120 µm n-column depth, 8 µm column diameter
  - Mask: CNM899
  - 9 RD53A 50x50 µm² (1-x)
  - 2 RD53A 25x100 µm² 1E (3-x)
  - 9 RD53A 25x100 µm² 2E (2-x)
- Diodes
  - 5-x 50x50 µm², 100x100 electrodes
  - 6-x 50x50 µm², 50x50 electrodes
  - 7-x 25x50 µm², 50x50 electrodes
  - 8-x 25x100 µm², 50x50 electrodes
  - 64 Test structures 3x3 matrix
- MOS
  - 9-x 3500x3500 µm²
  - Polysilicon Test structures

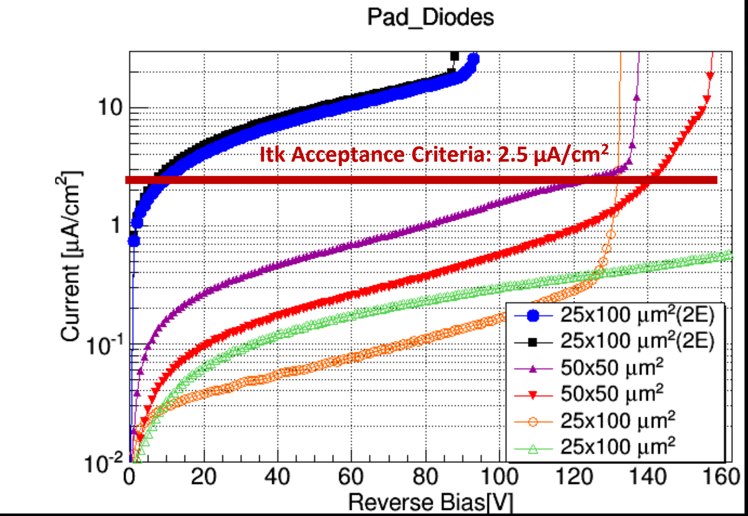


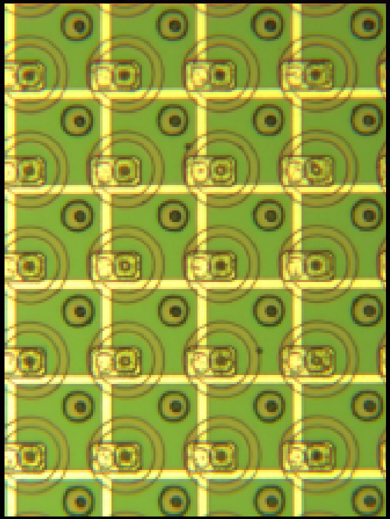


3D-SS. AIDA2020. RD53A. Run 11119

- I-V Measurements with temporary metal
  - Good yield for 50x50 µm^2 pixel sensors (~70%)
    - Breakdown takes place at high value voltages
  - Leakage current is below the ITk acceptance criteria
    - 2.5 µA/cm^2 for 50x50 µm^2 and 25x100 µm^2 (1E)
  - 25x100 µm^2 (2E) geometry has instead low yield
    - Small distance between p-columns and metal pad







3D-SS. AIDA2020. Run 11119. Distribution

- AIDA2020-ATLAS
  - Wafers 6, 8: Dicing, UBM at IZM; Flip-Chip at IFAE
  - ATLAS bump-bonding market survey requirements
- AIDA2020-CMS
  - Wafers 3, 5, 7: Dicing, UBM and Flip-Chip at IZM
  - Wafers 1, 2, 4 will be sent to the rest of CMS bump-bonding market survey candidates (one wafer for each candidate)

Thank you for your attention!

AIDA2020 Project
Wp7 IMB-CNM Activities

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