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MICRO-CHANNEL COOLING FOR COLLIDER EXPERIMENTS: REVIEW AND RECOMMENDATIONS

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Authors:	A. Mapelli, P. Petagna, M. Vos,

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In this paper, we discuss the potential of micro-channel cooling for high-energy-physics experiments. We discuss the experience gained in the production and operation of the micro-channel cooling systems in running experiments and experiments in construction. We also review the R&D programme towards future applications, with emphasis on the development of integrated micro-channel cooling solutions supported by the AIDA2020 project. The paper also discusses important steps that are needed to deploy micro-channel cooling more broadly in high-energy physics: a precise model of the cooling performance of bi-phase coolants in narrow channels, standardized connector solutions, and detailed studies into the thermo-mechanical requirements for the silicon detectors at future colliders.

Micro-channel cooling for collider experiments: review and recommendations

Editors: A. Mapelli[1], P. Petagna[1], M. Vos[2],
Members of AIDA2020-WP9 and external contributors:
D. Alvarez Feito[1], L. Andricek[3], M. Angeletti[1,4], M. Bomben[5], M. Boscardin[6], F. Bosi[7], G. Calderini[5], R. Callegari[1], P. Coe[8], J. Degrange[1], T. Frei[1,4,9], I. García[2], D. Hellenschmidt[1,10], A. Koutoulaki[11], C. Lipp[1,2], C. Marinas[2,10], R. Meunier[1], J. Noel[1], P. Renaud[1,4], M. Ullan[12], G. Vidal[2], G. Viehhauser[8], and M.A. Villarejo[2]

[1] *CERN, Switzerland*
[2] *IFIC (UVEG/CSIC) Valencia, Spain*
[3] *HLL-MPG, Munich, Germany*
[4] *EPFL, Lausanne, Switzerland*
[5] *LPNHE, Paris, France*
[6] *FBK, Trento, Italy*
[7] *INFN Pisa, Italy*
[8] *University of Oxford, United Kingdom*
[9] *CSEM, Neuchatel, Switzerland*
[10] *University of Bonn, Germany*
[11] *Universiteit Twente, The Netherlands*
[12] *CNM-IMB, Barcelona, Spain*

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Contents

1 **Introduction** **3**

2 **Performance of Micro Channel Cooling** **5**

3 **Fabrication of silicon microchannel plates** **8**
3.1 Wafer Bonding Approaches 9
3.2 Embedding Approach or Buried Channels Technology 10

4 **Accessible production facilities** **11**

5 **Pressure resistance of silicon structures** **14**

6 **Connectors** **17**
6.1 Commercially-available connectors 17
6.2 Soldered connectors 17
6.3 In-plane low mass connections 19

7 **Silicon micro-channel cooling plate fabrication** **21**

8 **Design tools and simulation** **23**

9 **The CERN micro-channel cooling test stand** **26**

10 **Measurements of CO_2 boiling in micro-channels** **30**

11 **Integrated micro-channels in sensitive Silicon ladders** **33**

12 **Integrated cooling channels in CMOS devices** **35**

13 **Future applications in high-energy physics** **37**

14 **Summary** **39**

1 Introduction

Position-sensitive silicon detectors form the heart of all modern-day collider experiments. Due to the increasing channel density, the high radiation environment at hadron colliders, and the strict requirements on the material budget, the cooling of these detectors represents an important challenge. To achieve the scientific goals of the next generation of experiments, it is vital that the cooling system is considered as an integral part of the detector design (1).

The micro-channel heat sink was first proposed in the early 1980s (2). The introduction of narrow cooling channels in high-power devices ensures an excellent heat-transfer coefficient between the substrate and the coolant, and thus a minimal thermal resistance. Today, micro-channel cooling plays an important role in the thermal management of electronics (microchip cooling, microreactors) and energy systems (fuel cells, microcombustion).

In high energy physics, micro-channel cooling offers a very competitive alternative to traditional cooling systems based on metal piping (3). The very short path between the heat load and heat sink offers superb thermal performance. The use of thin silicon plates reduces the contribution of the cooling system to the material budget. Finally, the use of silicon as a structural material avoids the mismatch of the thermal expansion coefficients that threatens the stability and integrity of the detector.

The use of micro-channel cooling was pioneered in high-energy physics by the NA62 experiment, with the installation of the GigaTracker in 2014. Evaporative CO_2 cooling in micro-channel cooling plates is foreseen for the upgraded LHCb Vertex Locator, that is to be installed in the experiment during LS2. Today, several groups involved in the ATLAS, ALICE, Belle II and linear e^+e^- collider projects are active in the development of micro-channel cooling solutions for silicon detectors. The development of micro-channel cooling is supported by work package 9 of the AIDA2020 project[1]

This paper is one of the deliverables of the AIDA2020 project. It reviews the R&D effort within the HEP community. We also present a detailed characterization of the cooling performance and compare it to state-of-the-art simulation tools. And finally, it presents directions for R&D towards more advanced micro-channel cooling solutions and future applications. We hope that this review may help others to orient their effort.

The first part of this paper presents the experience gained in R&D, prototyping and production of the first micro-channel cooling structures, in the hope that the lessons learned may be of use to the community. In section 2 the cooling performance of a system based on micro-channels is compared to that of classical solutions. The techniques to produce silicon cooling plates are briefly reviewed in section 3. The production facilities accessible to high energy physics are discussed in section 4, section 5 reports a series of measurements to establish the resistance to high pressure of different channel geometries and production

[1]The AIDA2020 project, funded under the H2020 framework programme with grant agreement number , initially ran from 2014 to 2019, and has been extended until April 2020.

schemes, section 6 lists the commercial and custom connectors used in HEP. Finally, section 7 summarizes the lessons learned during the production and operation of the cooling plates for the NA62 GigaTracker and the production of the prototypes for the LHCb VELO upgrade.

The second part of the paper presents a view on future challenges and opportunities to the deployment of micro-channel cooling in future high-energy physics experiments. To successfully design and fabricate the next generation of structures, a detailed understanding of the cooling performance of micro-channel cooling circuits is crucial. This challenge is addressed in the next three sections: section 8 presents the simulation tools used to predict the performance, section 9 describes a setup for the characterization of prototypes and section 10 compares an extensive set of measurements on bi-phase CO_2 cooling in a variety of channel dimensions to the results of the simulation.

An outlook to future developments and applications is given in section 11 through section 13. The ultimate cooling performance is obtained by integrating the cooling circuit inside the silicon sensor itself. Two sections present possible paths to realize such integrated cooling channels: section 11 describes a wafer bonding process that allows for the integration of the cooling circuit in classical silicon detectors, while section 12 demonstrates the integration of cooling channels in a working CMOS sensor. section 13 discusses the role of micro-channel cooling in future collider experiments.

To conclude, section 14 summarizes the most important findings of this paper.

2 Performance of Micro Channel Cooling

The benefits of minimizing the size of a heat exchanger by using small hydraulic diameter tubes or channels have been confirmed multiple times in the literature for various geometries, refrigerants, and applications; see e.g. (2; 4; 5). This approach provides a higher surface area to volume ratio compared to large-diameter macro-channels and results in higher heat transfer rates and smaller equipment size. Furthermore, a thin micro-channel cold plate allows for the minimization of the thermal path between the heat source and the heat sink, thus greatly reducing the thermal resistance of the assembly. The above statements are particularly valid when applied to the thermal management of pixel detectors by micro-structured silicon cooling devices. As a matter of fact, the design of an optimized on-board cooling for pixel detectors requires the maximization of the cooling efficiency. This implies minimizing two quantities:

- The amount of material crossed by the particles (i.e. the contribution to the "material budget");
- The temperature difference between heat source and heat sink for a given heat load (i.e. a practical "Thermal Figure of Merit").

The material of the detector is expressed in terms "radiation lengths" (X_0): the mean distance over which the energy of a high-energy electron is reduced to 1/e by the interaction with the material layer, 7/9 of the mean free path for pair production by an energetic photon and the relevant length scale that determines the amount of multiple Coulomb scattering. The radiation length (in g/cm^2 for materials with atomic number $Z > 4$ is approximately given by (6):

$$\frac{1}{X_0} = \frac{1}{716.408A} Z^2[\log 184.15Z^{-1/3} - f(Z)] + Z \log 1194Z^{-2/3}, \qquad (1)$$

with $f(Z) = a^2[(1 + a^2)^{-1} + 0.20206 - 0.0369a^2 + 0.0083a^4 - 0.002a^6]$, $a = \alpha Z$ and A the atomic mass of ther material in g/mol.

Crystalline silicon has a radiation length of 9.4 cm, to be compared with 1.7 cm for stainless steel and 3.6 cm for titanium, the two materials typically used for ultra-thin wall cooling pipes in pixel detectors. The term "material budget" indicates the ratio x/X_0 between the thickness of a certain material crossed by a particle in a detector and the radiation length of that material. Therefore, for the same wall thickness, the impact on the detector material budget of a silicon channel is 5.5 times smaller than the one of a stainless steel pipe and 2.6 times smaller than the one of a titanium pipe.

The Thermal Figure of Merit ($TFoM$) can be operatively defined as the temperature difference ΔT between the cooling fluid and the sensor, divided by the detector surface power density. The $TFoM$ parameter hence has dimensions $[K \cdot cm^2/W]$, i.e. those typical of a thermal insulance. In particular, when defined this way, the parameter gets the same formulation of the "R-value", a parameter widely used in civil engineering: the temperature difference per unit of heat flux needed to sustain one unit of heat flux between the warmer surface

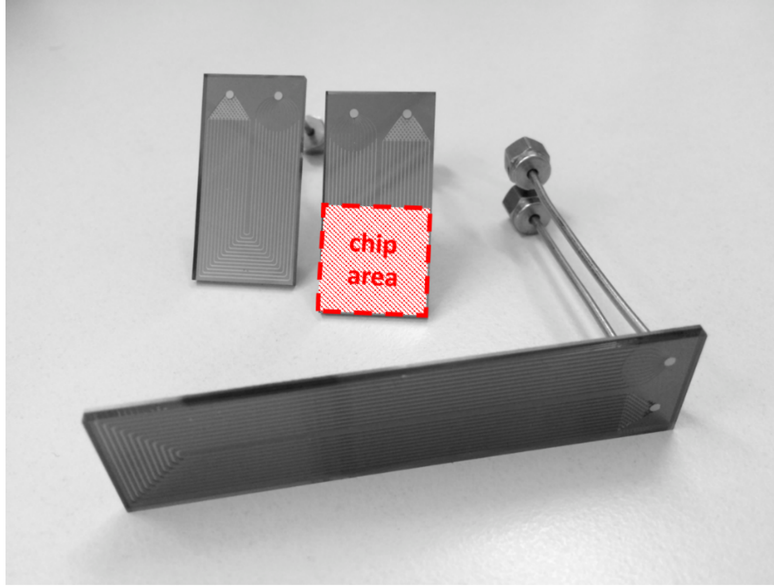

Figure 1: Examples of microstructured silicon cold plates optimized for CO_2 boiling flows. Design by CERN and LPNHE. Production by FBK.

and colder surface of a barrier under steady-state conditions. Therefore, when comparing different configurations for the thermal management of a detector, the one presenting the smallest thermal figure of merit is the one ensuring the highest global cooling efficiency.

Silicon micro-channel cold plates are natural candidates for the minimization of the $TFoM$ for a number of reasons:

- The very high heat transfer coefficient of fluids in micro-channels
- The very large surface available for heat exchange between the heat source and the heat sink
- The high thermal conductivity of crystalline silicon (7), ranging between 150 W/mK and 200 W/mK in the temperature range of interest
- The coincidence of Coefficient of Thermal Expansion of the heat sink and the heat source, suppressing the need for any complex compliant thermal interface between the two, thus minimizing the chain of interposed thermal resistances

Detailed measurements of the thermal figure of merit that can be achieved in bi-phase cooling in silicon micro-channels can be found in Ref. (8). A micro-structured silicon cold plate with 13 parallel channels with a cross section of 200 $\times$ 120 μm, as shown in Figure 1, designed by CERN and LPNHE and produced at FBK, was coupled by a simple Araldite layer with a 2$\times$2 cm^2, 100 μm thick

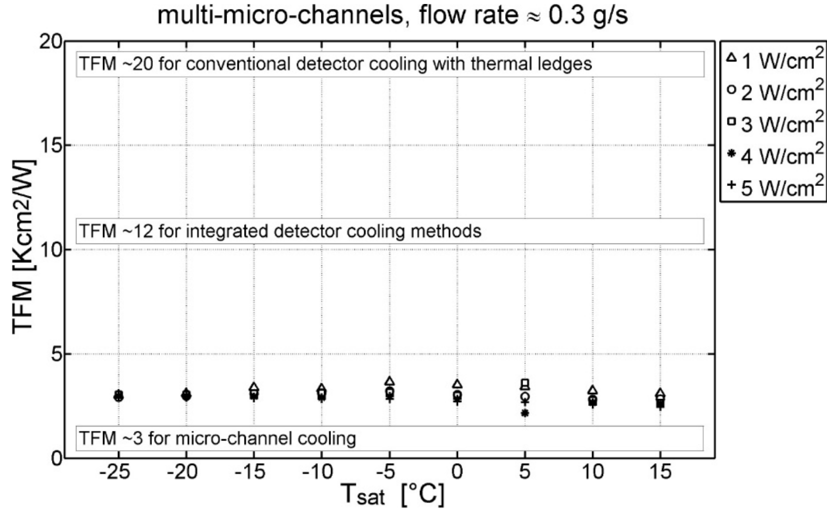

Figure 2: Measurements of the thermal figure of merit for bi-phase CO_2 cooling at a constant flow rate of 0.3 g/s and various saturation temperatures in test structures with micro-channels with a cross-section of 120 × 200 μm^2.

silicon heater, simulating a pixel module. The silicon cold plate was sealed by anodic bonding with a borofloat glass in order to permit high speed flow imaging, Saturated Carbon Dioxide at saturation temperatures from +15° C to 25° C was circulated in the micro-channel device at mass flow rates of 0.3 and 0.1 g/s (corresponding to a mass flux of 1000 and 300 $kg/m^2 \cdot s$, respectively) while the silicon heater was powered with surface power densities from 1 to 5 W/cm^2. The saturation temperature of the CO_2 was directly measured by immersion PT100 sensors before and after the micro-channel device, while the temperature on the hottest spot of the silicon heater (identified previously by a Finite Element simulation) was measured by a point K-type thermo-couple. All tests were executed under vacuum in order to ensure perfectly adiabatic boundary conditions. The measured $TFoM$ was found to be constant for the whole test range of the multi-micro-channels and always of the order of $\sim 3K \cdot cm^2/W$. An example is shown in Figure 2 (extracted from (8)).

The results obtained with micro-channel cooling can be compared to more traditional detector cooling techniques. Conventional detector cooling with thermal ledges coupled to metal pipes exhibits typically a $TFoM$ of $\sim 20K \cdot cm^2/W$, while highly optimized pipe-structure integrated designs may reach a minimum $TFoM$ of $\sim$ $12K \cdot cm^2/W$ (3). This implies that micro-channel cooling systems offer a cooling performance four to six times better than the one delivered by all the designs presently in use for the thermal management of modern pixel detectors. Integrated micro-channel circuits, where the coolant is introduced directly in the silicon sensor, can achieve an even more direct contact between heat source and heat sink, as discussed in section 11 and section 12.

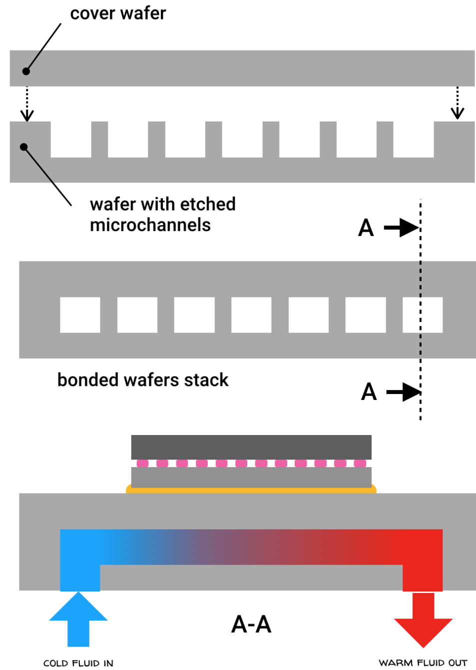

Figure 3: A cooling plate consists of a silicon wafer with etched trenches bonded to another wafer to close them. It is attached to a detector for its thermal management via a coolant circulating in the microchannels.

3 Fabrication of silicon microchannel plates

Recent developments in microfabrication techniques at CERN have defined a novel strategy for the construction and thermal management of pixel detectors. It is based on innovative silicon substrates with embedded microchannels distributing the coolant over the whole surface of the detector. These "microchannel cooling plates" are also the backbone of the mechanical integration of pixel detectors modules. A microchannel cooling plate is simply a substrate with small parallel channels inside separated by fins (see figure 3). Typically these channels have hydraulic diameters below the mm and are etched in silicon. The channels can be integrated into an active chip (direct cooling) or manufactured on a stand-alone plate to be attached to a device (indirect cooling).

Microchannels can be fabricated in silicon following two main approaches, that are described below.

3.1 Wafer Bonding Approaches

The most frequently used approach consists in etching the microchannels in one wafer and closing them by bonding another wafer on top. This technique is used at CERN to manufacture the cooling plates for the NA62 GTK and for the LHCb VELO LS2 Upgrade (9) and forms the basis of most R&D efforts, including the integrated channels of section 11.

Wafer bonding techniques can be classified into the following two categories (10):

- direct bonding (*e.g.* fusion bonding, anodic bonding),
- bonding with intermediate layers (*e.g.* glasses, metals, adhesives).

In all cases, and in particular for silicon direct bonding, the requirements on flatness, smoothness and cleanliness of the surfaces to be mated are stringent. They must be free of contaminants which can be classified as (a) particle contamination (like dust, hair, fibres), (b) organic contamination (hydrocarbons from the air, plasticisers from wafer boxes) and (c) ionic contamination (metal ions from metal tweezers or glass containers) (11). Of all contaminants, particles at the interface pose the biggest structural problem. A particle with a diameter of 1 μm at the interface between two 4" wafers can lead to a void with a diameter of about 1 cm.

Anodic bonding, also known as *filed-assisted sealing* or *electrostatic bonding* was first reported in the late 60's (12). It can be carried out between a vast number of material combinations. For most microfluidic applications it is performed between silicon and borosilicate glass. This technique was used at CERN (13; 14; 15) to validate the design of the microchannels for the NA62 GTK and LHCb VELO LS2 Upgrade. Various microchannel layouts were etched in silicon wafers. The microchannels were subsequently closed by bonding in vacuum sodium-containing glass wafers at high temperature (320°C) and by applying an electric field. Closing the channels with transparent glass allows a direct view of the liquid flow (C_6F_{14} and bi-phase CO_2 for the GTK and the VELO respectively).

Hydrophilic Wafer Bonding is the most commonly used technique to form bonds between two silicon wafers. A high-temperature process forms a solid bond between the two wafers. This approach was used for the production of the NA62 cooling plates and is also used for the LHCb VELO upgrade (9). In the DEPFET process (16) discussed in section 11 both silicon wafers are oxidized prior to the wafer bonding and the oxide layer acts as a natural etch stop in the subsequent chemical thinning step.

Hydrophobic Wafer Bonding – Hydrophobic surfaces are obtained by removing the native oxide. Such surfaces are mainly characterised by the presence of Si–H groups. Since the oxide is usualy removed by hydrofluoric acid (HF), Si–F groups are also obtained. The transition from hydrophilic to hydrophobic surface conditions is assumed to be above a concentration of about 25% of Si–F bonds (17).

Low-temperature wafer bonding is needed when there are structures or layers that do not tolerate the annealing temperatures required for hydrophilic or hydrophobic bonding (18). Typically this involves the activation of the surfaces with wet chemical processes or with a plasma either to increase their hydrophilicity, which increases the number of hydrogen bonds, or to generate new types of bonds (19).

A variant of this method etches half of the microchannel in a wafer and the other half in another wafer. This alternative has the advantage that the microchannels halves can have semi-circular shapes and when bonded together they form a circular pipe. However, this method requires a very precise wafer alignment and the wafer bonding of two structured wafers can lead to lower production yields.

3.2 Embedding Approach or Buried Channels Technology

Wafer bonding is a critical step in the production of silicon micro-channel cooling devices. An excess of local bonding defects, if close to a fluidic channel, can create a relatively large surface exposed to the pressure from the cooling fluid, bringing to the premature collapse of the cooling device. However, local bonding defects are not always easily detected, and this imposes expensive and time consuming quality controls on the produced devices.

An alternative approach consists in fabricating the microchannels by embedding them directly into a single wafer (20; 21; 22; 23) based on the SCREAM process introduced in the early 90's by Shaw *et al.* (24). This approach has the advantage of being fully compatible with CMOS devices - thus offering the advantage of allowing for the introduction of cooling channels in CMOS chips after their production. This technique is described in greater detail in a dedicated section 12.

4 Accessible production facilities

Several facilities have produced MCC structures aimed at applications in high-energy physics.

CNM-IMB The Barcelona branch of the Spanish micro-electronics centre (CNM-IMB) has in-house capabilities to process 4" wafers. For the micro-channel cooling plate prototypes presented in Ref (25) a channel array with varying widths is etched in silicon with the deep-reactive ion etching (DRIE). A second DRIE step is performed on the backside of the wafer, that opens through-holes to define the inlet and outlet. The micro-machined silicon wafer was sealed by bonding to a blank Pyrex wafer in an anodic bonding process, at high voltage (1000 V) and relatively low temperature ($400^{o}C$). CNM also has access to equipment for the characterization of the cooling plates and a simulation model that yields adequate predictions for the cooling performance with mono-phase fluid cooling.

MPG-HLL The Semiconductor Laboratory of the Max Planck Society (MPG-HLL) is a central facility of the Max Planck Society with expertise in development, design, and fabrication of state-of-the-art silicon radiation sensors. The current technology includes all production steps for the fabrication of active pixel sensors (DEPFET), pnCCDs, silicon drift detectors, and silicon strip and pad detectors. After the development for the all-silicon-module fabricated in SOI technology (26), the laboratory is working on the implementation of micro-channel cooling into this concept (27). The results of these developments are summarized in section 11. The prototyping was done together with external industrial partners, in particular for the deep reactive ion etching (DRIE) of the channels into the handle wafer and the final assembly of the cavity SOI (CSOI). These two steps are currently being qualified with equipment suppliers before installation in the process line of MPG-HLL.

FBK-CMM Fondazione Bruno Kessler (FBK), is a private non-profit research centre working for the public interest. FBK-CMM (Centre for Materials and Microsystems) is an applied centers organization operating in the following area of science and technology: i) material and interfaces, ii) device & microsystem, iii) integrated system for enviroment and renewable energy. The CMM has the capability to realize silicon device in house using the internal Micro Nano Facility. The internal capability is based on two separate clean rooms: one is for "clean" technologies (mainly focused on radiation sensors development and production), where consolidated and tightly controlled Si-based technologies are implemented; and one for MEMS, where more innovative, less tightly controlled processes, including also potentially IC contaminating materials like Gold, are allowed. Furthermore FBK have capability on: i) Device Testing, where the processed wafers with active devices are tested for process control and functional characterization; ii) Material Characterization, with a wide range of material characterization techniques supporting the technological development in the Clean Rooms and the activities on new materials developed in CMM. Regarding in particular micro channel cooling devices, in the past 5 years FBK developed two different approaches in collaboration with AIDA-2020

partners:

1. Embedded microchannels: FBK developed a new approach to integrate the cooling directly into the silicon devices. The microchannels are formed in silicon using isotropic SF6 plasma etching in a DRIE (deep reactive ion etcher) equipment. Due to their peculiar profiles, the channels can be sealed by a layer of a PECVD silicon oxide. By avoiding high temperature steps, the process results compatible with CMOS devices, i.e. in principle the electrical performance of the chip should not be affected.

2. Silicon microchannels sealed by a Pyrex wafer: the microchannels are realized on a silicon wafer using a Bosch process optimized to the specific application in a DRIE equipment and then they are sealed by a Pyrex wafer using a wafer bonding technology based on anodic bonding. This technique allows to control very well the channel wall roughness. FBK also has the capability to realize on the same silicon wafer both the microchannel and the inlet-outlet holes for the gas/liquid used for the cooling.

EPFL-CMI The Center of Microtechnology (CMi) of EPFL is a complex of clean rooms and processing equipment for the training and scientific experimentation devoted to the users of micro-technologies. Its main mission is to provide basic and advanced training on processes and technologies; to offer access to the processing equipment available in the clean room; and to cooperate with other academic institutions and research centers. Therefore, the CMi's offer addresses:

1. Education,
2. Scientific research, and
3. Access to micro-fabrication processes

The operation of CMi is the responsibility of the staff. The staff is a team of engineers and technicians, specialists in micro-technologies who guarantee the availability of processing equipment, evaluate, install and operate processing equipment, train the users, develop new processing steps and improve the existing ones, and assist researchers with technical advice. The users of CMi are undergraduate students, graduate students, post-doctoral researchers. The core activities of CMi are laboratory experimentation and development of processes and techniques of interest to EPFL and to its partners. The user's access to the clean room is prioritized in the following order:

- educational activities
- internal research
- partnership research with other academic institutions

All activity in the clean room is invoiced on the basis of the costs of consumable and of hourly processing rates, varying with the status of the user (EPFL

internal, External Academics, Industrials). The available state-of-the-art equipment covers all the main needs for Electron beam lithography, Photolithography, Etching, Thin film deposition, Metrology and Packaging (bonding, dicing, micro-machining, polymer printing)

5 Pressure resistance of silicon structures

Since the foundational work of Petersen (28), paving the way to micro-electro-mechanical system (MEMS) applications involving the generalized use of silicon as mechanical material in micro-systems, the mechanical properties of crystalline silicon have been carefully investigated. However, mainly due to very high economical interests in play, the publicly accessible knowledge is very limited with respect to the enormous amount of advanced industrial applications in the MEMS field. The anisotropic nature of mono-crystalline silicon also contributes to some persisting confusion: the 2001 work from Kim et al. (29), for instance, stresses that the Young's modulus, Poisson's ratio, and shear modulus of mono-crystalline silicon, although always high, are transversely and vertically isotropic for silicon (111), whereas these vary significantly for silicon (100) and (110). For example, for silicon (100) and (110), the Young's modulus varies from 130.2 GPa to 187.5 GPa, whereas for silicon (111) it is transversely isotropic at 168.9 Gpa, regardless of the crystallographic orientation. More recent investigations (30) have also shown that large variations in the reported mechanical properties may be ascribed to very different testing conditions, due to the lack of a unified reference norm. As a matter of fact, as the author stresses, despite the widespread usage of MEMS devices, issues related to uncertain mechanical reliability remain a major factor inhibiting the further diffusion of their usage.

The case of a silicon channel subject to a non-negligible internal hydraulic pressure is not very common in present applications. In the framework of the AIDA2020 project it has therefore been decided to pursue a systematic study on the mechanical resistance to internal pressure of silicon micro-channels of different width in function of the thickness of the exposed silicon wall. The standard sample of silicon channel designed for the test is shown in Figure 4: by varying the channel width w and and the thickness of the top wall t2, it is possible to study the pressure resistance of silicon micro-channels as a function of these two important parameters, thus providing fundamental information for the design of future cooling devices.

The pressure tests are performed in the dedicated experimental setup shown in **??**. Connected to a pump capable of developing pressures up to 700 bars, the setup allows for precise and repeatable positioning of the sample into the mechanical fixture providing the hydraulic connection to the pump. The pressure in the channel is continuously monitored and acquired during the test, and it is progressively increased until the limit value is reached and recorded, when the sample explodes.

After the test, the exploded samples are further examined to verify the fracture characteristics. Indeed, a local wafer bonding defect, if relatively large and close to the channel, may offer a larger surface to the action of the hydraulic pressure, largely increasing the local stress in the silicon wall and decreasing the limit pressure for the sample. In this case, the starting point of the fracture through the silicon bulk will be visible in cross section at the junction corner between the two wafers. The few samples presenting this kind of fracture are declared defective and discarded from the data analysis. Correctly bonded

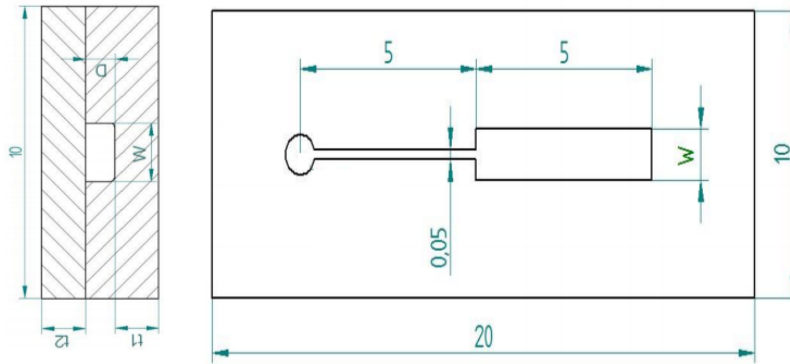

Figure 4: Schematic drawing of the standard sample used for the pressure tests on silicon micro-channels. Design by CERN.

samples present a fracture line starting from the bulk of the silicon wall and following one of the silicon cleavage planes. This is the case, for instance, of the SEM image of an exploded channel from a correctly bonded sample, shown in Figure 5.

A statistical analysis performed on the results from all samples qualified as "correctly bonded" yields the results in Figure 6. The positive effect on the maximum attainable pressure of decreasing the channel width and increasing the silicon thickness is clearly visible. however, a narrower channel will present a higher pressure drop for the same flow of refrigerant, while a thicker silicon wall will increase the cold plate's contribution to the detector material budget. Using the plot produced, it is possible to define the optimal parameters of the channel for every new silicon cold plate, based on the requirements of maximum test pressure, maximum allowed pressure drop and targeted material budget. For example, one can easily observe that, for the typical requirement of 150 bar as maximum test pressure, a silicon thickness of 100 μm above the channel is largely sufficient to operate in a CO_2 circuit a device designed with a 300 μm channel; while, on the other hand, a 70 μm silicon thickness may be dangerously close to the limit.

A detailed analysis of all the test conducted, also showing results for the dependence from other geometrical parameters is in preparation and will be reported in a future publication,

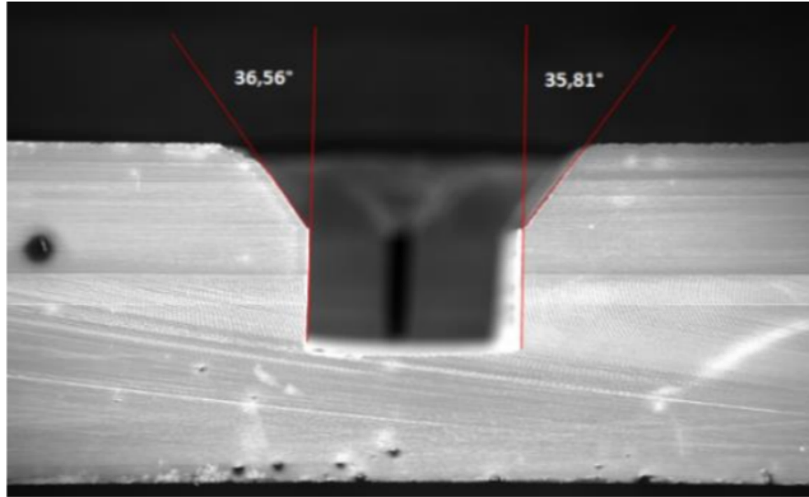

Figure 5: Example of channel fracture without wafer delamination: ”correct” fracture (SEM image taken at EPFL CMI)

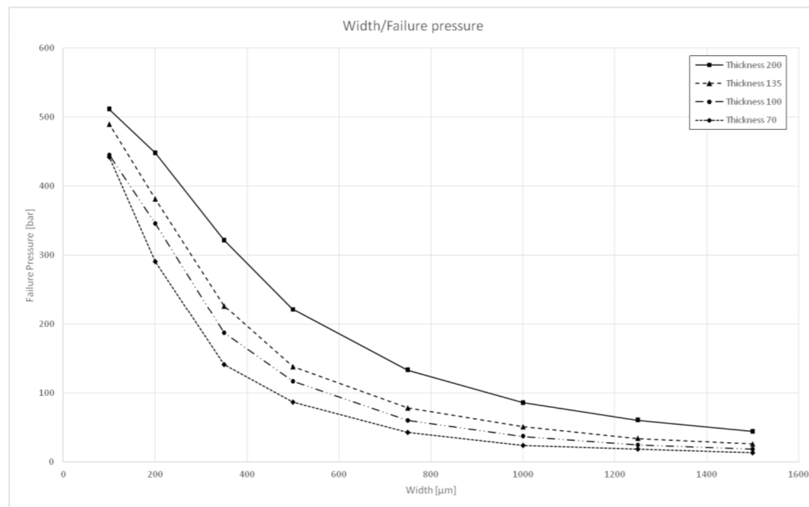

Figure 6: Limit hydraulic pressure for rectangular silicon channels as function of the channel width and of the wall thickness exposed to the pressure action

6 Connectors

Microfluidics has been an ever-growing field since decades. Nevertheless, to the best of our knowledge, standards are not available when it comes to fluidic connections. Even though some efforts are made to define guidelines for microfluidics in general, the wide variety of solutions developed are usually application-oriented. For the HEP community, common connection techniques are necessary in order to test prototypes on different test benches in various institutes as well as to interface microfluidics-based on-detector cooling systems to primary cooling circuits. The development of such standard connection techniques is part of the programme of AIDA2020-WP9. An important effort has been devoted to the development of versatile standard connectors. While the optimization of some of these techniques is still on-going, in particular related to additive manufacturing techniques, a list of standard connectors is now available for the HEP community. The most relevant techniques are listed in this section.

6.1 Commercially-available connectors

Among all commercially available microfluidic connection solutions the PEEK Nanoport Assemblies [1] from Upchurch Scientific have been determined as the most suitable for HEP. The 10-32 Coned Assembly has been used at CERN since 2010 to test the silicon/glass micro-channel cooling plate prototypes. This assembly contains an insert, a ferrule, a coned Nanoport, a gasket and a preformed adhesive ring (see Figure 1). It is rated by the vendor up to 69 bars and this has been verified experimentally at CERN [2]. Higher pressures can be reached by reinforcing the connectors with additional glue around the connectors. Metallic plates can also be added to reach pressures of hundreds of bars [3]. The PEEK connectors are aligned together with the gasket and the preformed adhesive ring to the inlets and outlets of the micro-channel plates, and they are clamped. They undergo a thermal treatment at 180C for 2 hours to develop a complete bond with the silicon substrate.

6.2 Soldered connectors

In both cases, a stack of metallic thin films is sputtered around the inlets and outlets of the micro-channel cooling plate. A typical stack developed by CEA-Leti in collaboration with CERN for silicon cooling plates is Ti(200nm)Ni(350nm)Au(500nm). The thickness of each layer can be varied and should be adapted to the metallization equipment, but this stack has proven to work in various cleanrooms.

The bond pads are patterned around the inlets of the microchannel device during the microfabrication process by a photolithography and metal etching sequence or by metal lift-off. Bond pads can also be sputtered afterwards on full wafers or single dies by sputtering the same metal stack through a shadow mask.

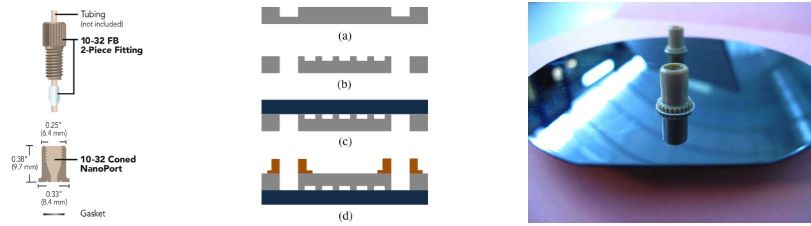

Figure 7: (left) Exploded view of the NanoPort Assembly 10-32 tested and validated for HEP applications. (center) Simplified microfabrication process-flow of micro-channel cooling plates; (a) Pre-etching of the inlets, (b) etching of the micro-channels and inlets, (c) anodic bonding of glass wafer and (d) glueing of the Nanoport connectors. (right) Nanoport connectors glued to a silicon/glass micro-channel cooling plate.

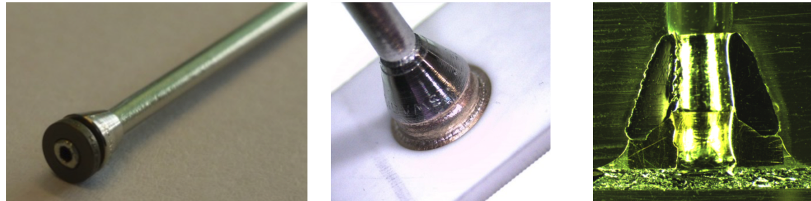

Figure 8: (left) Ferrules crimped around a stainless steel capillary. (center) Capillary with ferrules soldered to a ceramic substrate. (right) Cross-sectional preparation of ferrules crimped around a capillary soldered to a silicon substrate.

Two solutions have been developed to solder stainless steel capillaries to micro-channels cooling plates:

Chip-to-tube connections : this solution adapted from a development by Murphy et al. (31) uses ferrules crimped around the capillaries. It is of interest in particular for connecting prototype micro-channel cooling plates to experimental test-benches and laboratory cooling plants. Standard stainless steel capillaries are soldered directly on the surface of a microfluidic chip. This technique can be used on any type of substrate containing micro-channels on which a stack of metallic thin films can be deposited. A tool is required to hold the capillaries and the micro-channels in position on top of a hot plate. Filling material is added either between the ferrule and the cooling plate or around the ferrule. The ferrules are then heated with a soldering point tip to melt the filler. Alternatively, the assembly can go through a temperature cycle in an oven.

Machined connectors : this solution is used in the LHCb and NA62 experiments. A connector is machined in an alloy with a CTE close to the CTE of sil-

Figure 9: (left) Schematic cross-section of the machined connector welded to a capillary and soldered to a silicon substrate. (right) Picture of the 4 capillaries of the NA62 GTK detector welded to the Kovar connectors which are soldered to the silicon micro-channel cooling plate.

icon (e.g. Kovar for the NA62 cooling plates). This connector is LASER-welded to a straight capillary which is then bent according to the required routing in the experiment. The connector is coated with a stack of a few microns of Ti, Cu and Au or Ti and Au and it is held in position on top of the cooling plate with a dedicated jig. A filler material is wrapped around the connector (e.g. a wire of SnPb) and the assembly is inserted in a vacuum oven to undergo a temperature cycle.

6.3 In-plane low mass connections

A third connector solution was developed by IFIC (UVEG/CSIC) in Valencia, in collaboration with the University of Bonn and the semiconductor laboratory HLL of the Max Planck Society. It is intended for use cases where access to surface area of the silicon is impossible and where reduction of the material is essential. The custom 3D-printed connector of Figure 10 connects to the micro-channel cooling inlet and outlet on the sensor edge. This in-plane connection offers advantages in situations where the entire sensor is inside the acceptance and the material on top of the silicon must be minimized. It can also be used to connect several structures to form a long string. The opposite face of the connector presents an interface to commercially available hydraulic standards.

Three types of connectors have been printed that connect to:

- the Swagelok standard mechanical fittings for 6mm diameter pipes, primarily intended for standard laboratory tests
- the IDEX HS mechanical fittings (a standard in health sciences) for 1/32 “ diameter pipes, which offers a compact solution that can be easily connected and disconnected
- 1/32“ diameter PEEK tubes that are glued into the connector, for a low-mass permanent connection.

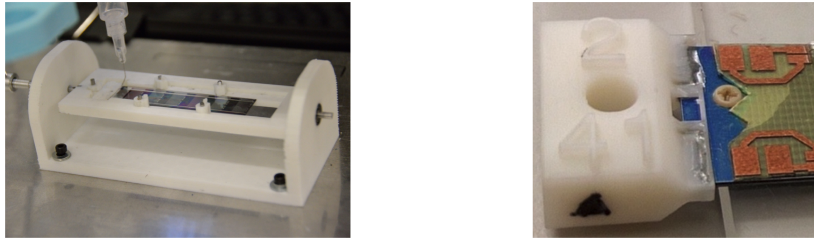

Figure 10: (left) Jig developed for the glueing of in-plane connectors on silicon substrates and (right) close-up of custom 3D-printed in-plane connector glued to a silicon substrate.

The plastic material guarantees small contribution to the material budget. The connection is sealed with Araldite glue in an automated gluing procedure.

The quality of the connection has been tested on a large number of samples. High-pressure operation was demonstrated in destructive pressure tests at CERN, where samples were shown to stand up to 80 bars. This is sufficient for mono-phase cooling solutions. Leak tests based on Helium detection have been performed on a dozen connections, initially at CERN and later in the installations of IFIC in Valencia. The Helium leak rates are of the order of $10^{-6} mbar.l/s$. The 3D-printed connectors have been used in extensive prototype tests in Bonn, at CERN and at IFIC.

7 Silicon micro-channel cooling plate fabrication

Two experiments have adopted micro-channel cooling plates as their cooling solution.

The **NA62 GigaTracKer** has pioneered micro-channel cooling technology at CERN, with single-phase liquid C_6F_{14} (32) cooling. The detector modules of both experiments rely on large silicon microchannel cooling plates to provide mechanical support to the pixel detectors and their associated electronics. The assembly process involve many steps including the soldering of metallic microfluidic connectors and the glueing of the hybrid detectors stacks to the cooling plates. The NA62 cooling plates have a footprint of 80 $\times$ 70 mm. They are thinned down to 210 μm in the acceptance region where the GigaTracKer (GTK) pixel detector is glued while the outer frame, where the four microfluidic connectors are soldered, is maintained at about 700 μm. Two connectors bring the coolant to the microchannels and two connectors recollect it to circulate it to the cooling plant. The thicker outer part of the cooling plate contains the manifolds that distribute the coolant into two networks of 75 parallel microchannels (200$\times$ 70 μm) each. The GTK modules have been operating successfully in the vacuum ($\approx$$10^{-6}$mbar) of the NA62 beam line since their first installation in 2014.

The **LHCb VELO** detector experiment plans to upgrade the VELO detector during long shutdown 2 with a cooling system based on two-phase evaporative CO_2 cooling in a silicon micro-channel cooling plate (33). The LHCb cooling plates have a constant thickness of 500 μm. They are bigger than the NA62 plates and their complex shape required the development of a dedicated dicing procedure based on through-silicon plasma etching. A single metallic microfluidic connector soldered to the cooling plate contains the inlet and the outlet manifolds. In this case the coolant is bi-phase CO_2 and each one of the parallel microchannels is etched in an optimised serpentine-like geometry to route them underneath the pixel detectors. The cross-section of the channels varies from 60 $\times$ 60 μm close to the inlet to 120 $\times$ 200 μm in the active area where CO_2 is boiling. The sudden increase in cross-section along the microchannels triggers the boiling. Two pixel detector tiles are glued on each sides of the cooling plate. The read-out flexes and electrical wires are cautiously routed along the stiff composites support legs together with the stainless steel cooling capillaries. Fifty-two modules are currently being prepared for the LS2 VELO Upgrade.

Figure 11 summarizes the main features of the cooling plates for the GTK detector modules and for the VELO cooling plates.

	NA62	LHCb
# of modules	3	52 (2x 26)
distance between modules	~10 m	2.5 cm
sensors	hybrid pixel	hybrid pixel
sensor size	60 x 38 mm	43 x 15 mm
sensors/module	1	4 (2 on each side of plate)
power dissipation (average)	~2 W/cm^2	~2 W/cm^2
coolant	liquid C_6F_{14}	evap. CO_2
cooling plate thickness	~200 µm	~500 µm
operating temp. on sensor	-10ºC	> -20ºC
max. operating pressure	~10 bars	~60 bars
safety pressure	~20 bars	~200 bars
operation in vacuum	primary vacuum of NA62	secondary vacuum of LHC
distance to beam	in the beam axis	5.1 mm

Figure 11: Features of the NA62 GTK detectors currently installed and of the LHCb VELO modules under construction for the LS2 Upgrade.

8 Design tools and simulation

The future development of micro-channel cooling systems relies on simulation to predict the thermal performance of prototypes and large-scale assemblies. It is vital to verify these methods experimentally and to gain a clear understanding of their reliability and limitations.

Studies reported in literature show that for single-phase flows the classic 1D semi-empiric correlations developed for macro-pipes only have very limited applicability in micro-channels. The established correlations for friction factor only work well in laminar flows, while those for heat transfer coefficient seem to require specific adjustments in all flow regimes (34). Successive studies have suggested that this might well depend on large experimental uncertainties and neglected scaling effects in the definition of the unidimensional models (35), but the issue is still subject of debate in the scientific community. However, the simulation of single-phase micro-channel cooling can be performed with standard 3D simulation tools coupling Finite-Volume-Modeling (FVM) and Finite-Element-Modeling (FEM). Indeed, full 3D numerical simulations of single-phase flows based on modern modelling approach of Reynolds Averaged Navier-Stokes (RANS) equations – nowadays implemented in many commercial CFD codes – have been proven to provide very reliable results, if a correct modeling approach is followed (36). The simulation allows for a rapid evaluation of design variants and hence to optimize the design with the minimal number of prototype production cycles. The simulation provides a complete characterization of the main aspects of the design. Finite-volume/finite-element methods give access to a large number of parameters related to the hydraulic properties of the circuit (flow rate, pressure drop, etc.) and the cooling performance (i.e. temperature gradient between heat source and heat sink for different thermal loads and the thermal figure of merit) of the design.

As an example, Figure 12 shows the simulation that was performed for Ref. (27). The design is implemented in numeric simulation software ANSYS (v17) starting from the 3D model produced with a standard CAD software. The mesh consists of several million elements, which allows a faithful 3D rendering of the details of the geometry. The CFX package of ANSYS provides detailed results for both the flow rate and thermal performance of the design. The volumes representing the fluid demand a much finer granularity than the solid parts, which only play a role for the thermal calculations (25). It is therefore recommended that the mesh for both is determined separately.

Several groups have verified the simulation results in measurements on prototypes (25; 27). Good agreement, typically to within approximately 10%, is found in predictions of the temperature, pressure and flow for a variety of coolants and channel geometries. We conclude that standard FVM/FEM simulation tools are quite reliable for systems based on single-phase cooling and can be of great use in the comparison of similar design variants and extrapolations to other materials, coolants, etc. with very well known properties.

The same software packages can also be used to predict the integral mechanical properties of the assembly. However, while the static and dynamic

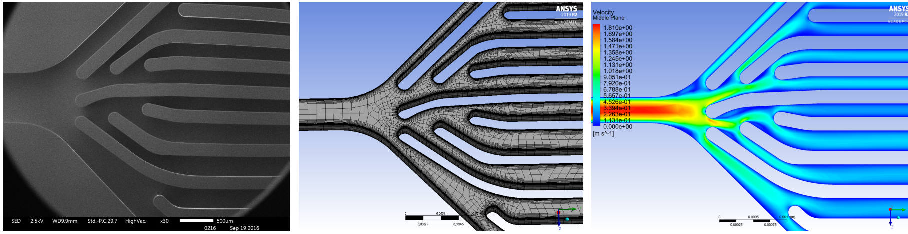

Figure 12: Simulation of the circuit implemented for the study of Ref. (27): (left) photograph of the circuit, (middle) mesh determined by ANSYS for the same region, and (right) liquid flow velocity in the center of the channel.

mechanical properties of a monolithic component in crystalline silicon can be very precisely predicted, particular care must used in calculating the interfacial strength of two bonded silicon surfaces. The mechanical properties at the interface between to joined silicon surfaces are indeed highly dependent on the presence of local imperfections in the close vicinity of micro-structured cavities. For the structures of Figure 12, for instance, the simulation was used to predict the maximum pressure that the manifold should be able to hold. In the comparison of the results with destructive pressure tests, most samples broke at significantly lower pressure than was predicted by the FEA simulation. A significant variation was found among the prototypes, which indicates an imperfect control of the wafer bonding process for these very early prototypes.

The NA62 GigaTracker design team relied on a mixture of analytical calculations and finite-element analysis to predict the thermal performance of the micro-channel cooling plates (37). The measured thermal performance of full-scale prototypes matches the prediction to very good accuracy. The study of the pressure resistance of a large number of simple test samples is also found to be in good agreement with the ANSYS prediction, but these studies focus on samples with perfectly bonded interfaces and do not take into account the possible delamination effects due to local bonding defects.

The situation is far more complex when dealing with the prediction of the cooling performance of two-phase evaporative flows in small channels, nowadays used in most pixel detectors. Indeed, only heavy specialist custom codes providing Direct Numerical Simulation (DNS) of the full two-phase Navier-Stokes equations can provide reliable numerical simulations of two-phase flows (furthermore, only in extremely simple channel geometries). No RANS-based code commercially available today has the capability of providing reliable forecasts of the thermohydraulic properties of two-phase flows in small diameter channels.

On the other hand, the confinement effects typical of mini- and micro-channels highly influence the boiling patterns and, henceforth, the thermal and fluidic behaviour of evaporative flows. This renders the classical 1D correlations and forecast approaches, historically developed for large channels, very unreliable when applied to these geometries. This is particularly true for CO_2, for which the amount of good-quality experimental reference data available in

the literature for CO_2 in mini- and micro-channels is extremely limited and the development of reliable predictive thermo-fluidic models is suffering large delays.

9 The CERN micro-channel cooling test stand

The CERN EP-DT laboratory already developed in the past a test station for the characterization of micro-channel devices with single phase liquid refrigerants. Based on a vacuum vessel for pure adiabatic boundary conditions during testing, the test stand was successfully used for the design, development and characterization of the micro-channel silicon cold plates for the NA62 GTK detector, the first HEP detector adopting this technology for the thermal management of its pixel modules (32).

Reliably establishing adiabatic boundary conditions is particularly important for a correct characterization of micro-channel silicon devices due to their extremely small thermal inertia and their large surface of heat exchange. This setup is now also available to test and characterize liquid-operated micro-channel devices. The fluid used is C_6F_{14} at controlled temperatures between +30° and -25°. The measured performances can however be transferred to different fluids via classical fluid dynamics correlations by scaling the recorded values on the specific fluid properties (density, viscosity, specific heat and thermal conductivity).

Detailed tests in a controlled are particularly relevant for two-phase evaporative cooling systems. Indeed, the confinement effects typical of mini- and micro-channels highly influence the boiling patterns and, henceforth, the thermal and hydraulic behaviour of evaporative flows, and one cannot rely on the classical correlations and forecast approach. This is particularly true for CO_2, where reliable laboratory measurements are scarce, due to the high pressure involved and the absence on the market of refrigerating machines circulating CO_2 in well-controlled conditions.

Furthermore, it is often very difficult to compare published measurements coming at different times from different laboratories, due to different testing conditions and procedures, and due to the influence of poorly controlled boundary conditions. For this reason, the amount of good-quality experimental reference data available in the literature for CO_2 in mini- and micro-channels is extremely limited and the development of reliable predictive thermo-hydraulic models is still lagging.

In the context of the WP9 activity of AIDA-2020, a new test stand dedicated to high precision measurements of the thermo-hydraulic properties of boiling flows of CO_2 has been designed and realized. Besides obtaining a larger and more reliable database for evaporative CO_2 pressure drops, heat transfer coefficients and flow patterns in small diameter pipes and micro-channel devices, the objective of the new experimental setup is to establish a new and repeatable standard for future measurements in other laboratories.

The setup can be divided into two main parts: (i) a stand-alone, transportable refrigeration unit which supplies minimally sub-cooled or saturated CO_2 at a controlled working pressure (38), and (ii) an experimental test circuit. The two-phase mechanically pumped loop (i), designed and built at CERN, delivers stable flows at controlled saturation temperatures from +20° C to -25° C. The loop is designed in such way that under normal working conditions the fluid

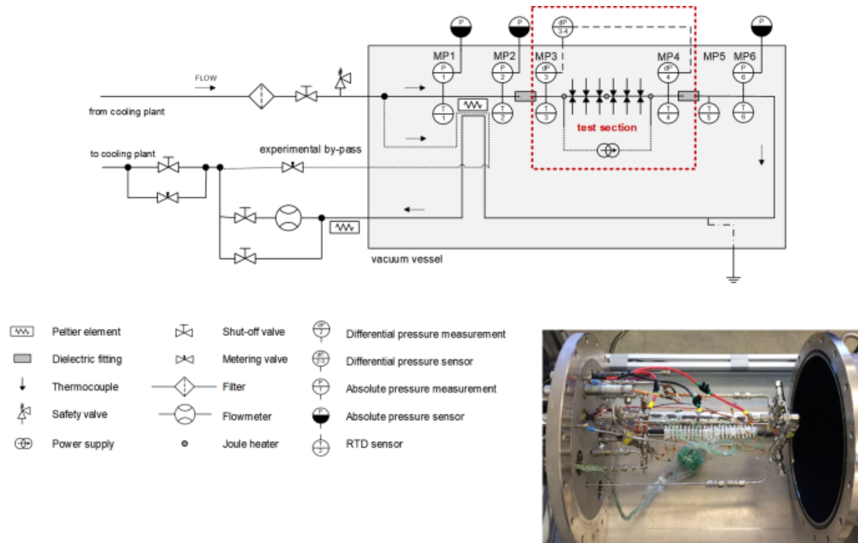

Figure 13: Schematic representation (PI Diagram) of the new CERN test stand for high precision characterization of CO2 boiling flows in mini- and micro-channels.

is delivered at saturation conditions at the inlet of any experiment with small scale CO_2 evaporators. The flow coming from the cooling plant is circulated through the test circuit (ii) as shown in Figure 13.

Also in this case, in order to ensure perfectly adiabatic boundary conditions, the tests are carried out within a stainless steel vacuum vessel. The most crucial components with respect to the direction of the fluid flow are described in the following. After entering the vacuum vessel the fluid passes the first measurement point (MP1) where the temperature of the fluid and its absolute pressure are acquired. A custom-made resistance temperature detector (RTD, PT100, 4-wire configuration) is being used and the sensing element is directly submerged in the flow whilst no major flow disturbance has to be expected. These sensors were calibrated to measure within an uncertainty of 0.015° C. Here the temperature of the fluid is measured at the bottom half of the incoming flow. For the absolute pressure measurements 3 mm OD stainless steel pressure lines are fed through the vessel wall, whilst the actual sensor (General Electrics UNIK 5000 series) is installed outside the vacuum vessel. The reading of MP1 is used to validate the set parameters of the cooling plant. Like all additional measurement points downstream this MP is realised by means of fluid-mechanical cross fittings or a combination of a cross and T-junction fitting (Swagelok). Figure 14 depicts schematically an example for a measurement point configuration.

Subsequently a Peltier element is installed in the circuit to function as a pre-heater or pre-cooler to bring the fluid to a desired temperature and thus control the inlet quality of the experiment. The Peltier element is fixed between

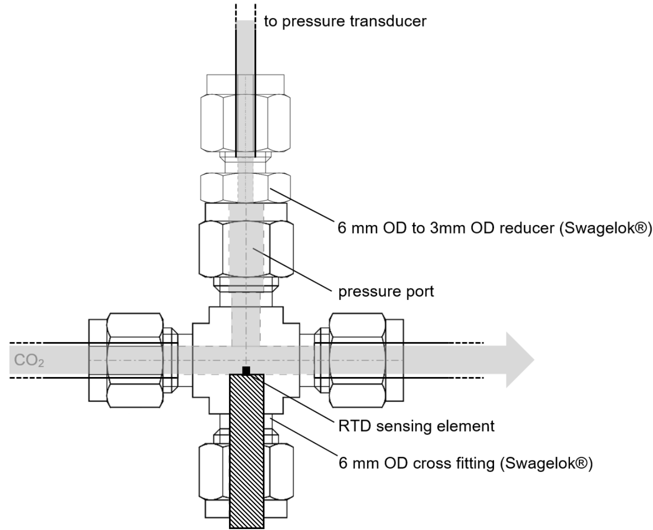

Figure 14: In-fluid pressure and temperature measurement point.

small copper blocks mounted onto the 6 mm OD tubing of the main circuit whilst one side of the Peltier is brought in contact with the return line for the correct functionality of the Peltier effect in vacuum. The Peltier is connected to a power supply and a relay outside of the vacuum vessel so the user is able to switch between its heating and cooling properties.

After this heating/cooling section the fluid passes through a second measurement point (MP2) where again temperature and pressure are acquired in the described fashion. Henceforth there is a dielectric fitting separating this measurement point from a third measurement point (MP3) which acts as the inlet of any test section, where a differential pressure port is installed. Dielectric fittings were installed on either side of the experimental tube to isolate the experiment from any stray currents caused by the connected electronics. The setup is designed to test various small scale CO_2 evaporators such as single tubes and multi-micro-channels. A fluid-dynamical adapter is installed accordingly to reduce the external diameter from 6 *mm* OD to the one of the device under test.

To measure the local outer wall temperature with an uncertainty of 0.1° C, pre-calibrated K-Type thermo-couples are used. In particular, in the case of single tubes, they are fixed by means of a steel-reinforced epoxy putty along the upper and the lower half of the tube resulting in six pairs within a distance of 30 mm. A detailed description of the design and production of the test station are available in Ref. (39).

The Joule effect is used to apply the desired heat flux to the test section. For silicon micro-channel devices a silicon mock-up is generally used to simulate

the Pixel module coupled to the device. This is a silicon chip of controlled planar dimensions and thickness, coated in clean room with a resistive metal layer, to which electrodes are soldered. For single tubes the direct Joule effect is generally used to generate the heat flux directly at the pipe wall. In this case, three copper electrodes are clamped and screwed onto the tubes. For this setup the configuration of two anodes to the left and right side of the tube and one cathode in the middle was chosen for security and accuracy reasons to avoid leakage currents beyond the test tube. Outside of the vacuum vessel a power supply delivers the required current.

Upon leaving the device under test, the fluid passes the fourth measurement point (MP4) where differential pressure and temperature are acquired as the outlet parameters of the experiment. The pressure drop between the inlet and the outlet of the device under test is measured with a maximum uncertainty of 1.5 $mbar$ with a differential pressure transducer (Endress + Hauser) placed outside of the vacuum vessel. The following two measurement points are installed for monitoring reasons and possible upgrades in the future (temperature, MP5 temperature and absolute pressure, MP6). After passing MP6 the fluid exits the vacuum vessel again. Two different flow meters are used for this setup covering two different test ranges. For flow rates from 0.16 to 4.0 g/s the Coriolis mass flow meter integrated in the cooling plant is used. However, for flow rates from 0.16 g/s down to 0.003 g/s an external Coriolis flow meter (Bronkhorst Mini-Coriflow M16) with an accuracy of 0.2% of reading (see Figure 13 is used in fully vaporized conditions after operating the dedicated by-pass valves. The readout and control of all components is operated with National Instruments hardware and LabView software and all relevant data are stored on a standard PC for further data processing.

The setup was designed to be very versatile without paying any penalty on its accuracy levels. Its wide range of possible test parameters allows for the creation of a consistent data base on evaporative CO_2 pressure drops, heat transfer coefficients and flow patterns in small scale evaporators. Especially the wide range of inlet conditions achievable (temperature, pressure and mass flow rate) is a unique feature in this field of research.

10 Measurements of CO_2 boiling in micro-channels

Extensive measurements campaigns on CO_2 boiling flows have been performed in the new CERN test facility. Measurements have been executed not only on multi-channel silicon devices, but also on single round tubes in stainless steel, with Internal Diameter (ID) of 0.5, 1 and 2 mm. While direct tests of multi-channel silicon devices are required in order to define the performance of different device configurations adapted to specific detector modules, precision measurements on single channels are extremely useful to verify the limits of applicability to CO_2 flows of models and 1D correlations generally used for the design of evaporators. Furthermore, as the mentioned ID's fall in the typical range of the long tubular evaporators presently adopted in most of the cold silicon trackers at LHC and HL-HLC, these measurements directly provide useful information to the designers of these detectors.

Accurate measurements of CO_2 flows in small pipes are very rare in literature, due to the intrinsic difficulty linked both to the absence of commercial refrigeration units units circulating CO_2 in controlled conditions and the high pressure involved, requiring specialized piping. For this reason, the CERN test facility has been accurately documented for possible duplication and is now being exploited for long-term systematic state-of-the-art measurements on CO_2 flows in all the parametric range of interest for present and future applications in silicon detectors.

A typical example of a parametric result obtained is reported in Figure 15, where the measured value of the Heat Transfer Coefficient (HTC) for round pipes of 1 mm and 2mm ID is reported as a function of the saturation temperature for different heat and mass fluxes. A large variation of the HTC in the observed temperature range is immediately visible, increasing of a factor 4 to 5 with the increase of saturation temperature from -25° C to +15° C, a phenomenon that is not correctly foreseen by any model available in the literature.

A second example can be used to show in detail the limits of using standard published models for the forecast of HTC of CO_2 boiling in very small ID pipes or channels. Figure 16 reports the measured value of the local HTC in a 0.5 mm ID pipe as a function of the vapour quality at a mass flux of 200 $Kg/(m^2 \cdot s)$ for three saturation temperatures. For each condition, the values predicted by three well known 1D correlations are shown for comparison. It is possible to see how the semi-empirical correlations provide a reasonable forecast of the measured value only when the experimental conditions are similar to those originally used as reference by the authors to develop them. This observation makes it clear that, for the design of the future detector thermal management systems, it is of fundamental importance to produce an as large as possible and accurate database of basic measurements. More generally accurate correlations can be formulated on the basis of these new results. Meanwhile it is possible to use the experimental results to benchmark all the existing correlations and provide the detector designers with clear indications on which correlation should be used depending on the specific configuration adopted.

Detailed results from measurements of both pressure drop and heat transfer

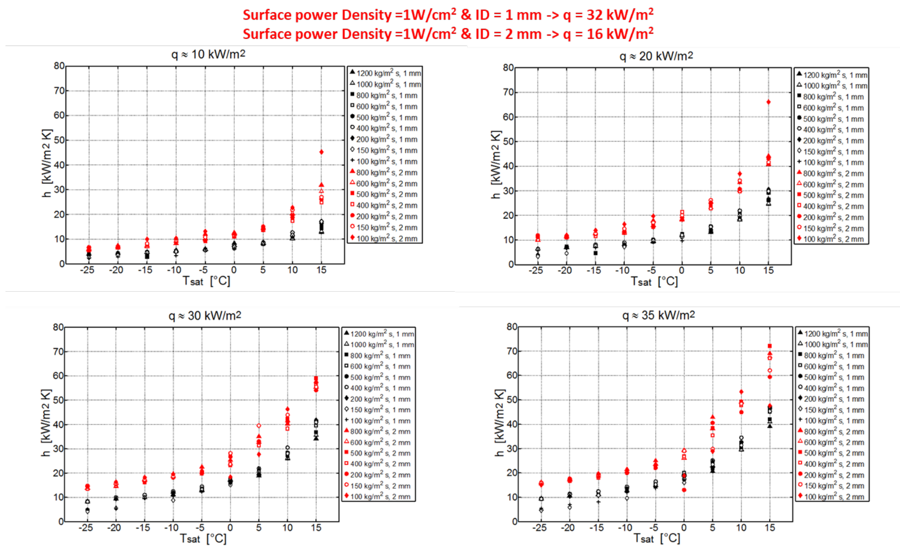

Figure 15: Heat Transfer Coefficient as a function of saturation temperature varying the mass and the heat flux for single stainless steel tube of 1 and 2 mm inner diameter.

coefficient in many configuration are to be published elsewhere (40), (41)

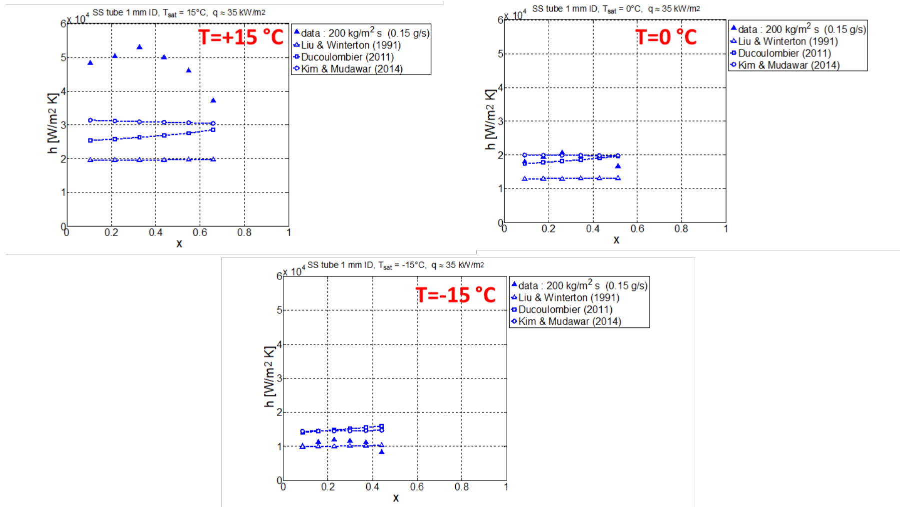

Figure 16: Measured Heat Transfer Coefficient as a function of vapour quality at different heat fluxes for a stainless steel tube of 0.5 mm ID, and comparison the value predicted by three well known 1D correlations

11 Integrated micro-channels in sensitive Silicon ladders

The applications of micro-channel cooling in NA62 and LHCb are based on the use of silicon cooling plates. In this approach the cooling plates must be integrated with the active detector elements in a gluing step. The proposal of Ref. (27) goes one step further and integrates the cooling channel in a handle wafer that is bonded to the active silicon sensor in a high-temperature wafer-bonding step. The result is a monolithic all-silicon ladder (26), with an integrated cooling circuit. As shown in figure 17, the process follows the steps used to produce the DEPFET ladders for the Belle II pixel detector (42) and future e^+e^- colliders (43), but can be adapted to any classical single-sided silicon (strip or pixel) detector design.

Two generations of such structures have been designed at IFIC Valencia. Small batches of prototypes were produced by the semiconductor laboratory (HLL) of the Max Planck Society in Munich. An extensive characterization was performed at Bonn University, IFIC and CERN with two mono-phase coolants: water and C6F14. Thanks to the very close integration of the heat source and the coolant, these structures achieve a thermal figure of merit ($TFoM$) down to $\sim 1K/(Wcm^2)$ (27). The results are in good agreement with a finite-element simulation in ANSYS.

A number of further structures and finite-element simulations aim to increase the level of realism. In complete detector designs an additional barrier to the heat transfer may be present due to the bump bond interconnection of the Front End or auxiliary ASICs to the sensor. The effect has been estimated in Finite Element simulation to lead to a deterioration of the $TFoM$. New prototype structures with bump-bonded dummy ASICs to validate the simulation with measurements have been prepared at HLL-MPG and are awaiting characterization at IFIC at the time of writing.

In the first batch of prototypes had a cooling circuit only under the end-of-ladder area, where the power density is typically highest. The second generation of prototypes also includes samples where a cooling channel covers the rim of a larger-area ladder area ($10 \times 1\ cm^2$). This is found to yield an adequate cooling performance for moderate power density sensors, with the performance limited by the heat transfer across the sensor.

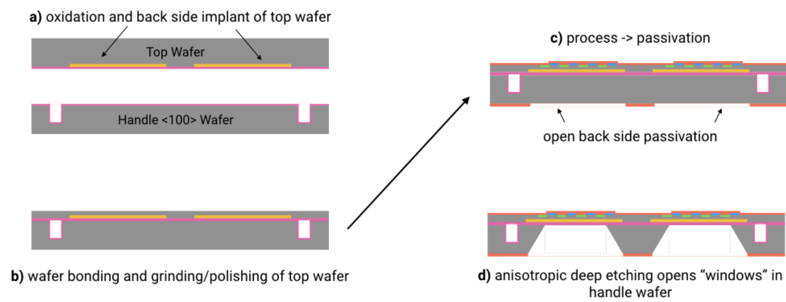

Figure 17: Figure 1. The process sequence for production of thin silicon sensors with electrically active back side implant and integrated cooling channels starts with the oxidation of the top and handle wafer and the back side implantation for the sensor devices; cooling channels are etched into the handle wafer before bonding (a). After direct wafer bonding, the top wafer is thinned and polished to the desired thickness (b). The processing of the devices on the top side of the wafer stack is done on conventional equipment; the openings in the back side passivation define the areas where the bulk of the handle wafer will be removed (c). The bulk of the handle wafer is removed by deep anisotropic wet etching. The etch process stops at the silicon oxide interface between the two wafers (d). The cooling channels are only accessible after dicing of the wafers.

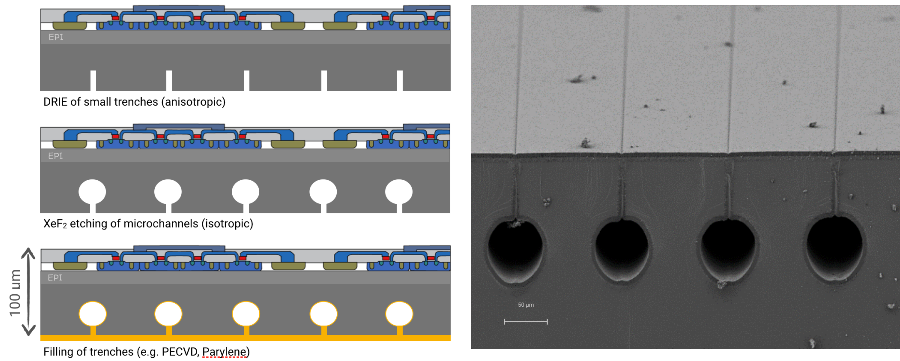

Figure 18: (left) Simplified process-flow for the fabrication of buried microchannels on the backside of a monolithic pixel detector. (right) SEM image of buried microchannels.

12 Integrated cooling channels in CMOS devices

A CMOS-compatible microfabrication process was developed at CERN to embed microfluidics into silicon dies. This process is of particular interest to fabricate cooling microchannels on the backside of monolithic pixel detectors.

A demonstrator is currently being produced by post-processing functional MALTA chips (44) in the class 100 (ISO5) MEMS cleanrooms of Center on MicroNanofabrication (CMi) at the Swiss Federal Institute of Technology (EPFL). The fabrication starts by patterning small trenches (3×10 μm) etched into the backside of the pixel detector to a depth of 30 μm. After passivating the sidewalls of the trenches, microchannels are etched isotropically with XeF_2 at the bottom of the trenches. The trenches are then sealed with 5 μm of parylene. A 3D-printed connector was designed and a procedure to glue it on the backside of a MATLA chip was validated (see figure 19). This connector is foreseen for testing purposes only and further optimisation is required to minimise its mass penalty. Fluidic tests have been performed and the system holds 110 bars. It is leak tight with up to an He leak rate of 10^{-8} mbar·l/s. After the introduction of the buried channels the CMOS chip remains fully functional and has successfully detected particles from a radioactive source. A full set of electrical tests and a testbeam are foreseen to characterise MALTA chips with embedded microchannels.

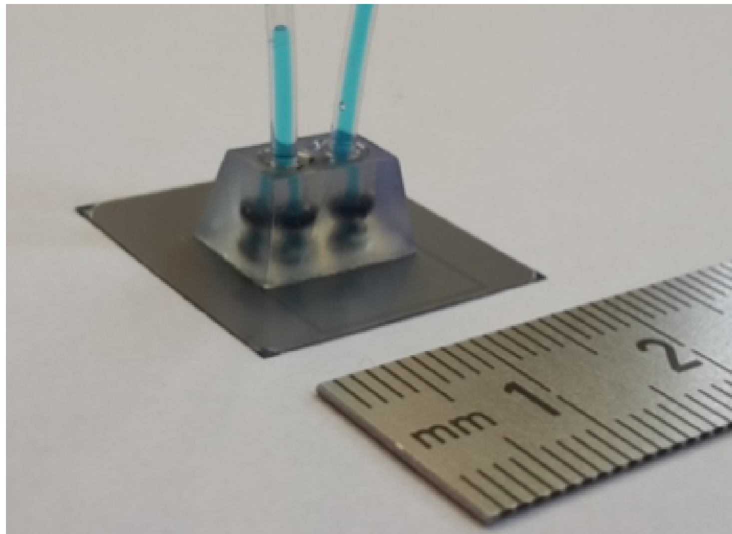

Figure 19: 3D-printed connector with plastic capillaries glued to a 100 μm thick MALTA chip.

13 Future applications in high-energy physics

A broad consensus exists in the HEP community that the collider facility to succeed the LHC at the energy frontier should be an electron-positron collider with a centre-of-mass energy that is large enough to produce Higgs bosons. Possible realizations include designs for a linear collider - the International Linear Collider (45; 46), to be hosted by Japan, and CERN's Compact Linear Collider (47; 48) - and circular colliders - FCCee (49) at CERN and CEPC (50) in China. The experiments at such a facility can provide superb measurements of the Higgs properties and interactions, of electro-weak precision observables and (at a later stage) top quark couplings.

To achieve this goals the detectors must be instrumented with excellent vertex detectors and tracking systems. The total contribution to the material budget of the tracker should amount to less than 10% of a radiation length (46), an order of magnitude less than the trackers installed in the ATLAS and CMS experiments. The vertex detector and tracker design must therefore explore new solutions for support and cooling that go beyond today's state of the art.

Electron-positron colliders present a very different environment than energy-frontier hadron colliders such as the Tevatron and LHC. In comparison, the radiation hardness requirements are relatively relaxed, with a maximum displacement damage due to non-ionizing interactions equivalent to approximately $10^{10} n/cm^2/year$ for CLIC (47) to several times $10^{12} n/cm^2/year$ for CEPC (50) (the total fluence is scaled to the equivalent 1 MeV neutrons according to the NIEL hypothesis (51)). Room-temperature operation is therefore generally possible. Also the requirements on the read-out speed tend to be more relaxed. The power density for the highly pixelated vertex detector (52) is expected to be less than 100 mW/cm^2.

In the relatively less demanding environment of lepton colliders, cooling through a forced convection of gas may be adequate under certain conditions. Recent experience with air-flow cooling in the STAR heavy flavour tracker (53) and the vertex detector of the Belle 2 experiment (42) show that this approach can be successfully deployed in silicon detector systems with stringent requirements on mechanical stability. Also one of the designs of the ALICE ITS upgrade (54; 55) and the Mu3e (56) design rely very heavily on gas-flow cooling. Two groups have set up test facilities to evaluate the cooling performance and the impact of the air flow on the stability of light-weight detector structures: the CLIC group at CERN (57) and the University of Oxford (58). The latter facility was built with support from the AIDA2020 project and is open to external users.

The detector concepts developed for the linear collider projects ILC and CLIC rely on air-flow cooling, in combination with pulsed powering of the detector. The spill structure of linear colliders, with a duty cycle of a few per mille, allows for a reduction of the average power consumption by a large factor and hence reduces the load on the cooling system. The circular collider detector concepts have adopted the same requirements and a similar design as the linear collider detectors. However, as circular colliders are DC machines, pulsed power-

ing is not possible and the power management requires much greater attention, and possibly a different set of solutions.

Micro-channel cooling can be a valuable solution at high-energy electron-positron colliders. It offers a very efficient way to remove the heat from the detectors, with excellent control over the cooling performance. Integrated solutions, such as those presented in section 11 and section 12, are potentially compatible with the very challenging material budget. Thus, micro-channel cooling can complement gas-flow cooling in detector regions with higher power density or stricter cooling requirements. Also for large-area tracking systems, where the logistics of air cooling have not been addressed, micro-channel cooling can be a competitive solution. The case for micro-channel cooling is particularly compelling at colliders with a 100% duty cycle, as envisaged by the FCCee and CEPC projects.

On a somewhat longer time line, a future *pp* collider is envisaged with a centre-of-mass energy well beyond that of the LHC. The HE-LHC and FCChh projects (59; 60) at CERN and the SPPC (61) in China could achieve centre-of-mass energies up to 100 TeV. These facilities represent a severe challenge for the design of the silicon trackers, as the total NIEL fluence will locally reach up to nearly $10^{18} n/cm^2$ (1 MeV neutrons) over the lifetime of the experiment, well in excess of the $10^{16} n/cm^2$ of the HL-LHC. The power density of highly granular pixel detectors is expected to be 1 W/cm^2 or more.

The next generation of very high-energy *pp* colliders requires novel solutions to avoid annealing and thermal runaway of the sensors. Ultra-low-temperatur operation, possibly below -30° C, is required. In practice, CO_2-based systems are limited to -40° C (3). While novel coolants are being investigated that could bring down the operation temperature of the cooling system, it is important to keep the temperature gradient between coolant and detector as low as possible. Micro-channel cooling, with its unrivalled thermal figure of merit, is therefore a very promising solution for the most challenging regions of the detector.

It is clear that micro-channel cooling offers important advantages. At lepton colliders, micro-channel cooling can be deployed in combination with gas-flow cooling, where the micro-channel system provides better cooling performance for parts of the detector with higher power density. The excellent thermal figure of merit and the much reduced contribution to the material budget render micro-channel cooling an interesting alternative for future hadron colliders.

14 Summary

Micro-channel cooling is a promising new technique to evacuate the heat generated by high-density silicon tracking and vertex detectors. The close integration of heat source and heat sink yields unrivalled cooling performance, with thermal figures-of-merit for realistic systems down to 3 $K \cdot cm^2/W$, a factor four better than optimized traditional cooling solutions. At the same the contribution to the material budget can be reduced considerably and the close matching of thermal expansion coefficients avoids deformation of the system under a heat load. Thus, micro-channel cooling provides a competitive solution for future electron-positron colliders, especially for circular colliders. The case for micro-channel cooling is even more compelling in future ultra-high-energy hadron colliders.

The first generation of high-energy physics experiments to adopt this new technique has finalized the production of silicon cooling plates for their pixel detectors. The successful operation of the NA62 GigaTracker yields a convincing proof for the reliability of micro-channel cooling. The LHCb VELO upgrade is expected to demonstrate the feasibility of two-phase evaporative cooling in micro-channels.

A large-scale deployment of micro-channel cooling in high-energy physics is made possible by a number of developments. A close collaboration with technological centres with in-house production capability (CNM-IMB, EPFL, FBK, HLL) has been key to develop optimal production processes for different applications. A deep understanding of the mechanical properties of cooling structures and of the cooling performance of two-phase systems is developed through an extensive set of measurement on prototypes and simple test structures. Standard connectors provide an efficient solution for new groups and guarantee high-quality connectivity.

A complete integration of the micro-channels and the sensitive detector elements is possible. Two groups have demonstrated the feasibility of embedding micro-channels inside silicon detectors, in an all-silicon structure compatible with a classical silicon pixel or strip detector and in a working CMOS sensor.

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