Minutes of the RADWG meeting held on 22 April 2010

Present: Thijs Wijnands, Daniel Kramer, Chiara Bracco, Markus Brugger, Gonzalo Penacoba, Erik van der Bij, Evangelia Gousiou, Roberto Losito, Christian Paillard , Ketil Roeed, Claude Dehavay, Aurelie Pascal, Pierre Dahlen, Javier Serrano, Giovanni Spiezia, Miriam Munoz, Helmut Jena, Reiner Denz, Antonio Marin, Julien Palluel

Matters arising – (Thijs Wijnands, Daniel Kramer):

- It was announced that starting from 1 May 2010 Thijs Wijnands will not be involved anymore in the RadWG and its related activities but remain the RSO of the EN department on full time. His current responsibilities will be distributed as follows:
    - RadWG chairman – Markus Brugger
        - D.Kramer remains the scientific secretary
    - CNRAD test coordination and material handling – Daniel Kramer
    - Radiation tests and support to users for radiation tolerance of electronics – Giovanni Spiezia
    - RadMon operation – Alessandro Masi
    - RadMon development – A.Masi, G.Spiezia, D.Kramer
- CNRAD Users requiring access to the computer for the remote reset need to ask Nicolas De Metz-Noblat (this was later changed to Alastair Bland as he has the official rights). The access to the pdf file with the remote reset procedure is restricted to RadWG members only.
- A proposal for a new proton/mixed field test facility will be presented to the May LHCC. It could be built in the East area and will require the Dirac experiment to be dismounted
- The CNRAD radiation field interface was updated with the dose calibrations announced last year and is available at the following link (click the dragon). The new test positions will be included later.
- Additional monitoring added to the WorldFip repeater in CNRAD. The 2.5V and 5V regulators are measured online (2.05/4.5V currently) and a remote reset of the FPGA was added as well. A third device will be tested later in the year with voltage regulator and monostable recommended by C.Pignard (HTC123 monostable and LM317 2.5V voltage source).

Proton and HI induced SEL in a Xilinx XC95108 – (Thijs Wijnands):

- The Xilinx CPLDs are extensively used in the LHC power converters and the interlock systems.
- The device XC95108PQ100 is based on 5V FastFLASH technology and was produced in 1998.
- In 2003, it was tested with 60 MeV protons and exhibited a very low SEU cross section
    - 2x(3+3) devices were tested (95144-10PQ160 and 95144-15PQ100)
    - 2 suspected SELs, documented in *AB-Note-2003-041-PO*
- During the 2008 tests in CNRAD 3 crashes of the power converter were observed and the forth one was a catastrophic failure.
    - CPLD observed under microscope and the damage zones around the power lines clearly pointed to a SEL (electrical overstress)
- The HIREX company was hired to characterize the 5V CPLDs for SEL and SEFI with heavy ions
    - Devices were un-lidded and placed on temperature regulated test boards in vacuum

- Tests with low penetration ions were conducted in UCL Belgium in December 2009 and with high penetration ones in Radef Finland in January 2010. Additional tests with 250MeV protons were done in PSI.
- The onset of SEFI and SEL is at the LET of about 7 MeV/(mg/cm^2)
- The cross section at 15MeV/(mg/cm2) is few 10^{-5}cm^2 for SEFI and SEL
  - The maximum LET which can be realistically obtained in the LHC mixed field environment in Si is about 15 MeV/(mg/cm^2)
  - Stepwise current increase suggests micro latching
  - SEFI type 1 could be recovered with a warm reset
  - SEFI type 2 requires a power cycle and is much more frequent
- One JTAG failure was observed as well (renders the programming impossible)
- Temperature scan showed an improvement of 1.7x if temperature was lowered from 85 to 50^{o}C
- The cross check measurements with 250MeV p+ showed unexpectedly low cross section for SEFIs type 2
  - Sigma SEL (4 devices) ~ 2.7x10^{-12}cm^2
  - Sigma SEU (4 devices) ~ 9x10^{-13}cm^2
  - Sigma SEFI2 (4devices) ~ 2.5x10^{-11}cm^2
  - Attempt to burn the CPLD failed! After 2 SEL events, the current was kept for 60 s (1.5 resp. 2.5A)
- It is so far not very clear how to extrapolate the heavy ion measurements to the expected mixed field conditions in the LHC.
- It is clearly much better to test the devices if possible at 250 MeV than at 60MeV in order to increase the chance to see SEL or eventually SEFIs for some devices
- The price for the heavy ion tests was about 10keur

CERN Fip project - discussion – (E.van der Bij):

The uFip chips are provided by Alstom, but the latest generation is several hundred times more SEE sensitive than the old batches and on top of it the support from Alstom is planned to phase out soon. The rights where then bought by CERN and the support and development of the new versions is provided by BE/CO. The project dedicated web space can be found here.

- The **nanoFip** development has already started and is programmed in the Actel Flash based PROASIC3 FPGA.
  - A3P250 FPGA is filled by 50% with the actual VHDL code (done by P.Alvarez) and is ready for tests
  - Test board PCB design ongoing by an external company
  - The test bench VHDL code is being written by G.Penacoba (2 months to finalize)
  - Original Alstom code seems to be practically unusable. The code was rewritten, but in order to make the design simple and therefore more robust, many functions were removed like i.e.:
    - WorldFIP messages
    - Many registers
  - Several new features were added:
    - the status is sent with the data
    - the design can be integrated with the user code
    - longer variables and wider IOs available (16bit)
    - reset with specific variable
    - no setup required

- the chip should be **ready** by **end of 2010**

- The "Dream" solution for the users would be the full functionality copy of the previous chip, pin and voltage level 100% compatible, but RadTol. The **MICFIP** project would be approaching this idea.
  - It is unclear how many clients would actually need this
  - Is the **microFIP** the only sensitive chip on the board, so the only one to be **replaced**?
  - The ASIC would be produced in IBM 130nm technology (non rad-tol specific?) and designed in cooperation with PH-ESE
  - Only 3.3V can be used, otherwise power regulator has to be used INSIDE the package
    - G. Penacoba noted that Cryo group uses 3.3V even for the fieldDrive
    - Regulator doesn't fit in the TQFP package, so PIN compatibility would be excluded
    - Reliability of an eventual adapter design not guaranteed (can be even impossible)
    - Not clear if 5V signal levels can be achieved
  - Mitigation of the SEEs can be done by:
    - Triplication at the chip level (3 copies of the same chip)
      - Regular resets of the chips will be required in order to clear the wrong states induced by SEUs
      - SET are likely not an issue as the operating frequency will be at most 2.5MHz
      - Synchronization of the chips might be challenging
    - TMR at the register level needs a full understanding of the design

  - Responsibilities for the development have to be clarified. PH/ESE could agree to the following:
    - Compile Alstom code, triplicate logic, provide simulation environment
    - Add logic that sends erroneous packets when SEU detected
    - NOT to verify if simulations are correct
    - NOT to Guarantee that the produced chip corresponds to simulation
  - Other project members would then have to:
    - Qualify design based on simulations of Alstom's test benches
    - Add other test benches to qualify
    - Adapter to package (**never done, highly risky**)
    - Verification is very time consuming
  - COST estimation
    - ~ 4 FTE (+X for TMR design)
    - ~ 1.5 MCHf
  - Items to be clarified: [**follow-up: BE/CO** who coordinates the collection of requirements]
    - Responsibilities in the project.
    - List of foreseen use cases and the attitude of the users towards the project
      - Is it necessary to use the current PCB?
      - What are the signal levels used?
      - What are the required time scales?
      - If the PCB has to be redesigned anyway, is the preferred solution micFIP or nanoFIP?
    - Detailed feasibility, manpower and cost estimation/planning missing.
    - Is the foreseen deadline in late 2012 too late for the users?

- **nanoFIP+** project
  - It could be done as an upgrade of the current nanoFIP design once the later one is validated.

- Additional features could be added in order to make it software compatible with the current designs.
  - What are the missing features required in the nanoFip+? [**follow-up: BE/CO**].

- Discussion related to the xxFip roadmap
  - CRYO (G. Penacoba): If the nanoFip is used with only 2 variables, 2 separate systems have to be maintained in parallel and only complete sectors can be replaced with the nanoFip as the event agent cannot handle both systems at the same time. If the micFIP solution is chosen the group can continue with the current spares and continuously replace with the new system
  - CO (J. Palluel): The event agent could be changed in order to handle both systems in parallel (3 and 2 variables)
  - CRYO (G. Penacoba): As users we prefer to have the "dream" solution investigated, but if only SW has to be rewritten in order to use the nanoFIP, the micFIP budget is not justified.
  - CO (J. Serrano): nanoFIP and uFIP are standard of FIP protocol. Only the front end SW has to be changed to use 2 variables. Single **segment** can handle **EITHER 2 OR 3 variables**.
  - QPS (R. Denz): If the final chip is **100% SW compatible** (from the QPS system point of view), the PCB could even be changed. It is then necessary to be absolutely sure about the full compatibility. The change of the board is far easier than the modifications in the QPS supervision system and renders the potential upgrade of the system easier as well.
  - "Another important point is the availability of the new **chip or the VHDL** code (sufficient for us). One should be aware that in order to be ready for a potential upgrade during the long shutdown in 2012 we need to have the chip or VHDL code by the end of **this year latest**."
  - Other points:
    - The dual ported RAM in the nanoFIP will be TMR protected
    - Only QPS is currently using the new version of the uFIP chips in the tunnel
    - Magnetic field problems will not be addressed as the same transformer will be used. No complaints were so far received. (problems observed by T. Wijnands in CMS)

ELMB++ development, short report – (M. Brugger):

- Meeting was held to see if a new development can/should be launched (organized by PH see link)
- presentation from Alessandro Marchioro (RadWG 9.7.09) was describing the current system
- ELMB -> Embedded Local Monitoring Board
  - radiation tolerant device
  - digital and analog I/O
  - It can distribute timing, monitor and do certain control operations
- The main question is if the possible development would be useful for the machine
  - Could it solve / improve existing installations, or help in future developments?
  - What would be the machine requirements: e.g., WordFip connectivity (currently only CAEN)
  - Is on board intelligence required?

Point iteration report approval – (G. Spiezia):

- The links to the reports of IR1,5,8 were presented and deadline for the collection of the missing information was set to 1 June

Overview of the CV equipment in the LHC underground areas with elevated radiation – (H. Jena):

- Minutes TO BE COMPLETED