# CernFIP Project

## BE-CO
## 22 April 2010

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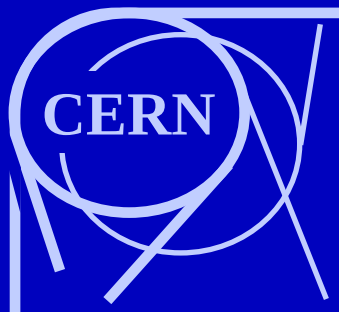
CERN




# Overview

NanoFIP overview, progress, next steps

MICFIP: migration of original MicroFIP design?

Conclusions

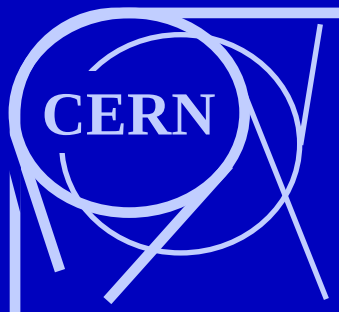
# NanoFIP Overview

## WorldFIP slave designed from the ground up

- Needed implementation in FPGA
- Code from Alstom not re-usable in the view of two engineers

## Features were defined with users

- Features removed: use KISS principle
  - Simple = more radtol
  - No experience designing WorldFIP
- Users requested additional features
  - As anyway was possible
  - Only simple ones accepted




# NanoFIP Features

## Added features to MicroFIP

- No setup required
- Status sent together with the data
- Larger variables
- Reset with specific variable
- Wider stand-alone I/O (16 bits vs 8) and simple memory interface
- VHDL code in Actel IC or can be combined with user code

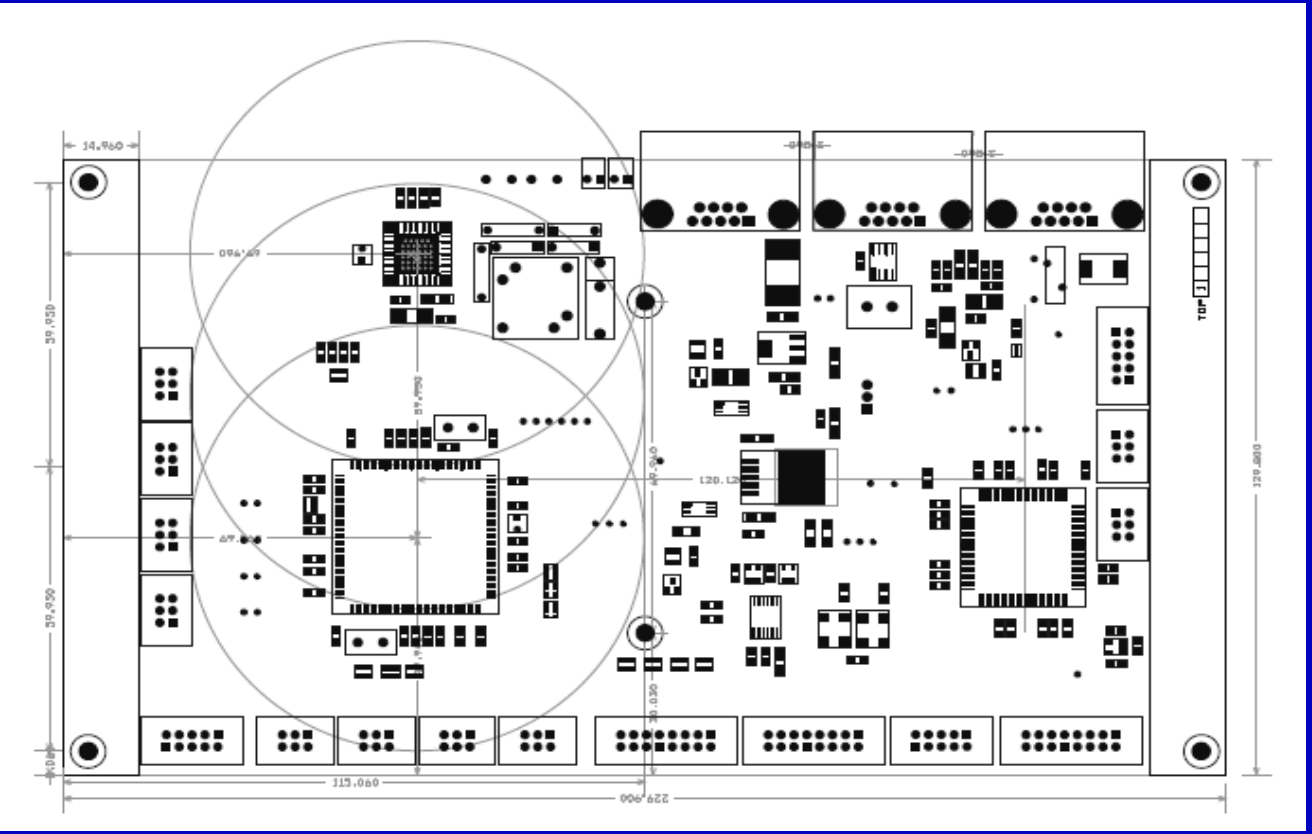
## Removed features from MicroFIP

- No WorldFIP *message* support
- Other registers

# NanoFIP Progress

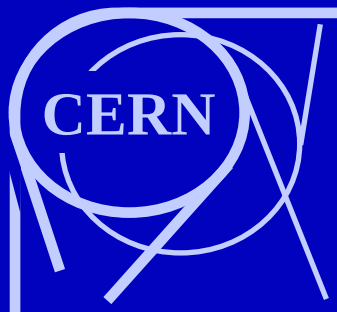
- **Specification available**
- **Implementation**
  - VHDL code written by P. Alvarez (BE/CO). 50% of A3P250
  - ready for testing and debugging on test bench
- **VHDL test bench design**
  - VHDL code being written by Gonzalo Penacoba (TE/CRG)
  - Needs 2 months of work to finalise
- **Test board design**
  - Being designed by a commercial company
  - Schematics design review held on 26 March 2010
  - PCB design underway
  - 1-2 months of work to debug NanoFIP

# NanoFIP test board



# NanoFIP
# Next Steps

- Finalise design
- Review and document VHDL code in detail
- Debug on VHDL test bench
- Debug on test board
- Radiation tests
  - Actel is known, would be checking TMR quality
- Design a real application board
- Document and make available as IP
- Support users to migrate designs




# MICFIP

# MICFIP
# - The Dream Solution -

## Having a 100% compatible chip would be good

- Boards having problems can just replace chip
- No redesign and costly production of new boards needed
- It would be 100% compatible
  - » Pin compatible
  - » Signal level compatible
  - » Power supply compatible
  - » Functional compatible

## Not clear *how many* clients would need this

- Unclear if MicroFIP is the only 'too sensitive' IC on boards
- Should request clients
  - » not asked before as compatible chip never considered

# MICFIP meeting with PH-ESE

## 29 April 2010

- **Power supply compatibility: *5V operation not possible***
  - Need to include a power regulator in package
  - Which applications use 3.3V, who 5V?
- **Pin compatibility: *not possible***
  - TQFP package cannot handle power regulator
  - Required adapter design not trivial or maybe even impossible
- **Signal levels**
  - Not clear if can make 5V level compatible
- **Radiation tolerance: need major work**
  - Triplicating full design with output voting needs regular reset
    - » is not 'self-cleaning' SEU errors
  - Triplicating on register level needs full understanding of design

# MICFIP meeting with PH-ESE
## *continued*

## Responsibility of PH-ESE

***Assumption: Alstom's code is a trusted black box* - is it really?**

- Compile Alstom code, triplicate logic, provide simulation environment
- Add logic that sends erronous packets when SEU detected
- Will *not* verify if simulations are correct
- Quarantee that produced chip corresponds to simulation

## Responsibility of *others*

- Qualify design based on simulations of Alstom's test benches
- Add other test benches to qualify
- Adapter to package (never done, highly risky)

# MICFIP meeting with PH-ESE
## *cost estimation*

| | | |
|---|---|---|
| Logic design | 6 months for 2 people | PH |
| | X months if need TMR | PH |
| Other design | 6 months for 2 people (I/O, reg) | PH |
| Verification | 12 months for 2 people | ? |
| Package design | 12 months for 1 person | ? |

| | |
|---|---|
| Total: 4 person year (+X) (resources not available) | 600 KCHF |
| 5000 chips | 400 KCHF |
| Adapter package | 150 KCHF? |
| Package proto, TMR design | xxx |

# MICFIP migration Risks

- Responsibility not clear
- Total manpower effort not understood
- Costs not yet well calculated
- Risk of introducing new features when TMR
  - breaking up original idea of simple re-use of code
- Designed chip may not work
  - Not pin-compatible, adapter may not be reliable (if possible at all)
  - Signal level compatibility. Loose 5V I/O signal level
  - Design errors not catched in testbench...
- Radiation tests may conclude negative

# CernFIP project next possible steps

## NanoFIP

- Continue development and test
- Should be ready by end of 2010

## NanoFIP+

- Add features to NanoFIP
  - » make it software compatible (message support, addressing)

## MICFIP

- Responsibility for development should be very clear
- Find use cases and user's feeling about this solution
- Needs investigations on cost, compatibility (signal levels, power requirements, pins), TMR possibility *and risks (e.g. costly respin)*
- Precisely estimate total time and cost, roughly 1.5 MCHF
- Planning: late 2012 earliest

# Conclusions

## NanoFIP design progressing

- Slowly but steadily
- Makes that CERN understands fully the technology

## Once understand, have a path to the future

- Add message support, more compatibility etc.

## Unclear what to do with new option of migration of original Alstom design

- What are the use cases?
- What is the total cost
- are the risks acceptable?

# Need to know

**If you want to keep using current PCB:**

- What supply voltage used in your design?
- What signal level used in your design?
- What are your timescales?

**Would you use NanoFIP or MICFIP if you need to redesign your PCB?**

**What features would you need in NanoFIP+?**

**What is your planning anyway?**