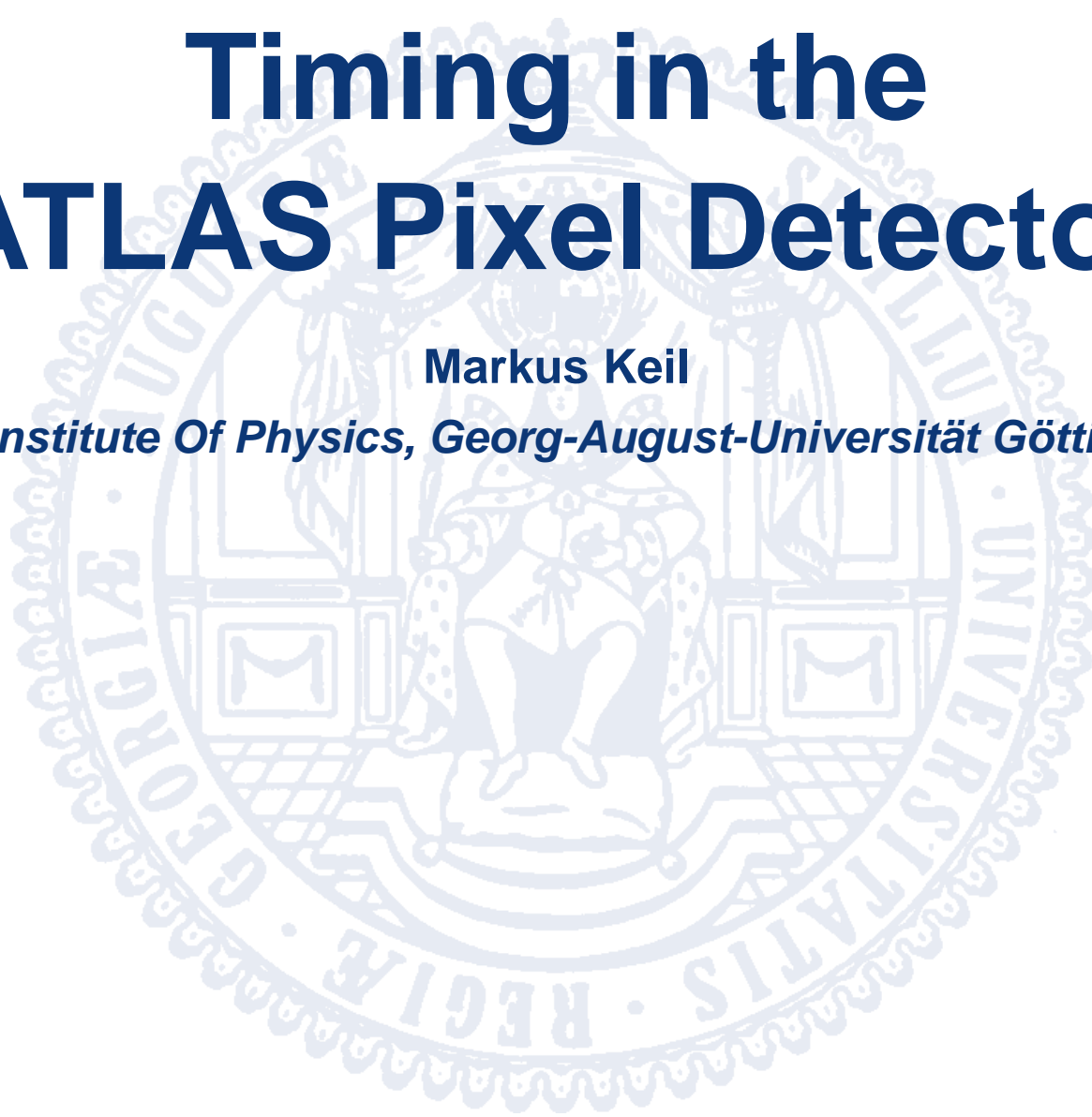# Timing in the ATLAS Pixel Detector
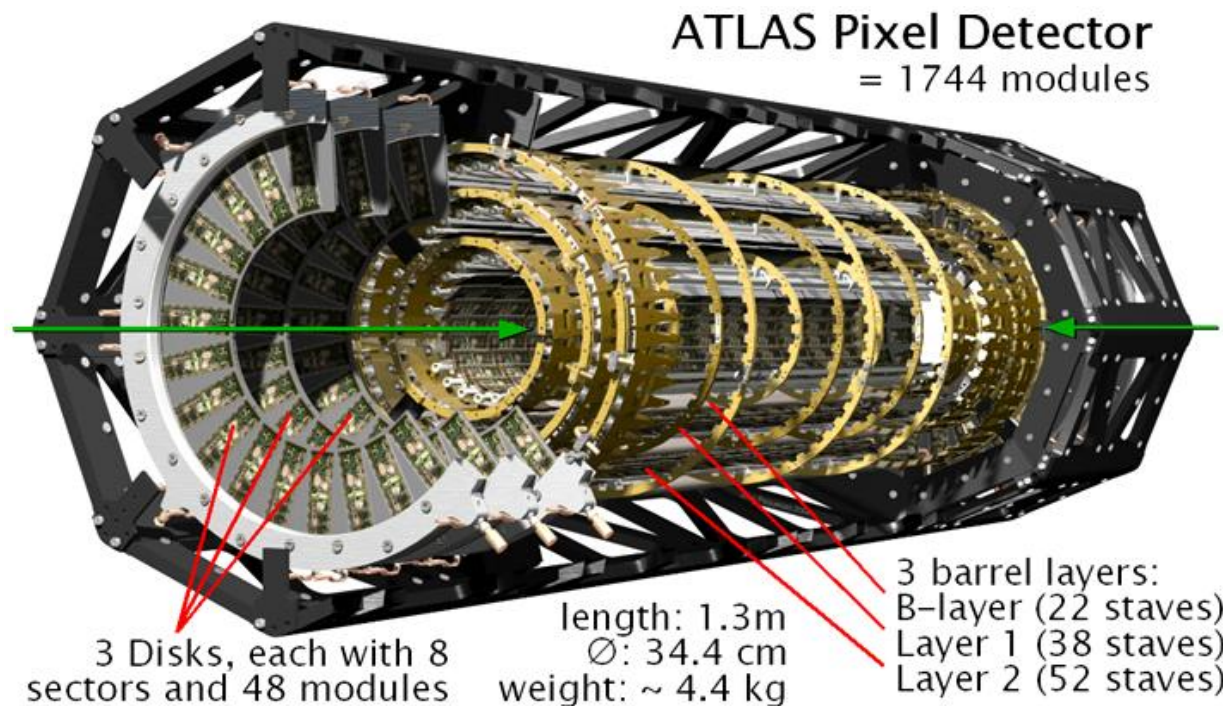
Markus Keil

2nd Institute Of Physics, Georg-August-Universität Göttingen

ATLAS Pixel Detector = 1744 modules

3 Disks, each with 8 sectors and 48 modules

length: 1.3m
Ø: 34.4 cm
weight: ~ 4.4 kg

3 barrel layers:
B–layer (22 staves)
Layer 1 (38 staves)
Layer 2 (52 staves)

- **The ATLAS Pixel Detector**
    - The FE Chip: Readout Architecture and Pixel Cell
    - Global Readout Architecture
- **Timewalk**
- **Limitations and Improvements**

The ATLAS Pixel Module

- ## Pixel Sensor:
  - active area 6.08 x 1.64 cm2
  - thickness 250 µm
  - n+ (pixels) on n (bulk) with p+ backplane
  - typically 400 µm x 50 µm pixels
 - operation bias voltage 150 – 600 V

- ## Module Readout:
  - 16 FE chips,
    in total 46080 readout channels
  - energy measured as Time-over-Threshold (1 ToT = 25 ns)
  - MCC chip builds local event
  - up to 160 MHz data transfer

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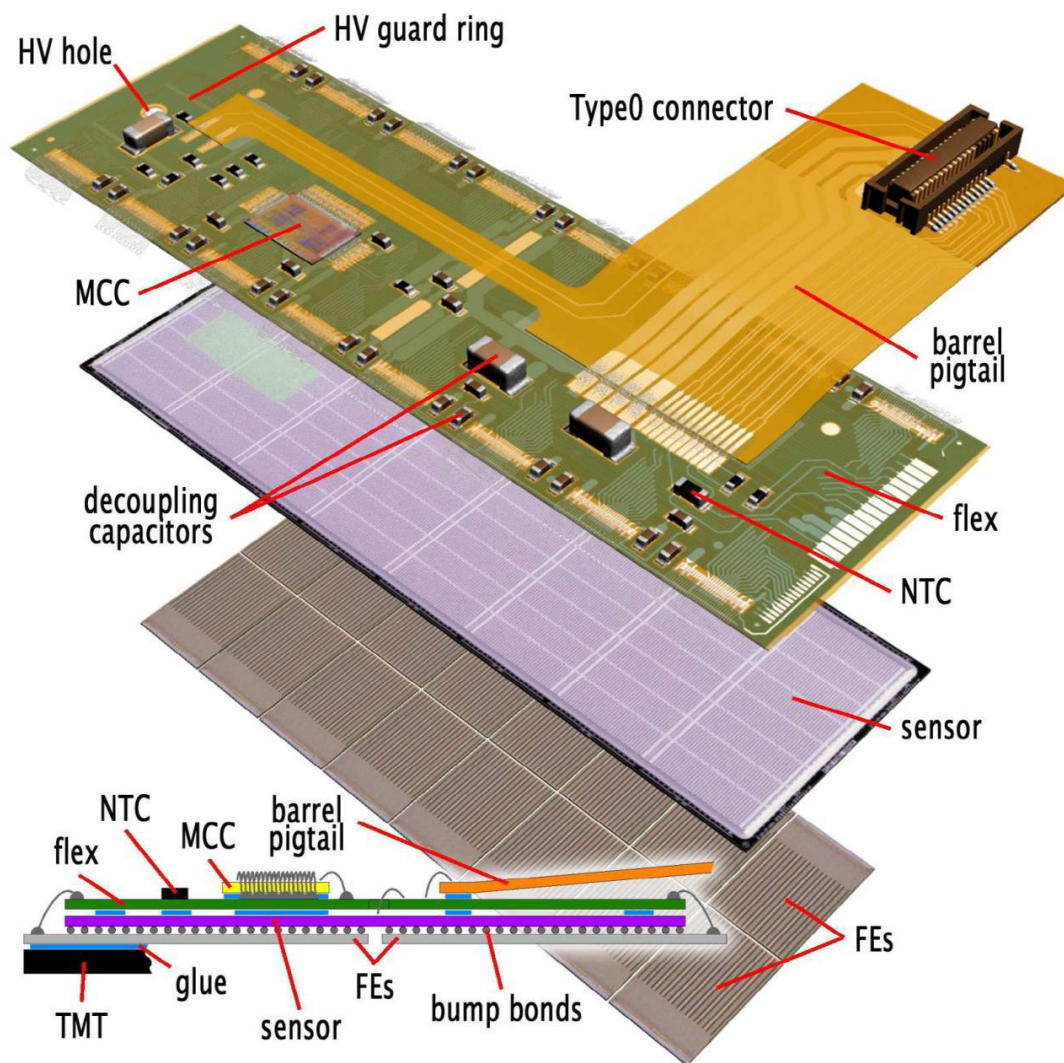
- Each FE chip contains:

  - A matrix of 2880 pixels

  - An end-of-column logic with hit buffers

- In each pixel:

  - Zero suppression

  - Time stamping

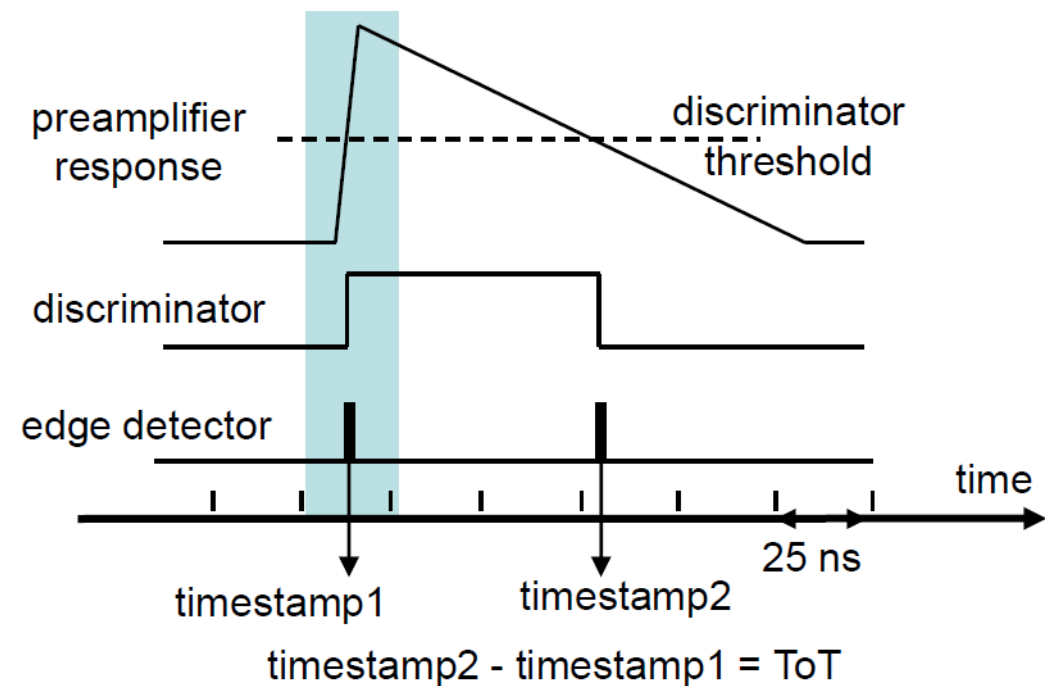- In the EOC logic:

  - Hit storage

  - Trigger coincidence

  - …
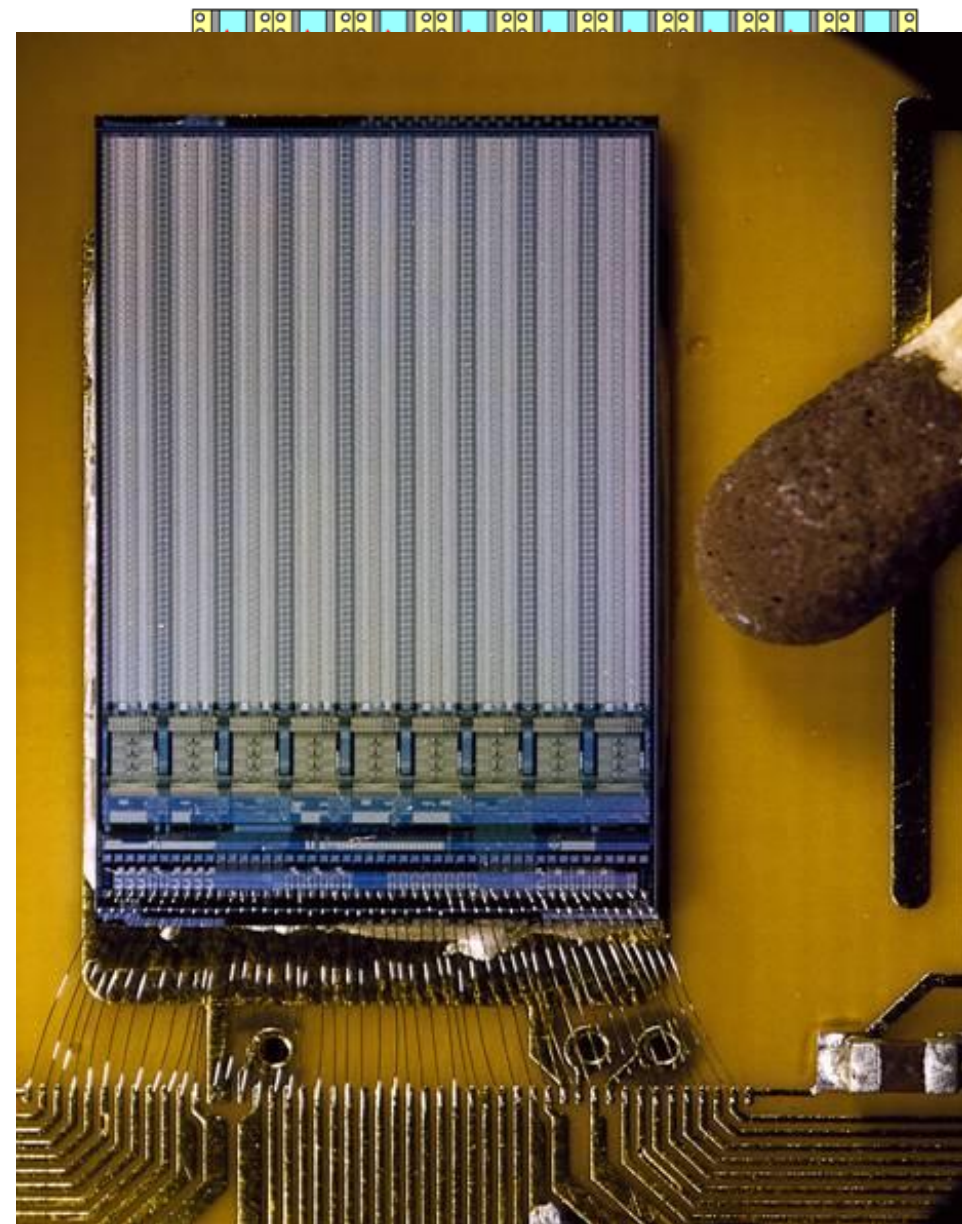
Data output   L1   Power supplies

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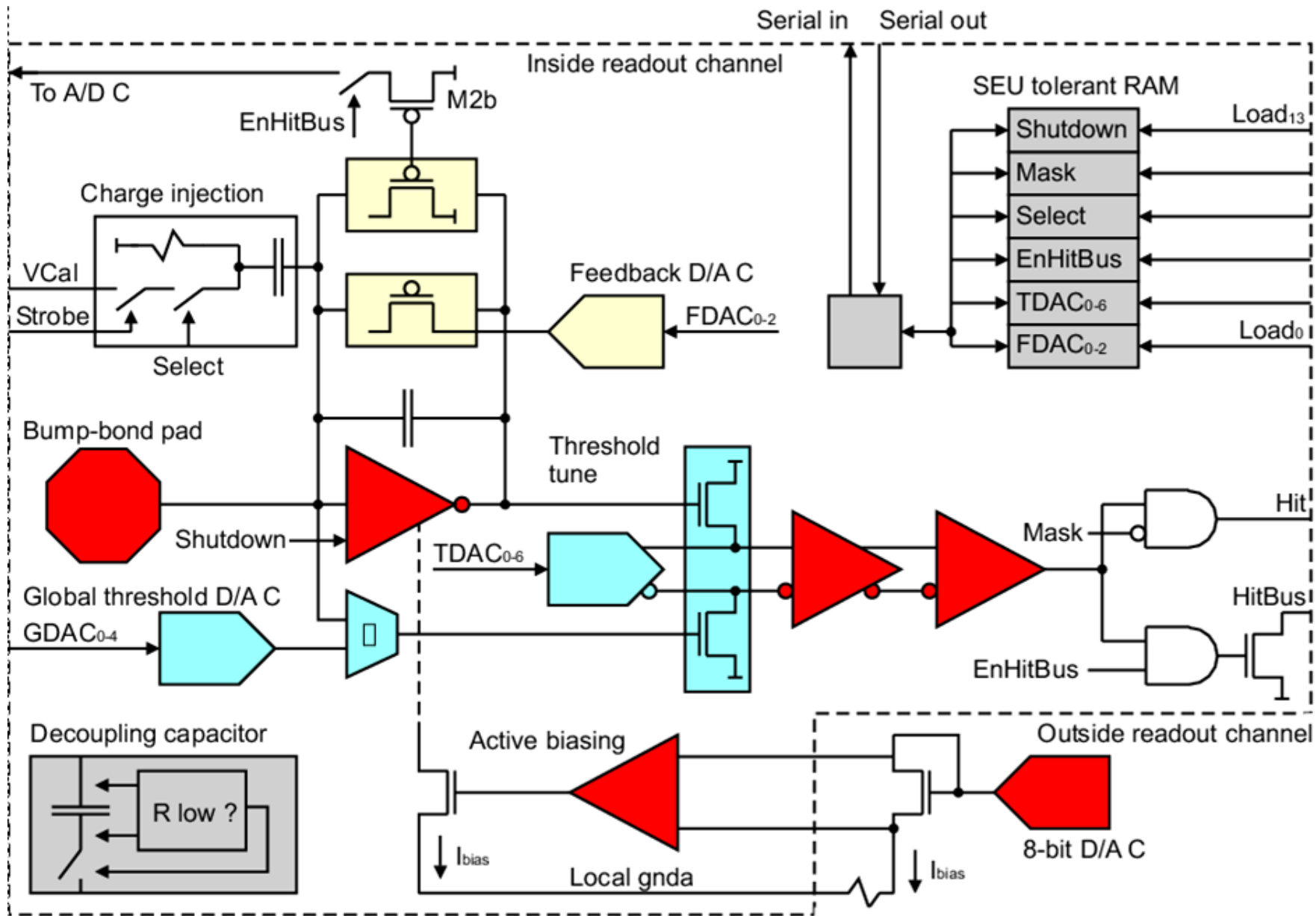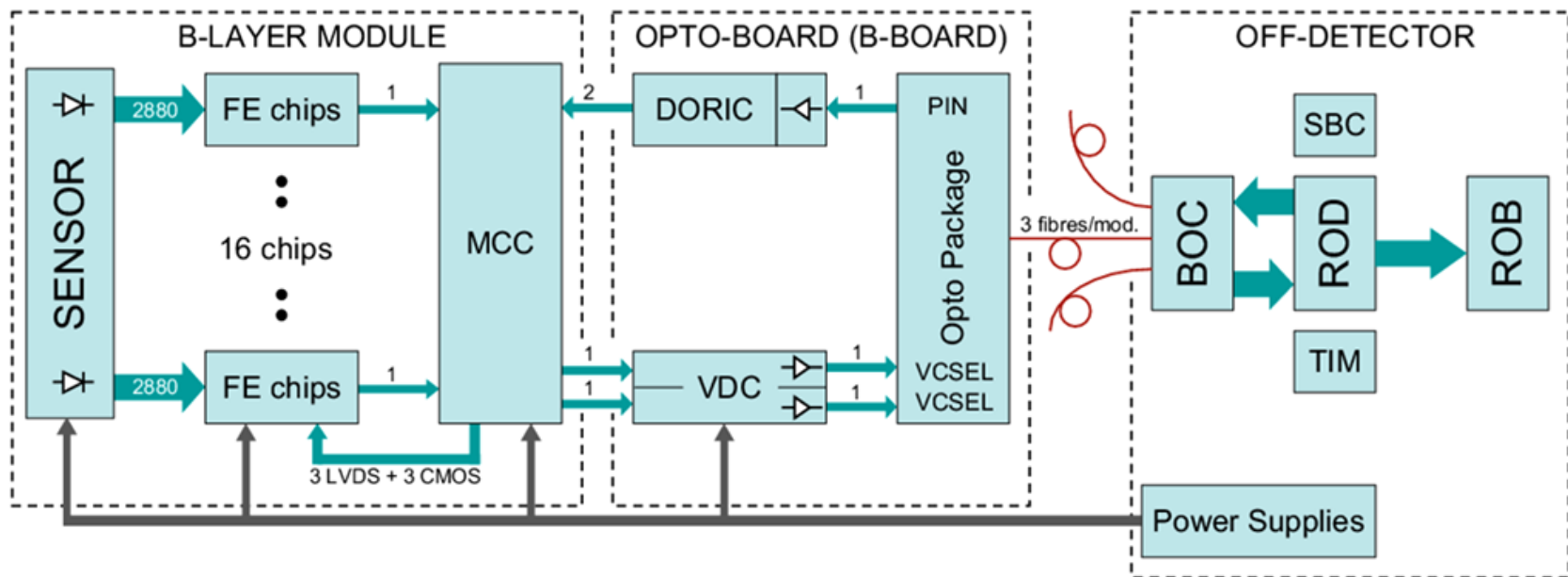
- Timestamp is distributed in the pixel matrix

- In case of a hit, the hit pixel saves the current time stamp into a RAM cell

- The hit is then transferred to the end-of-column buffers

- If after the programmable trigger latency a trigger arrives, the hit is sent out of the FE chip, erased otherwise

- (Saving of the trailing edge timestamp allows calculation of the Time over Threshold)

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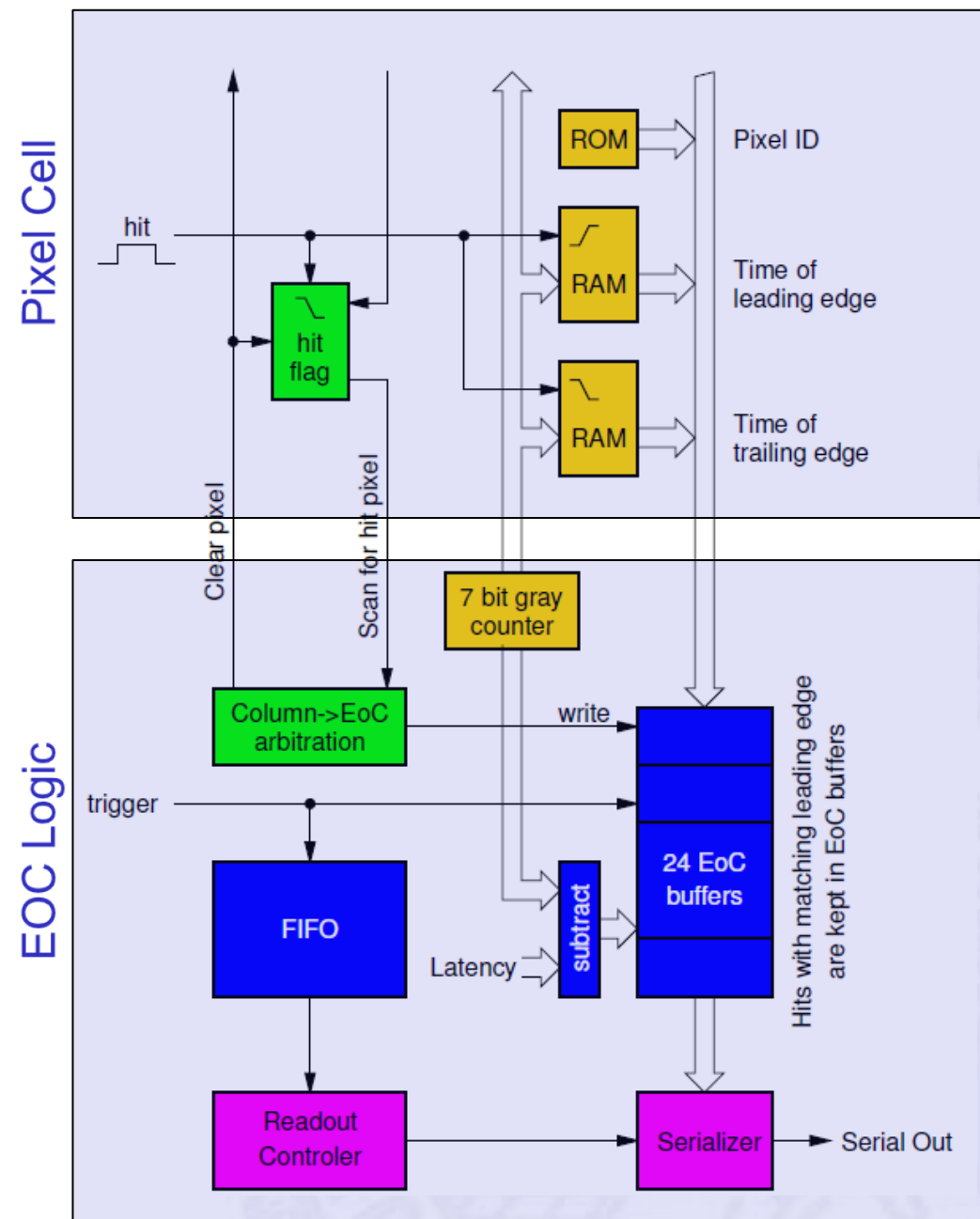
- The only timing information for the pixel hits are the leading and trailing edge timestamps

- The timestamps are generated from the 40 MHz module clock which is sourced from the LHC clock

- Leading edge information is used for trigger coincidence, trailing edge gives ToT and therewith amplitude information

preamplifier response — discriminator threshold

discriminator

edge detector

time

25 ns

timestamp1   timestamp2
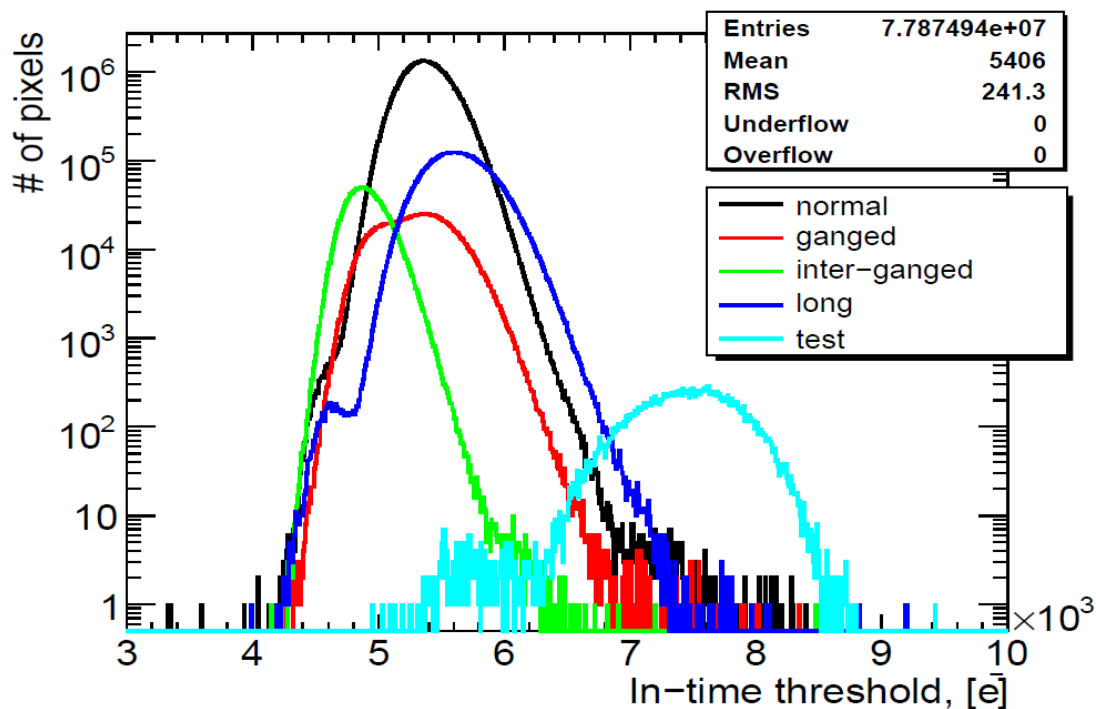
timestamp2 - timestamp1 = ToT

- Clock and commands (in particular trigger commands) are sent via optical fibres to the modules (1 fibre per module)

- A sub-ns delay can be added to each channel to account for all timing variations (crate-to-crate variations, fibre and cable lengths, time of flight)

- In case of a trigger the module controller chip (MCC) sends between 1 and 16 consecutive triggers to all FE chips of the module (25 ns – 400 ns readout gate)

- Timewalk: large charges are detected faster than small charges

- (For ATLAS) this is critical if timewalk exceeds 25 (20*) ns and the hit gets the timestamp of the next BC

- Definition of intime threshold: smallest charge that is detected "in time"

* We foresee to set the delays such that large charges are detected 5 ns after the beginning of the BC (to account for jitters, pixel-to-pixel variations etc.)
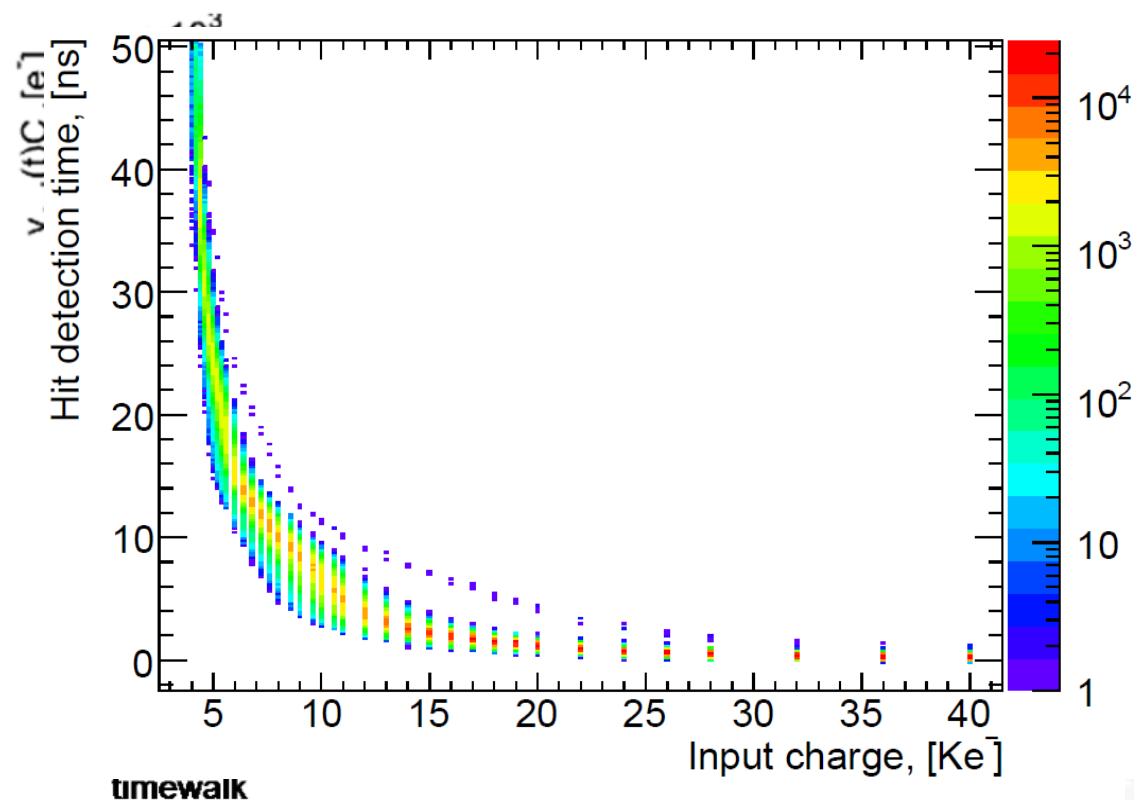
- **Measurement of the in-time threshold at a discriminator threshold of 4000 e**

- **Timewalk adds another ~1400 e of overdrive on top of the discr. threshold to detect the particle in time**

- **On-chip correction mechanism to improve this (see below)**

Entries	7.787494e+07
Mean	5406
RMS	241.3
Underflow	0
Overflow	0

— normal
— ganged
— inter-ganged
— long
— test

# of pixels

In-time threshold, [e]

- Calibration measurement of the turn-on time for large charges (100 ke) for all pixels in the detector

- All pixels fall within a 4 ns window

- Timing corresponds to timing foreseen for beam operation: large charges are detected on av. 5 ns after the beginning of the BC.
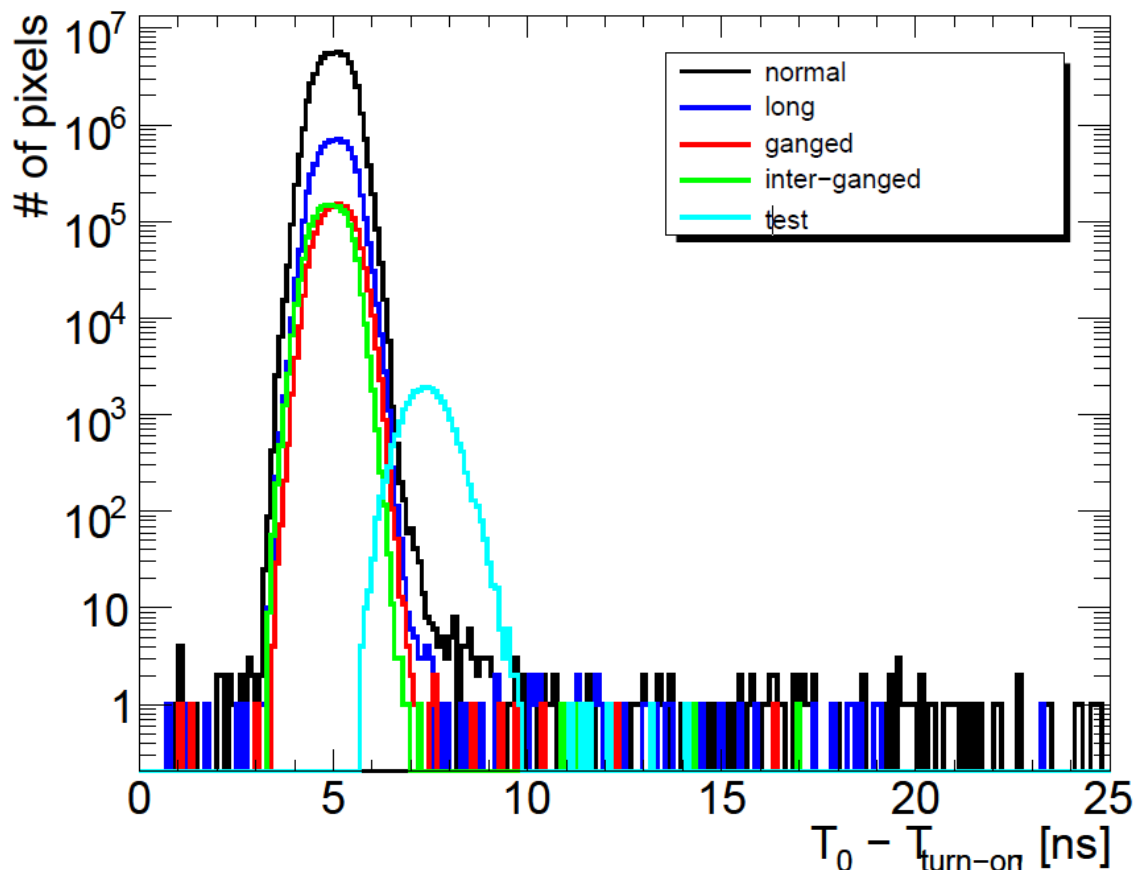
Improving the time resolution in view of CLIC (without complete re-design) ...

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- Two main limitations for timing:

  - 25 ns binning of the readout

  - Timewalk

- Possibilities <u>not</u> discussed in the following:

  - Major redesigns of the FE chip
    (e.g. The analogue pixel cell)

  - Change of the operation parameters
    (Can improve timewalk, but increases the power)

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- By construction the highest time resolution achievable with the ATLAS Pixel Chip is the clock cycle (in ATLAS 25 ns)

- Possible Improvement 1: Increase clock speed

  – Problems: Room for improvement limited, removes margin for radiation damage

- Possible Improvement 2: Add in-pixel TDC

  – Easily possible to add a TDC in each pixel cell, measuring the phase between each hit and the following clock edge, thus giving the exact position of each hit *within* the clock cycle

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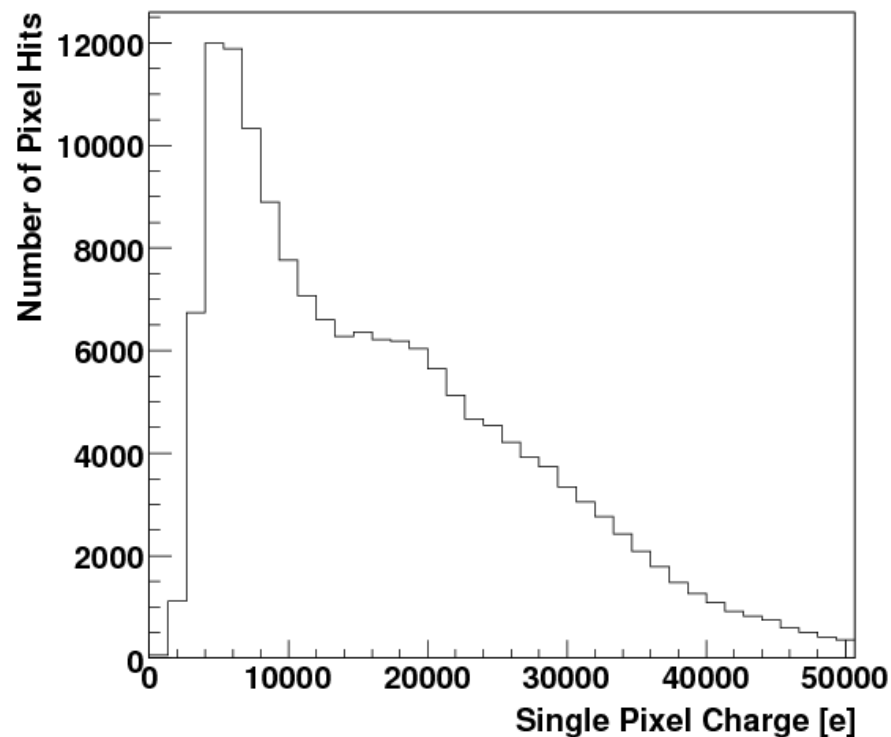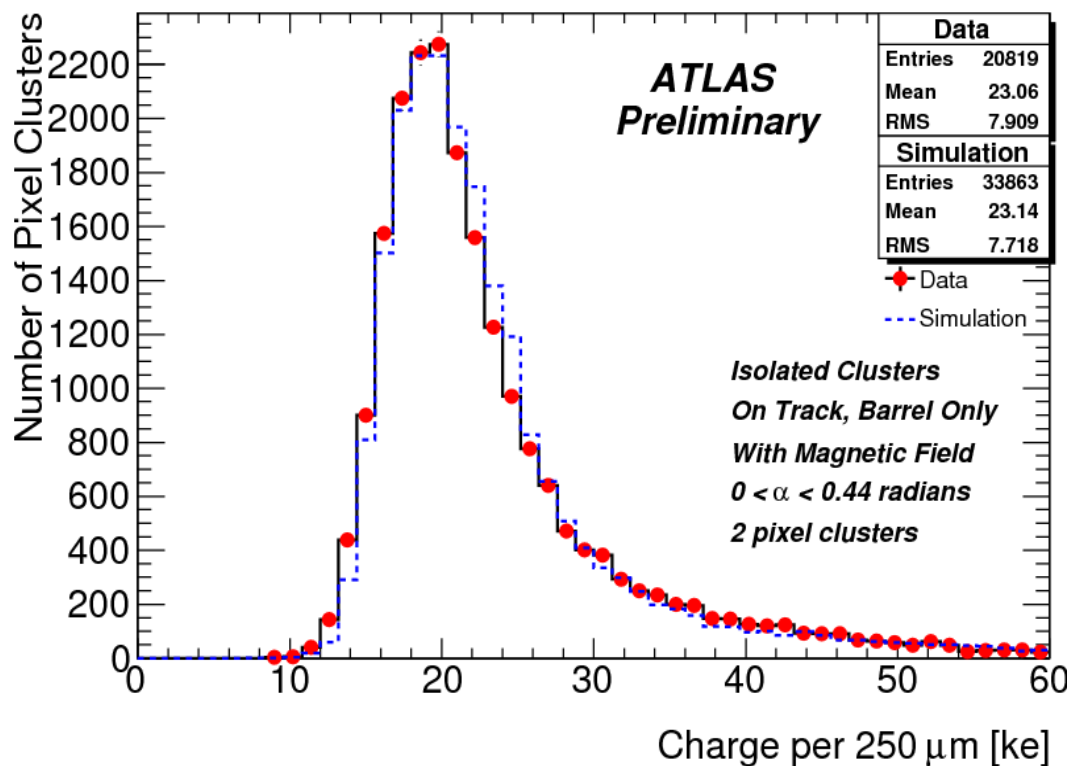
- Deposited charge relatively high with respect to the threshold (3500 e – 4000 e)

- But: Threshold is applied to charge collected in single pixels → much smaller

- Effect will be more important for smaller pixels (and thinner sensors...)

- (Both plots show charge calculated from ToT: left after, right before clustering)
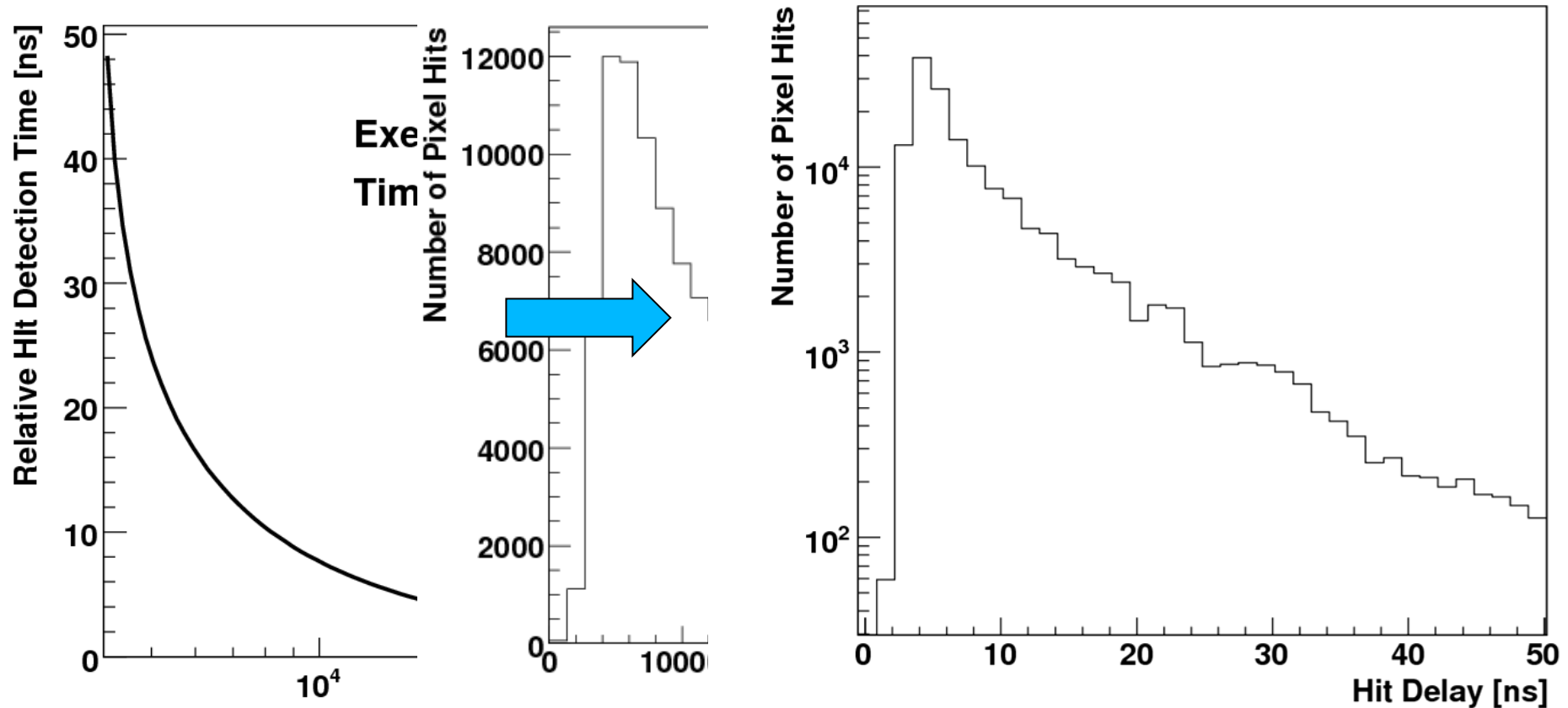
- Apply exemplary timewalk curve to distribution of single pixel charge

- Timewalk needs to be addressed when going below 25 ns time resolution

- Distribution will be flatter (worse) for more charge sharing

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- **Improvement 1: Hardware**
  (Already implemented and used in ATLAS Pixel Chip)

  – If ToT is below a (configurable) threshold, assume that the hit suffered timewalk > 1 clock cycle

  – Write hit twice: Once in the original clock cycle (BC), once one BC earlier

  – Advantage: Hits can be recovered without enlarging the readout gate

  – Second threshold allows to remove hits from the original BC (to not increase number of "noise" hits due to hit doubling)

  – Allows to completely remove effect of timewalk (on the scale of 25 ns), but second threshold has to be chosen carefully to reduce occupancy

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- Improvement 2:

  - Enlarge readout gate
    (i.e. Read out more than 1 BC)

  - Do calibration measurement
    timewalk vs. ToT

  - Correct the hit time offline

  - Simulations done in a summer
    student project (L. Gonella, M. Keil,
    2005) suggest that if using the offline
    correction in connection with a TDC
    information the time resolution can
    be improved well below 10 ns.

  - Disadvantages: Higher data rate,
    need for careful offline calibration

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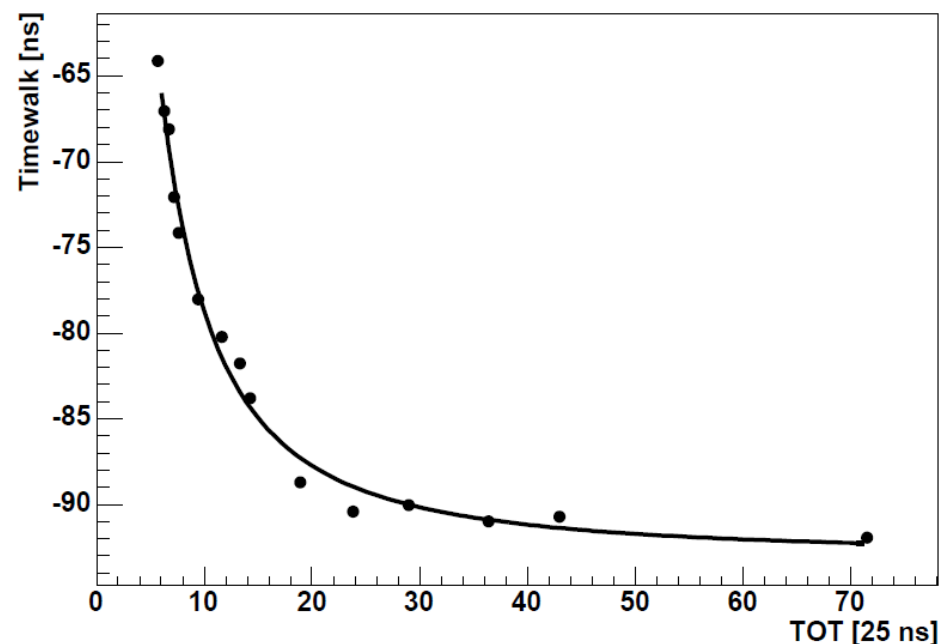
- The requirement for ATLAS is to detect charges within 25 ns

- The main ingredients to address these requirements are:

  - An analogue FE with sufficiently low timewalk + an on-chip timewalk correction

  - A 40 MHz readout

  - A per-module fine delay to absorb all timing differences *between* the modules

- Possibilities to improve the time resolution would involve:

  - A finer time stamp, probably sub-clock-cycle by adding an in-pixel TDC

  - A different analogue cell or an (offline) timewalk correction

  - However: this will not necessarily be enough with smaller charges and more charge sharing

- Backup ...
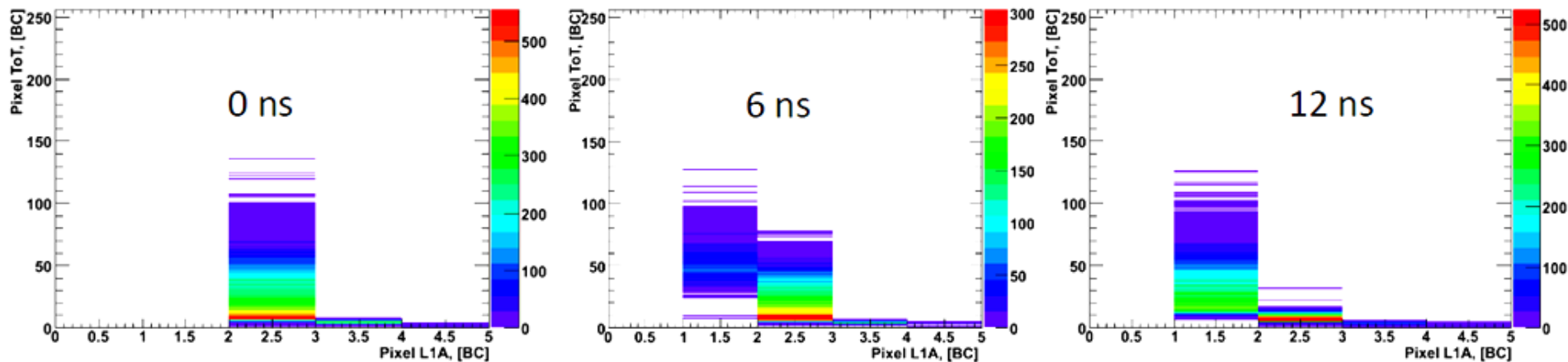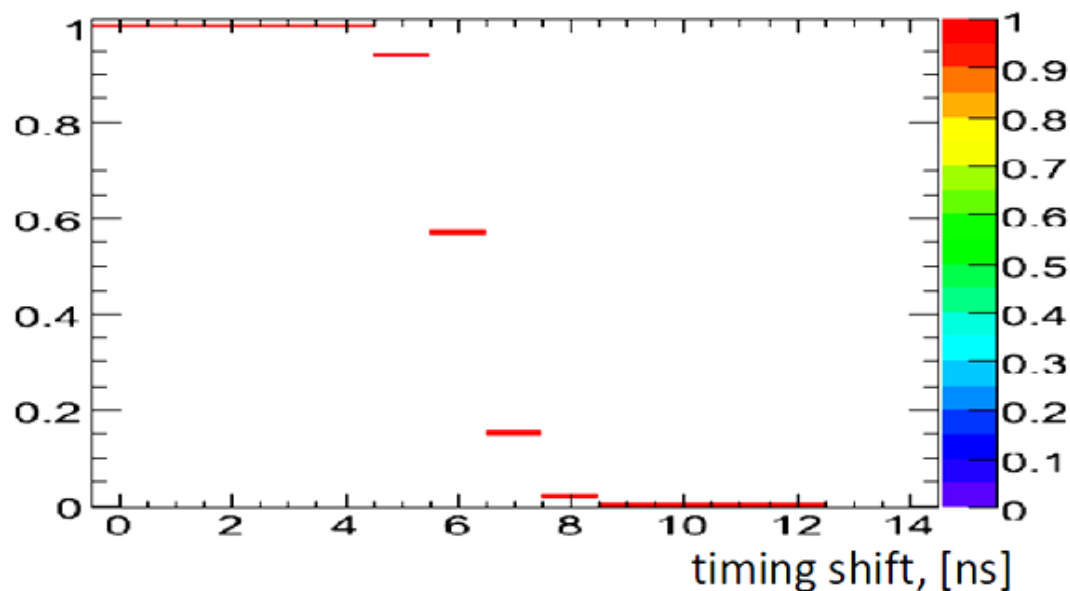
- Delay scan with collision data allows exact measurement of the single-module timing