## Description

The FastIC chip reads the signal delivered by the sensor and processes it in a current mode method. A block diagram is shown in Figure 1. The architecture is based on the HRflexToT chip [2].

The input stage generates three replicas of the incoming signal, the weight of each replica being different. The first replica, with the highest weight, corresponds to the timing signal that is sent to a fast current discriminator which compares the signal with a programmable threshold. This programmable threshold can be set at level below the charge delivered from the sensor when a single photoelectron is detected. The leading edge of the signal at the comparator output retains the information of the time of arrival of the detected particle. The chip can be programmed to output this signal for each channel. It also outputs a fast-OR combining the timing signals of all the channels.

The second replica is processed by some circuitry in order to measure the deposited energy in the sensor. The processing chain contains a transimpedance amplifier, a shaper (with a selectable peaking time, the nominal being ~25ns-50ns), a peak detector and hold (PDH) and a discriminator that compares the output of the PDH with a ramp. The time duration of the digital pulse at the output of this discriminator is proportional to the charge delivered by the sensor.

The third replica is the trigger signal. Two trigger signals can be generated. The Low Level Trigger and the Cluster Level Trigger. The Low Level Trigger is the OR of the output of the comparators of the trigger channels and the Cluster Level Trigger compares the sum of the signals deposited in all the channels in a chip with a selectable threshold. These trigger signals can be used to start the ramp generator for the energy to time conversion. The fast timing OR and a pulse externally fed into the chip can also be used for this purpose.

At the output of the time and energy processing branches, the channel can be programmed to provide 1. The Time-Of-Arrival information only, the Time over Threshold information or a combination of the two. In the latter case, the channel generates two pulses for an incoming input signal. The first pulse's rising edge contains the information of the ToA and the second pulse's width contains the information on the linear Energy measurement.

The output driver can be programmed either in CMOS single-ended or differential SLVS. There is also the possibility to monitor internal signals (e.g. the output of the transimpedance amplifier, the shaper or the PDH, as can be seen in Figure 1. The input stage can be programmed to work in both positive or negative polarity. It is also possible to combine 4 channels and sum their signals at the input stage's output. This active summation functionality is integrated to explore the impact of segmenting large SiPMs (with large capacitance) into smaller ones to achieve lower jitter while covering large detector areas. The expected performance of the chip is presented in Table 1.

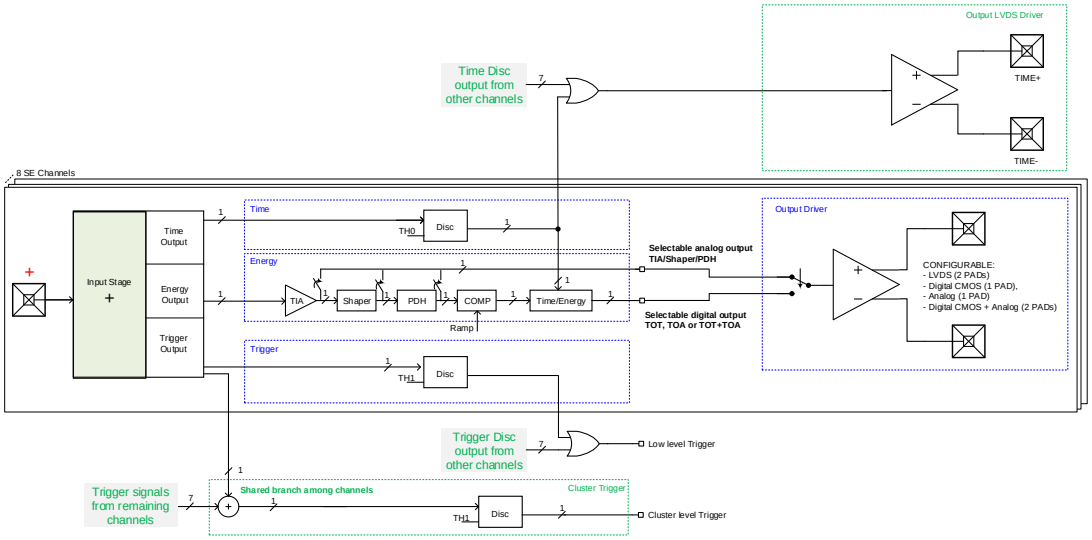



*Figure 1. Block diagram of the FastIC ASIC channel when programmed in a single ended architecture. The Input Stage, the Time, Energy and Trigger channels and the Output driver are shown.*

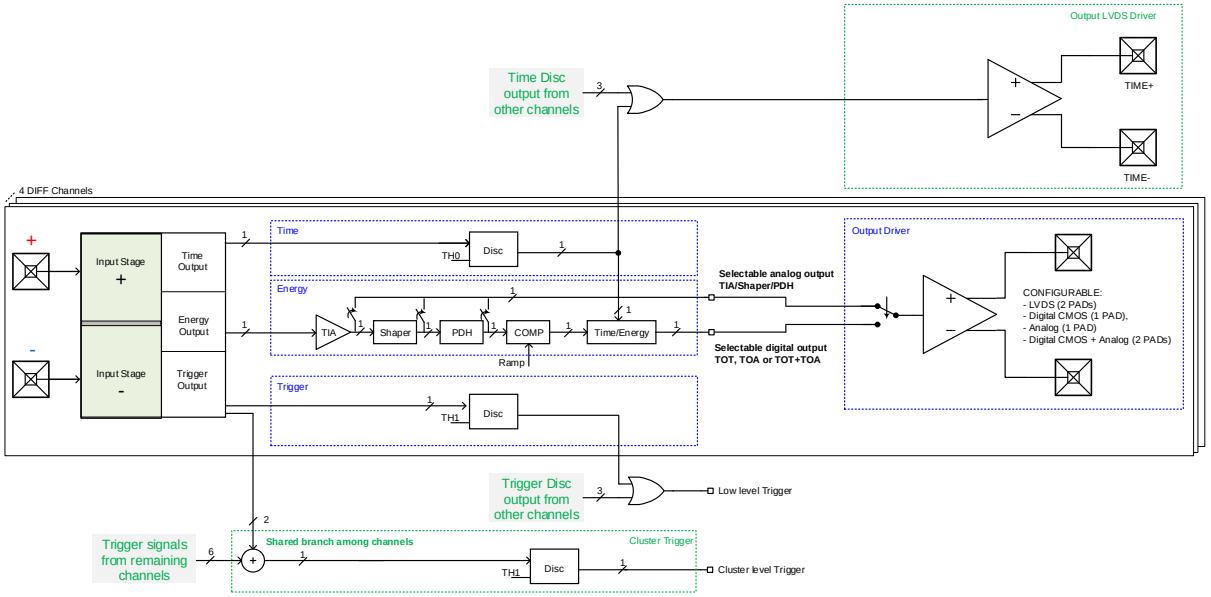



*Figure 2. Block diagram of the FastIC ASIC channel when programmed in a differential architecture.*

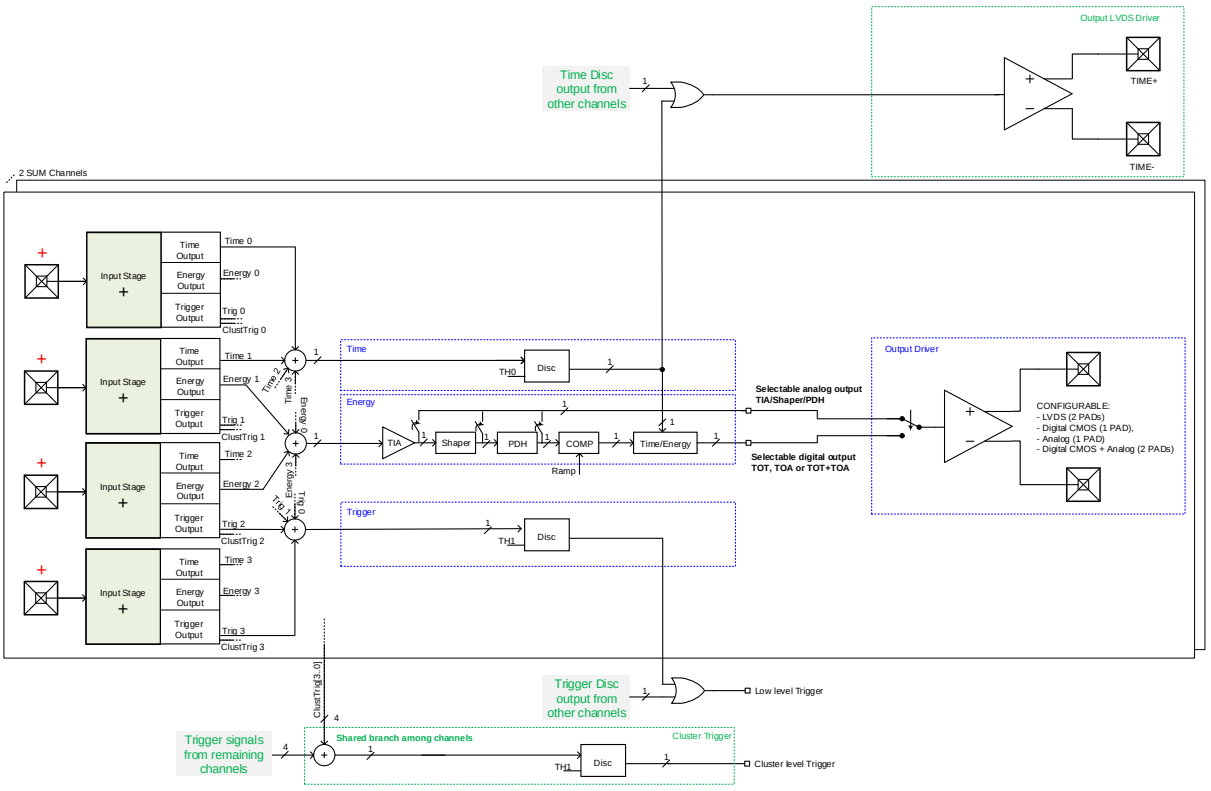


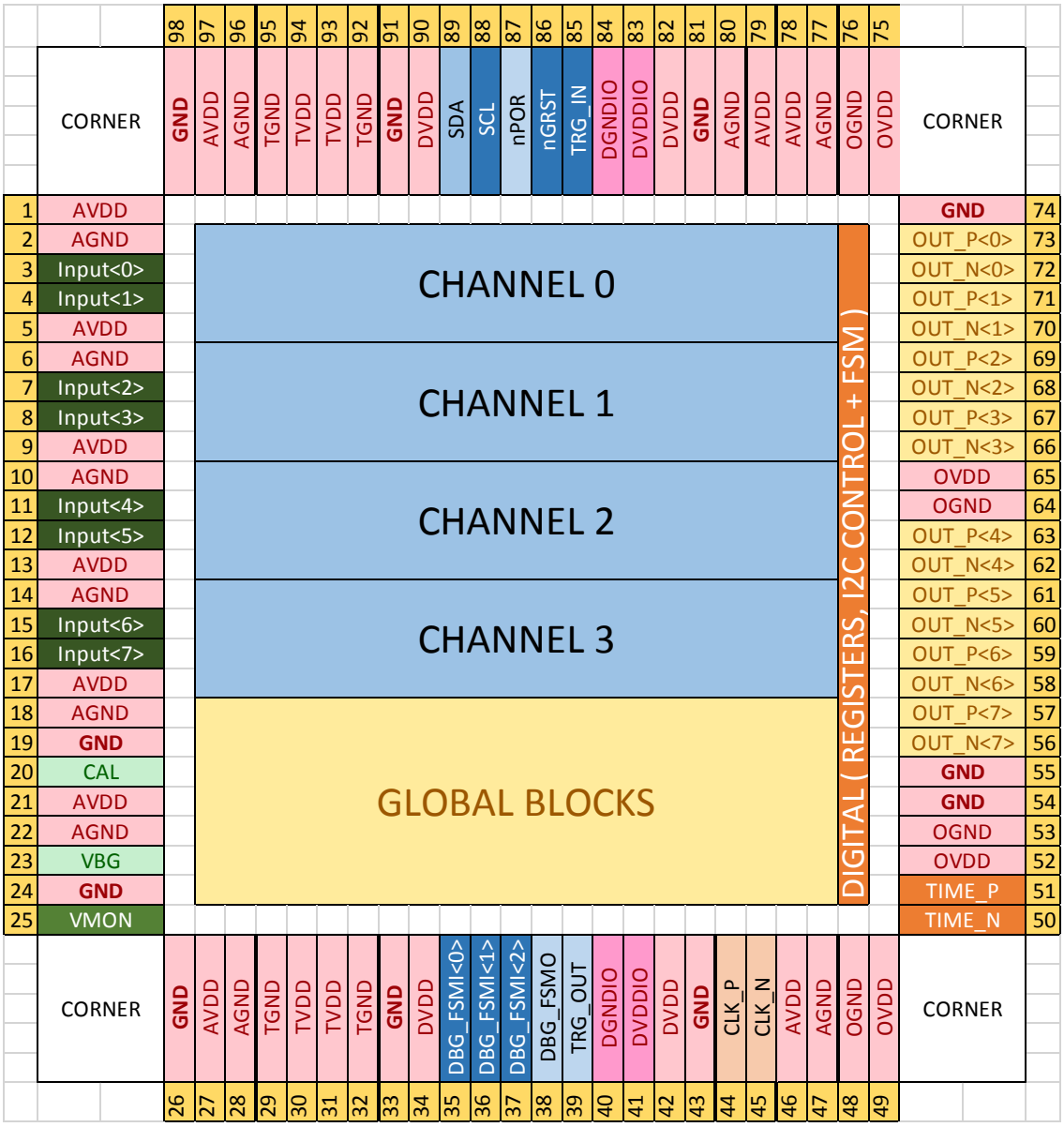

*Figure 3. Block diagram of the FastIC ASIC channel when programmed to actively sum the signals in 4 channels.*

*Table 1. Expected FastIC chip performance.*

| Parameter | Value |
|---|---|
| **Technology** | 65 nm CMOS |
| **Power consumption** | ~ 6 mW/ch in SE mode ($V_{DD}$ = 1.2 V), depends on operation mode (~ 3 mW/Input Stage) |
| **Number of channels** | 8 SE / 4 DIFF |

| | |
|---|---|
| **Connection Type** | Configurable SE (Pos/Neg polarity), DIFF, Sum of 4 (Pos/Neg polarity) |
| **Electronics Time Jitter** | ~ 25 $ps_{rms}$ SPTR (330 pF 3x3 SiPM, LCT5 S13360 SiPM, Vov = 4.5 V, L = 1.2 nH) |
| **Energy Resolution** | Linear (~ 2.5 % Linearity error) |
| **Dynamic Range** | 5 uA - 20 mA |
| **Maximum Rate** | ~ 2 MHz (Linear ToT readout), > 50 MHz (Non-linear ToT. Pulse-shape-dependent) |
| **Testing and Calibration** | Yes |
| **Interface** | I2C (compatible with picoTDC) |
| **Output** | Configurable Digital (single-ended CMOS or differential SLVS) or Analog output (10 pF load). |

## FastIC chip diagram



## FastIC chip pin list

| PIN NO. | NAME | TYPE | DESCRIPTION |
|---|---|---|---|
| **3, 4, 7, 8, 11, 12, 15, 16** | Input<0:7> | Analog input | Analog Input channels 0 and 1. When processing differential signals Input<0> is the positive polarity input and Input<1> is the negative polarity input |
| **56 TO 63, 66 TO 73** | OUT_P<0 to 7><br>OUT_N<0 to 7> | Output | Energy/Time Output Channels <0 to 7>. Configurable: CMOS single ended output, SLVS differential output, analog output for monitoring energy channel |
| **19, 24, 26, 33, 43, 54, 55, 74, 81, 91, 98** | GND | Power | Ground (chip substrate) |
| **2, 6, 10, 14, 18, 22, 28, 47, 77, 80, 96** | AGND | Power | Analog ground |
| **29, 32, 92, 95** | TGND | Power | Ground for the circuits setting the threshold |
| **40, 84** | DGNDIO | Power | Digital ground IO (clock domain) |
| **48, 53, 64, 76** | OGND | Power | Output driver ground |
| **1, 5, 9, 13, 17, 21, 27, 46, 78, 79, 97** | AVDD | Power | Analog power supply voltage (1.2V) |
| **30, 31, 93, 94** | TVDD | Power | Analog power supply for the circuits setting the threshold (1.2V) |
| **34, 42, 82, 90** | DVDD | Power | Power supply digital (1.2V) |
| **41, 83** | DVDDIO | Power | Power supply digital (1.2V) |
| **49, 52, 65, 75** | OVDD | Power | Power supply output driver (1.2V) |
| **20** | CAL | Analog | Calibration signal. Voltage signal that gets converter into a current through an internal ~70Ω resistance |
| **23** | VBG | Analog | Voltage reference of the chip. Value fixed to ~214mV |
| **25** | VMON | Analog | Output signal to monitor DC internal voltages |
| **35, 36, 37** | DBG_FSMI<0:2> | Digital Input | Debug signal to control the FSM (Input). Can be used to program the address of the chip for the I2C bus. |
| **38** | DBG_FSMO | Digital Output | Debug signal to control the FSM (Output) |
| **39** | TRG_OUT | Digital Output | Trigger Output signal |
| **44, 45** | CLK_P, CLK_N | Digital In | Differential input clock |
| **50, 51** | TIME_P,<br>TIME_N | Digital Out | Differential Timing Fast-OR signal |
| **85** | TRG_IN | Digital In | External trigger for energy measurement |
| **86** | nGRST | Digital In | Reset signal |
| **87** | nPOR | Digital Out | Power on Reset output signal, connected externally to nGRST |
| **88** | SCL | Digital I/O | I2C Clock Line (Open drain $R_{INTERNAL}$=40kΩ) An external resistor can be put externally to increase the data rate of the I2C bus. |
| **89** | SDA | Digital I/O | I2C Data Line (Open drain $R_{INTERNAL}$=40kΩ) An external resistor can be put externally to increase the data rate of the I2C bus. |

**SLVS Transmitter**

| Parameter | Description | Min | Nom | Max | Units |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage range | 1.08 | 1.2 | 1.32 | V |
| $V_{CMTX}$ | Common-mode voltage[A,B] | 430 | 600 | 770 | mV |
| $\lvert\Delta_{VCMTX(1,0)}\rvert$ | VCMTX mismatch when output is Differential-1 or Differential-0 | | | 5 | mV |
| $\lvert V_{OD}\rvert$ | Differential voltage[B,C] | 140 | 200 | 270 | mV |
| $\lvert\Delta V_{OD}\rvert$ | VOD mismatch when output is Differential-1 or Differential-0 | | | 10 | mV |
| $V_{OH}$ | Single-ended output high voltage[B] | | 700 | 900 | mV |
| $V_{OL}$ | Single-ended output low voltage[B] | 300 | 500 | | mV |
| $I_{MOD}$ | Modulation output current [D] | 0.7 | 0.8 to 4 | 5.4 | mA |
| $Z_L$ | Load impedance | | 100 | | Ω |

[A] Common mode: $(V_{DP} + V_{DN}) / 2$.
[B] Value when driving into differential load impedance 100 Ω. Termination load is external.
[C] Differential voltage: $V_{DP} - V_{DN}$, values for 2mA setting, scales accordingly for other currents.
[D] Modulation current is programmable in 0.8 mA steps from 0.8 mA to 4 mA. Default setting could be 2mA.

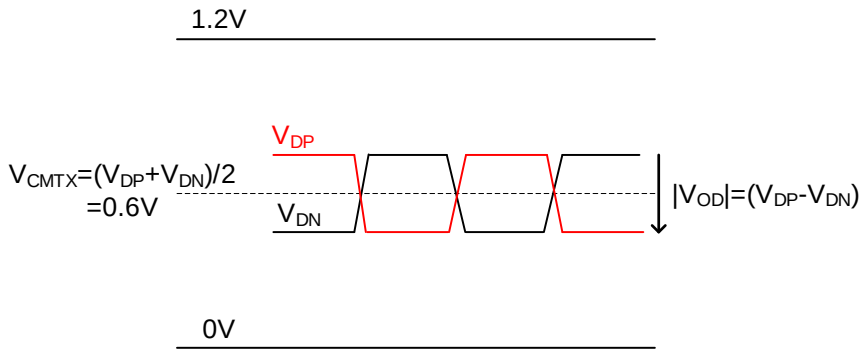



*Figure 4. Voltage definition for SLVS transmitter.*

**Reset Connection Scheme**

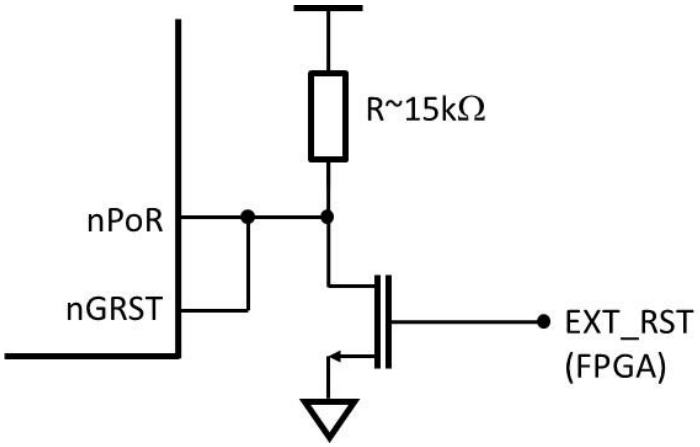



*Figure 5. Scheme to connect the Reset in the chip.*