The Abdus Salam
International Centre
for Theoretical Physics

Multidisciplinary Laboratory

MSADC
2Ch (continuous) and
16Ch (triggered) System
ICTP

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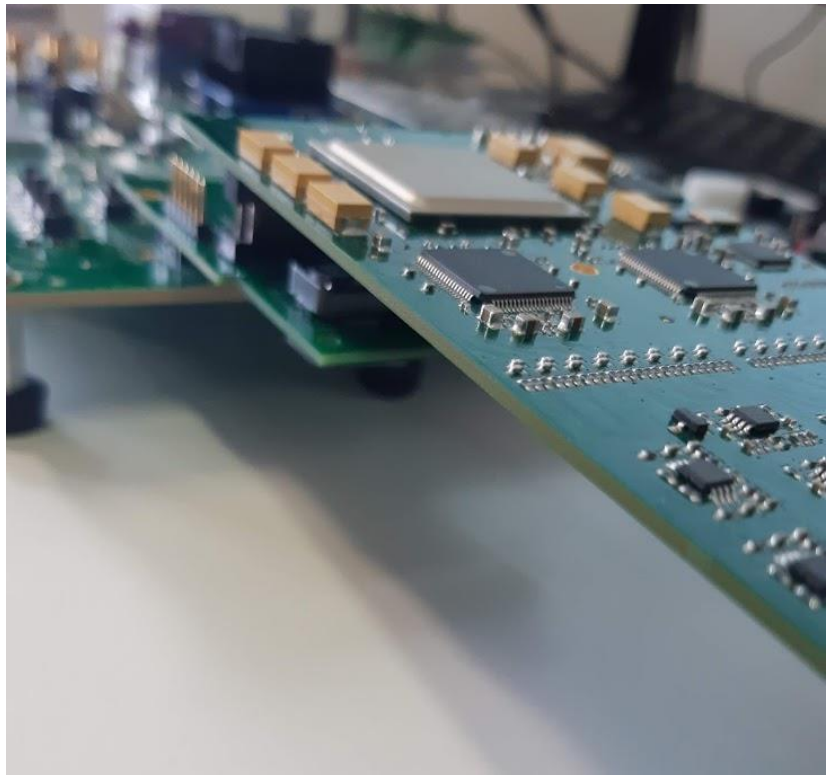
Readout system, two DAQ approaches



- MSADC
  - Two independent channels, continuos data stream
  - Sixteen channels fixed 4k data, triggered events
- Carrier Design
  - Two channels MSADC hardware handler and packet builder
  - Sixteen channels trigger handler
- Python Scripts
  - 2 channels design, packet length, source mode and channel selection options are available
  - 16 channels, trigger mode, source mode and pre-trigger time options are available
- Adapter and Power board
  - 9V @ 3A power input
  - Full QSH-90 to FMC signals mapping
  - All four power domains to feed MSADC (only one 3.3V domain)

System design for 2Ch (selectable) MSADC output data stream

MSADC Requirements

- Up to 40 MHz clock input
- System reset signal
- Two independent channels streamers
- Individual channel selection signals

Carrier Design (Firmware/Hardware)

- Programmable frequency clock output
- System reset generator
- Multi-platform design
- Online programmable data length packets

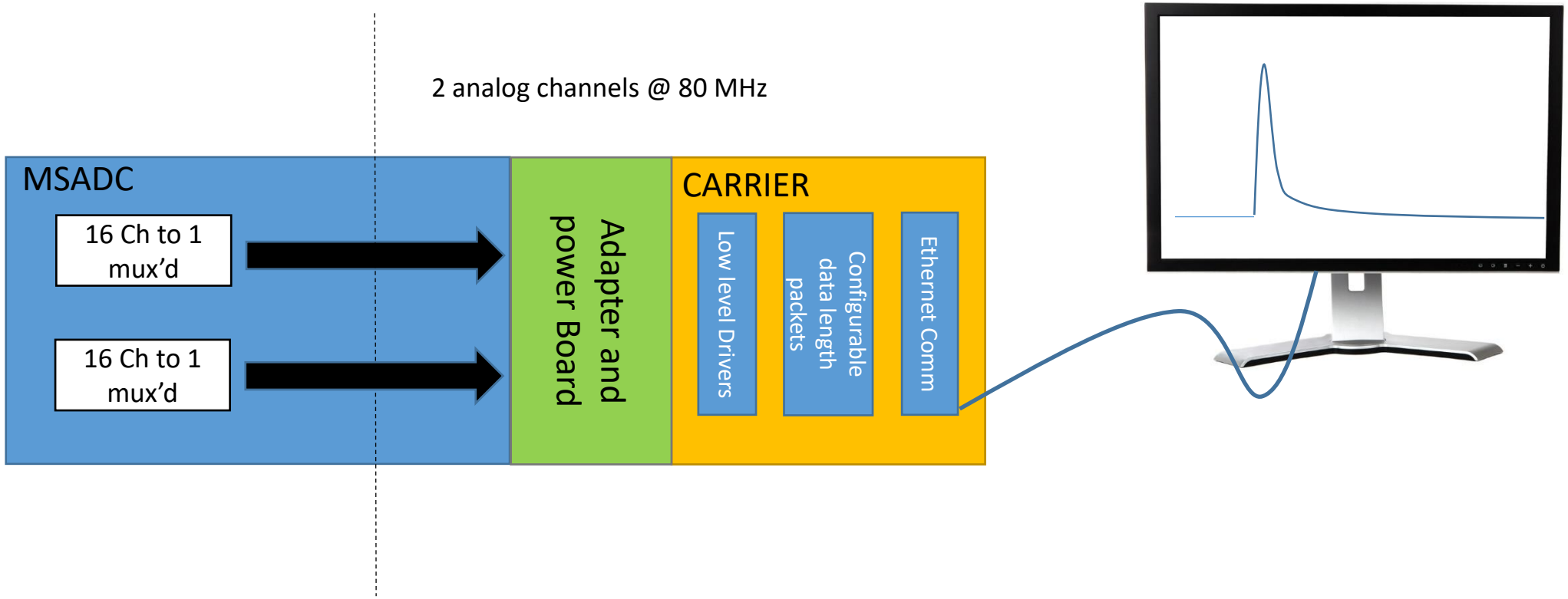
MSADC to Carrier Interface Characteristics

- 12 bits data width
- 80MHz data rate
- Data valid signaling
- 12 LVDS DDR Data transmission lines

PC Software Interface

- Up to 4 Million data points retrieval
- Channel selection
- Configurable Ethernet communication parameters

MSADC system design for 2Ch



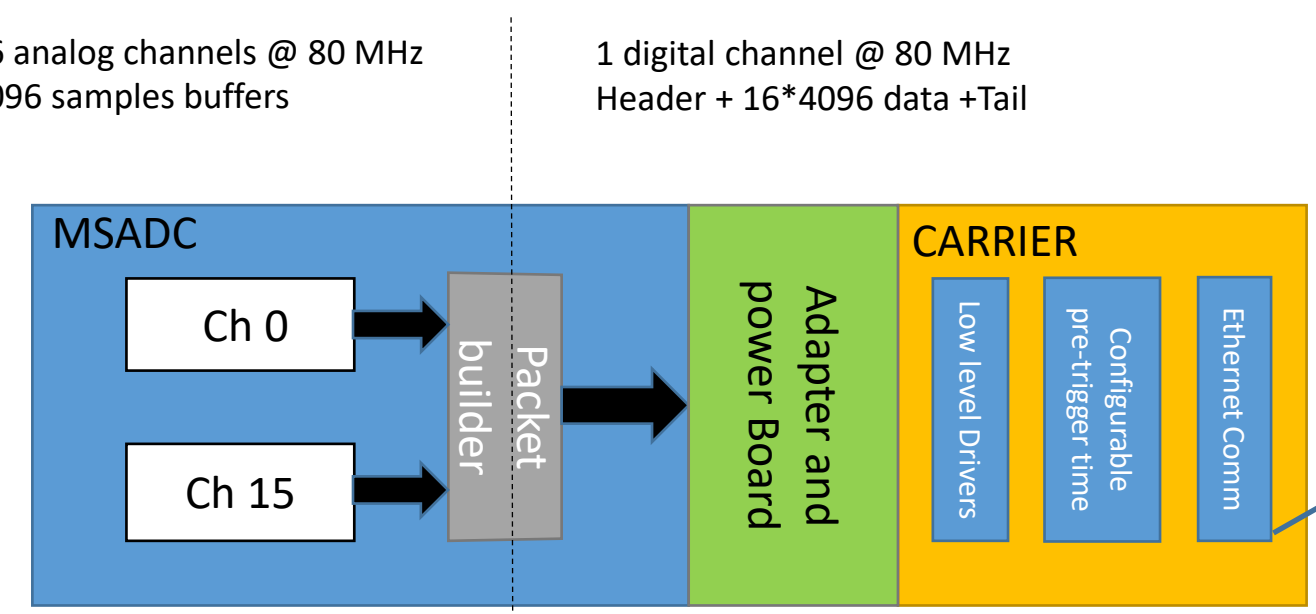
MSADC -- Readout system for 16 channels

- Selectable trigger depth on runtime
- Selectable trigger source (software/external)
- 16 Channels @ 80MHz – 4096 samples per channel
- Ethernet communication to transmit the data stream
- Personal Computer interface to retrieve the data when desired
- Test suite in hardware to verify the correct working of the entire system
- Portable design, implemented in the zedboard but can be easily ported to any zynq7000 based board.

MSADC Firmware Modifications and Carrier Board development

16 analog channels @ 80 MHz
4096 samples buffers

1 digital channel @ 80 MHz
Header + 16*4096 data +Tail



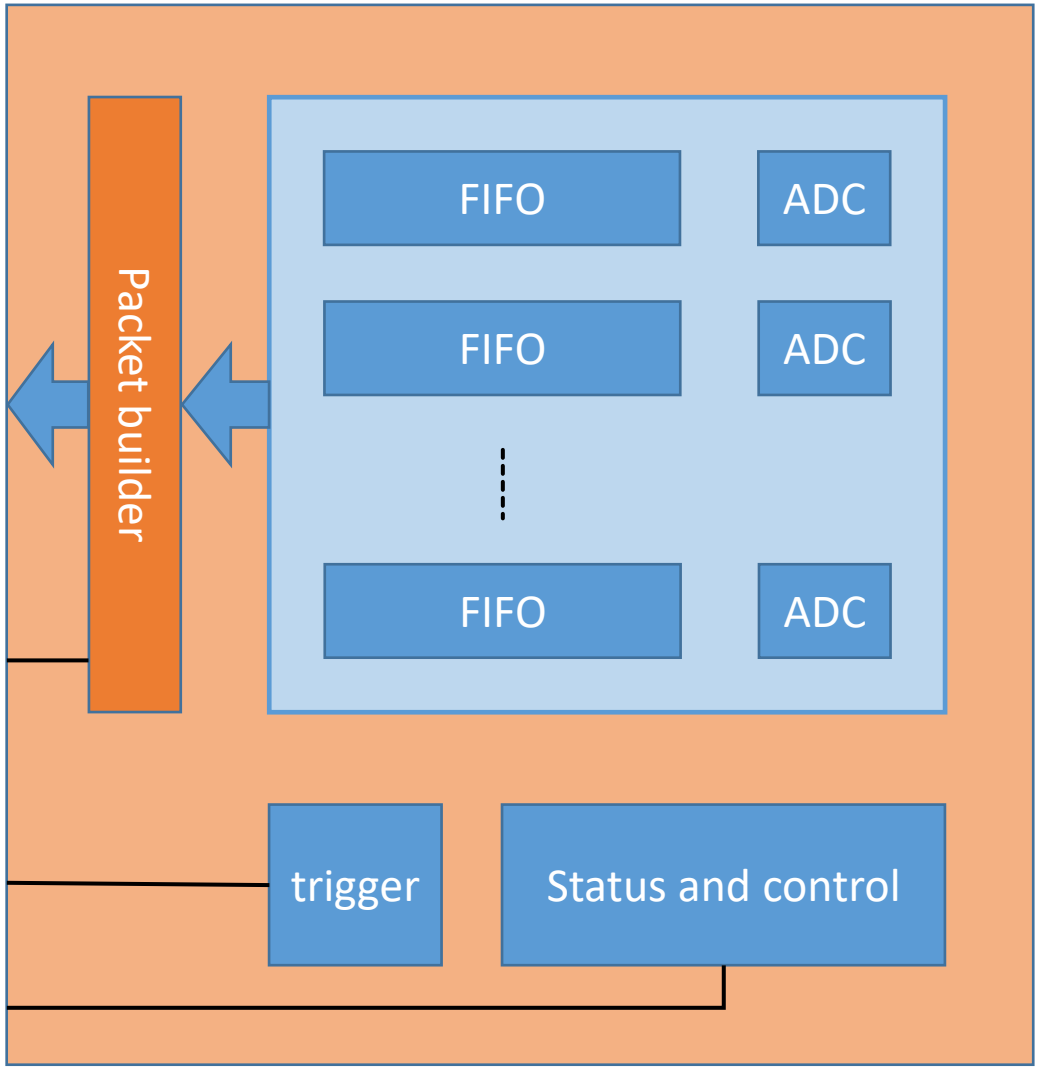
Modifications, Test beam in Mainz and proton radius measurement

MSADC Triggered and buffered data approach

- 16 channels readout system
- 4096 continuous stream per channel
- External triggering
- Interleaved channels stream mode
- 12 LVDS DDR Data transmission lines

Future work

- Selectable data lenght per channel
- Channel interleaved or atomic transmission packets
- Continuous stream readout system
- Need of some loseless data compression method
- Study of maximum number of channels
- Data transmission needs and capabilities study, theoretical and practical



I/O Data rate using the SERDES blocks (theoretical)

Data transmission capabilities are not enough

- 16 available LVDS lines (Total 20, 2 used for clocks, 2 for MCU I2C)
- Max data rate specification is 800 Mb/s
- Total transmission capability could be 16 * 800 Mb/s = **12800 Mb/s**
- Each ADC produces 12bit x 80 Msps = 960 Mb/s
- Total transmission needs, 16 * 960 Mb/s = **15360 Mb/s**

- Theoretical speed ratio: 83,3%

Git repositories

- MSADC Firmware Project
  - https://gitlab.com/brunovali/msadc_muxd_single_ch/
- MSADC to Carrier Adapter Board
  - https://gitlab.com/brunovali/msadc_interposer
- Carrier design and PC Software
  - https://gitlab.com/brunovali/mainz_ciaa_msadc