The Abdus Salam
International Centre
for Theoretical Physics

Multidisciplinary Laboratory

MPSoC Ultrascale + Analysis

Advantages of an embedded processor

Smaller footprint and space requirements

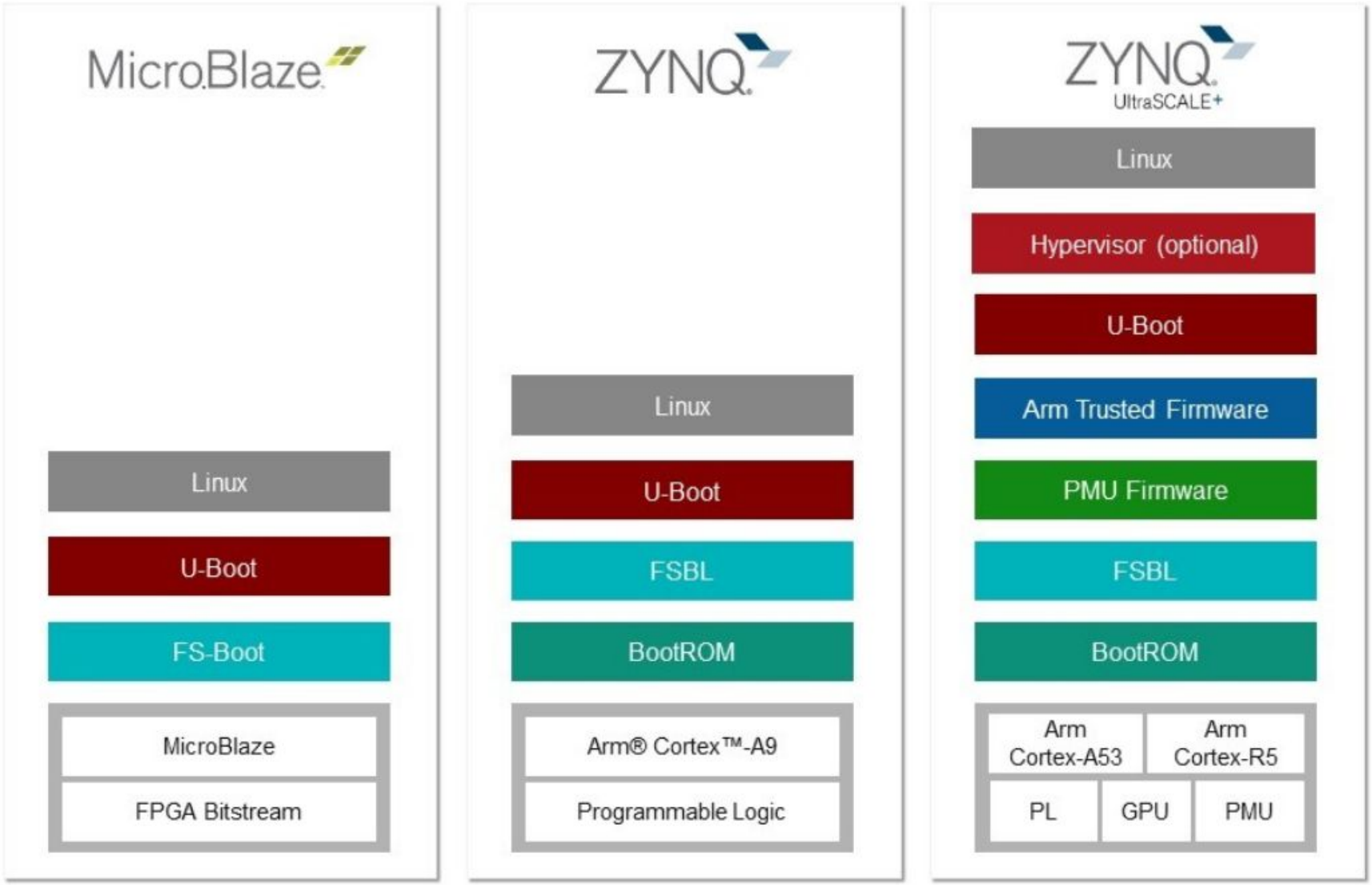
Robust communication between the FPGA and the processor.

Provides assistance for relatively slow online calculations (calibration, thresholds, coefficients, etc).

The implementation of an OS provides network communication tools ideal for slow control activities (parameters, status reports, etc).

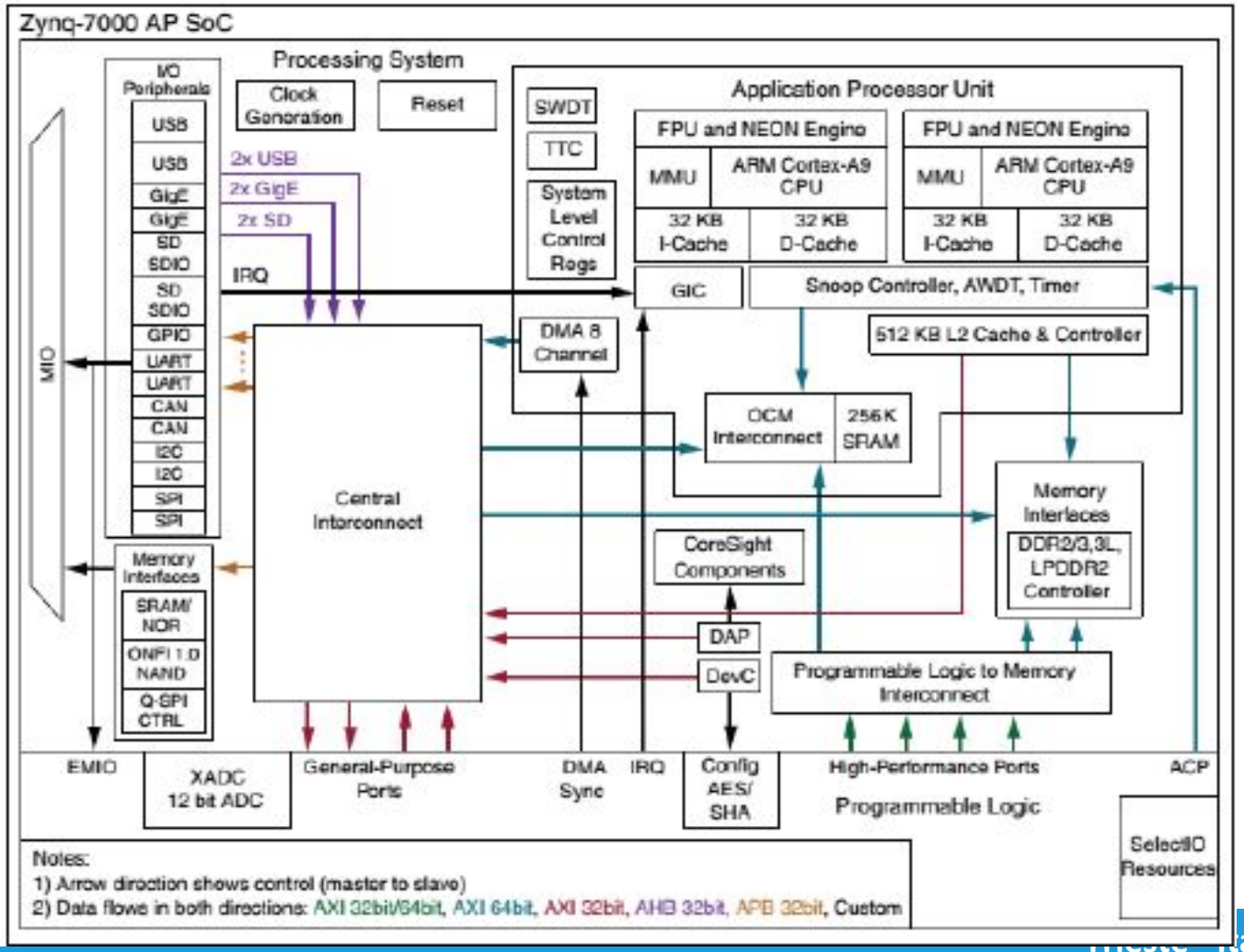
FPGA manager provides an interface for loading a bitstream.

Supports multiple bitstreams for the same PS and corresponding device tree overlay (dtbo) Ideal for interspill configurations.



Platform Management Unit (PMU). The PMU controls the power-up, reset, and monitoring of resources within the system.

Zynq vs Zynq Ultrascale +



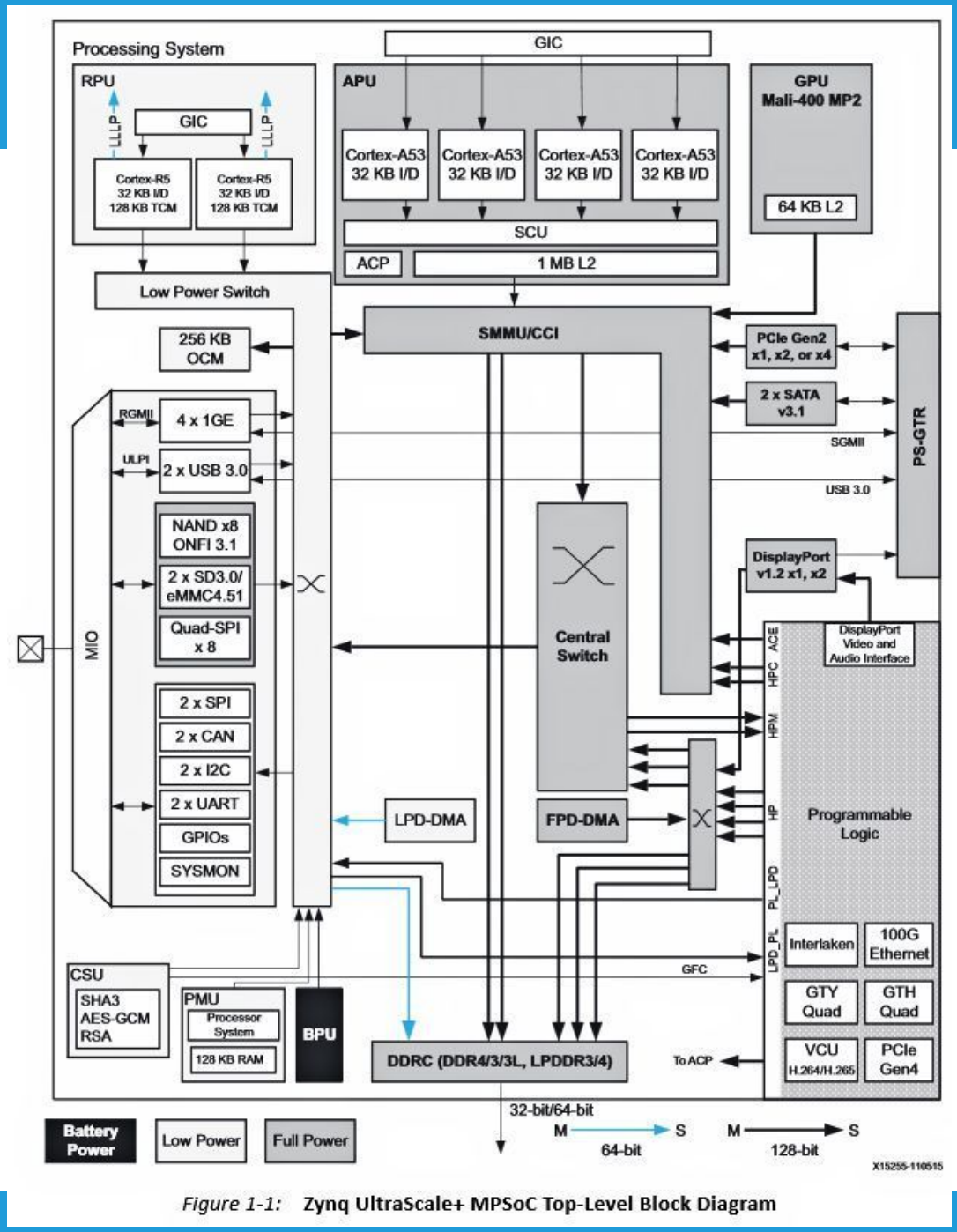


Figure 1-1: **Zynq UltraScale+ MPSoC Top-Level Block Diagram**

Arm Cortex-A53 Based Application Processing Unit (APU)

Quad-core Armv8-A Architecture
o 64-bit or 32-bit operating modes

CPU frequency: Up to 1.5GHz

Single/double precision Floating Point Unit (FPU)

Dual-core Arm Cortex-R5 Based Real-Time Processing Unit (RPU)

CPU frequency: Up to 600MHz

Armv7-R Architecture Dual-core processor.

On-Chip Memory

256KB on-chip RAM (OCM) in PS with ECC

Up to 36Mb on-chip RAM (UltraRAM) with ECC in PL

Up to 35Mb on-chip RAM (block RAM) with ECC in PL

Up to 11Mb on-chip RAM (distributed RAM) in PL

Two DMA controllers of 8-channels each supporting

Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and scatter-gather transaction support Serial Transceivers

Four dedicated PS-GTR receivers and transmitters supports up to 6.0Gb/s data rates o Supports SGMII tri-speed Ethernet, PCI Express® Gen2, Serial-ATA (SATA), USB3.0, and DisplayPort.

Open Asymmetric Multi-processing (OpenAMP) for software applications between processors (in MPSoC Ultrascale +)

	ZU2EG	ZU3EG	ZU4EG	ZU5EG	ZU6EG	ZU7EG	ZU9EG	ZU11EG	ZU15EG	ZU17EG	ZU19EG
Application Processing Unit	Quad-core Arm Cortex-A53 MPCore with CoreSight; NEON & Single/Double Precision Floating Point; 32KB/32KB L1 Cache, 1MB L2 Cache										
Real-Time Processing Unit	Dual-core Arm Cortex-R5 with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Cache, and TCM										
Embedded and External Memory	256KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3; External Quad-SPI; NAND; eMMC										
General Connectivity	214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; WatchDog Timers; Triple Timer Counters										
High-Speed Connectivity	4 PS-GTR; PCIe Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII										
Graphic Processing Unit	Arm Mali™-400 MP2; 64KB L2 Cache										
System Logic Cells	103,320	154,350	192,150	256,200	469,446	504,000	599,550	653,100	746,550	926,194	1,143,450
CLB Flip-Flops	94,464	141,120	175,680	234,240	429,208	460,800	548,160	597,120	682,560	846,806	1,045,440
CLB LUTs	47,232	70,560	87,840	117,120	214,604	230,400	274,080	298,560	341,280	423,403	522,720
Distributed RAM (Mb)	1.2	1.8	2.6	3.5	6.9	6.2	8.8	9.1	11.3	8.0	9.8
Block RAM Blocks	150	216	128	144	714	312	912	600	744	796	984
Block RAM (Mb)	5.3	7.6	4.5	5.1	25.1	11.0	32.1	21.1	26.2	28.0	34.6
UltraRAM Blocks	0	0	48	64	0	96	0	80	112	102	128
UltraRAM (Mb)	0	0	13.5	18.0	0	27.0	0	22.5	31.5	28.7	36.0
DSP Slices	240	360	728	1,248	1,973	1,728	2,520	2,928	3,528	1,590	1,968
CMTs	3	3	4	4	4	8	4	8	4	11	11
Max. HP I/O(1)	156	156	156	156	208	416	208	416	208	572	572
Max. HD I/O(2)	96	96	96	96	120	48	120	96	120	96	96
System Monitor	2	2	2	2	2	2	2	2	2	2	2
GTH Transceiver 16.3Gb/s(3)	0	0	16	16	24	24	24	32	24	44	44
GTY Transceivers 32.75Gb/s	0	0	0	0	0	0	0	16	0	28	28
Transceiver Fractional PLLs	0	0	8	8	12	12	12	24	12	36	36
PCIe Gen3 x16	0	0	2	2	0	2	0	4	0	4	5
150G Interlaken	0	0	0	0	0	0	0	1	0	2	4
100G Ethernet w/ RS-FEC	0	0	0	0	0	0	0	2	0	2	4

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System Monitor	2	2	2	2	2	2	2	2	2	2	2
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Transceiver Fractional PLLs	0	0	8	8	12	12	12	24	12	36	36
PCIe Gen3 x16	0	0	2	2	0	2	0	4	0	4	5
150G Interlaken	0	0	0	0	0	0	0	1	0	2	4
100G Ethernet w/ RS-FEC	0	0	0	0	0	0	0	2	0	2	4

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System Monitor	2	2	2	2	2	2	2	2	2	2	2
GTH Transceiver 16.3Gb/s(3)	0	0	16	16	24	24	24	32	24	44	44
GTY Transceivers 32.75Gb/s	0	0	0	0	0	0	0	16	0	28	28
Transceiver Fractional PLLs	0	0	8	8	12	12	12	24	12	36	36
PCIe Gen3 x16	0	0	2	2	0	2	0	4	0	4	5
150G Interlaken	0	0	0	0	0	0	0	1	0	2	4
100G Ethernet w/ RS-FEC	0	0	0	0	0	0	0	2	0	2	4

iW-RainboW-G35M ZU19EG Zynq UltraScale+ MPSoC System On Module

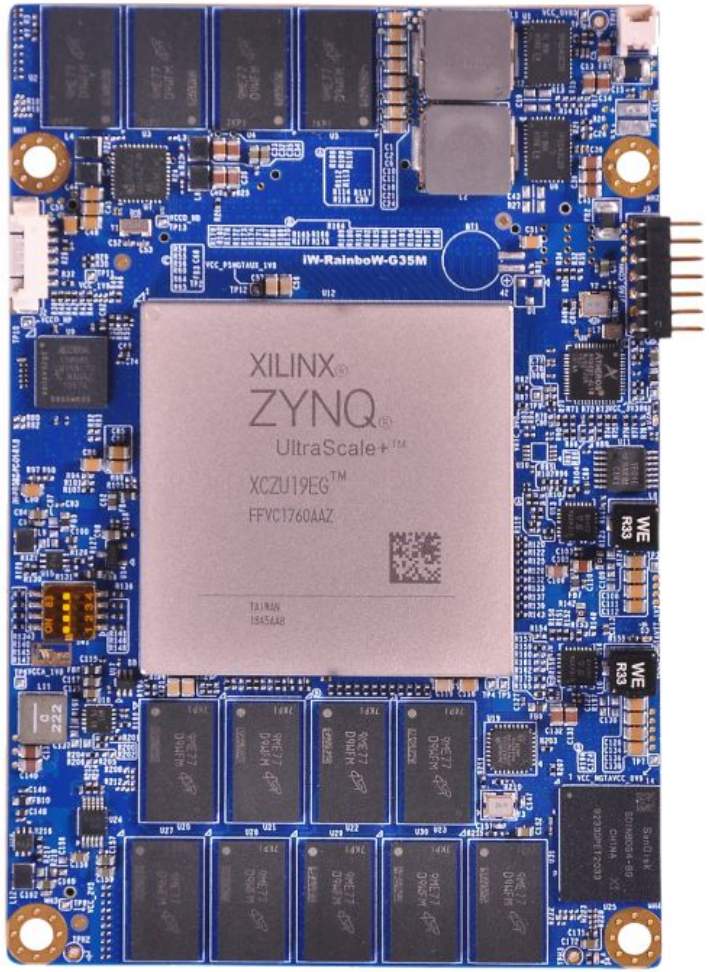
Zynq UltraScale+ MPSoC PL Interfaces:

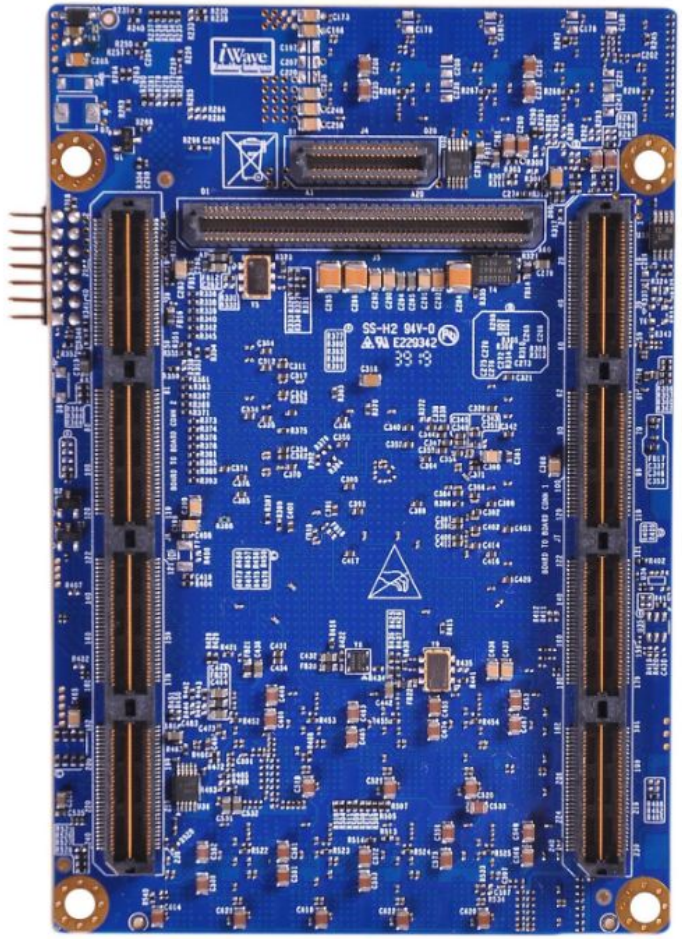
32 x High Speed transceivers @ 16.3Gbps

16 x High Speed transceivers @ 32.75Gbps

48 LVDS Pairs/96 SE IOs/ 32 ADCs

46 SE IOs/ 16 ADCs

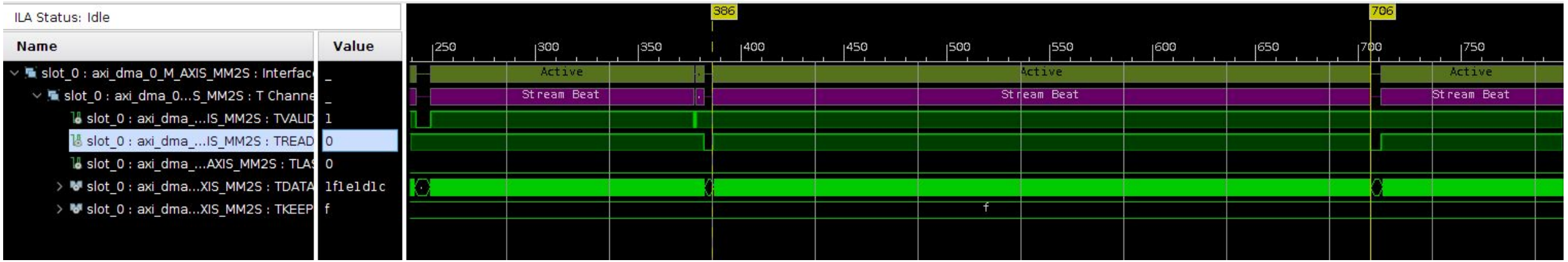


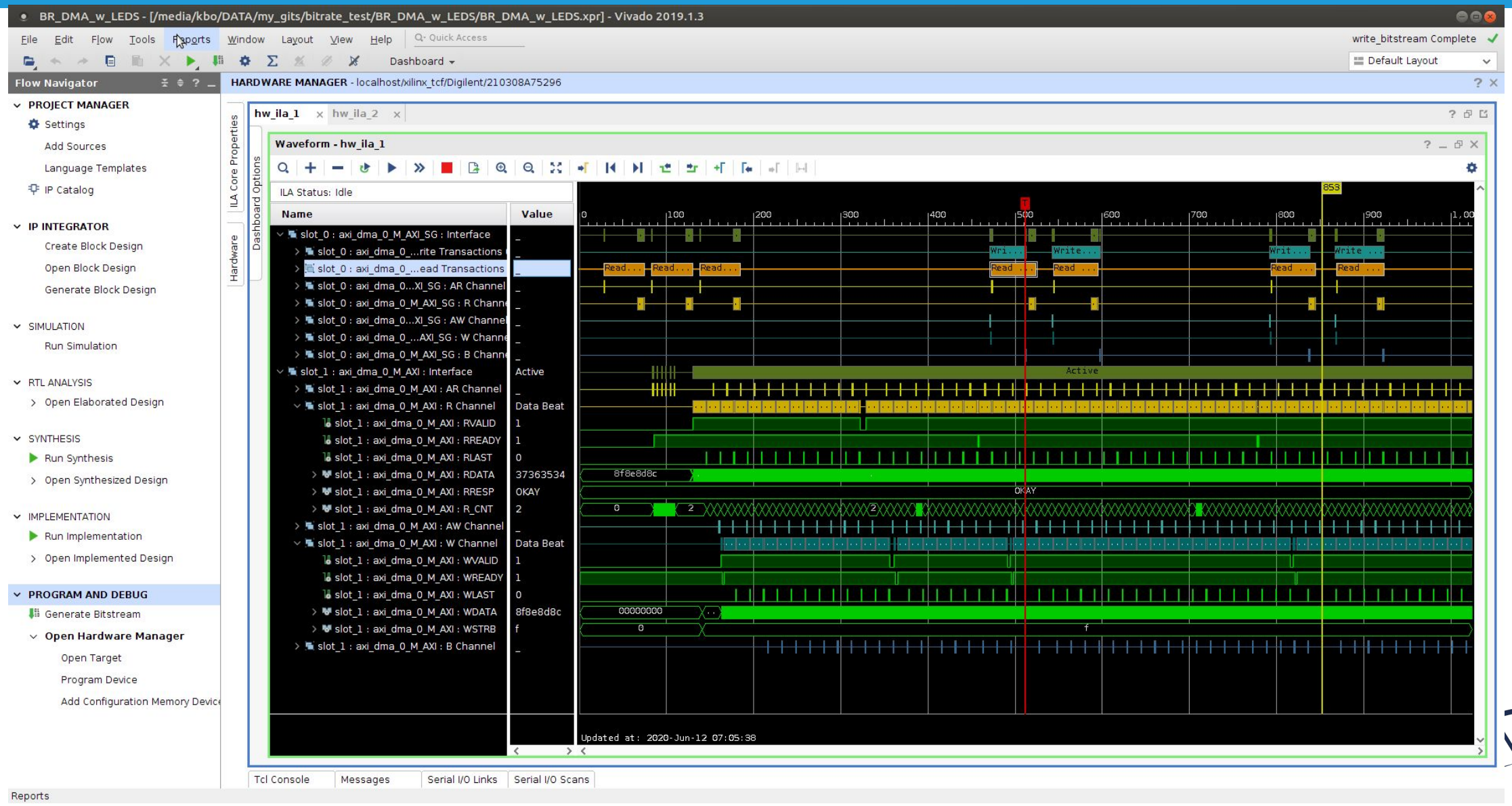


Tests and work in progress

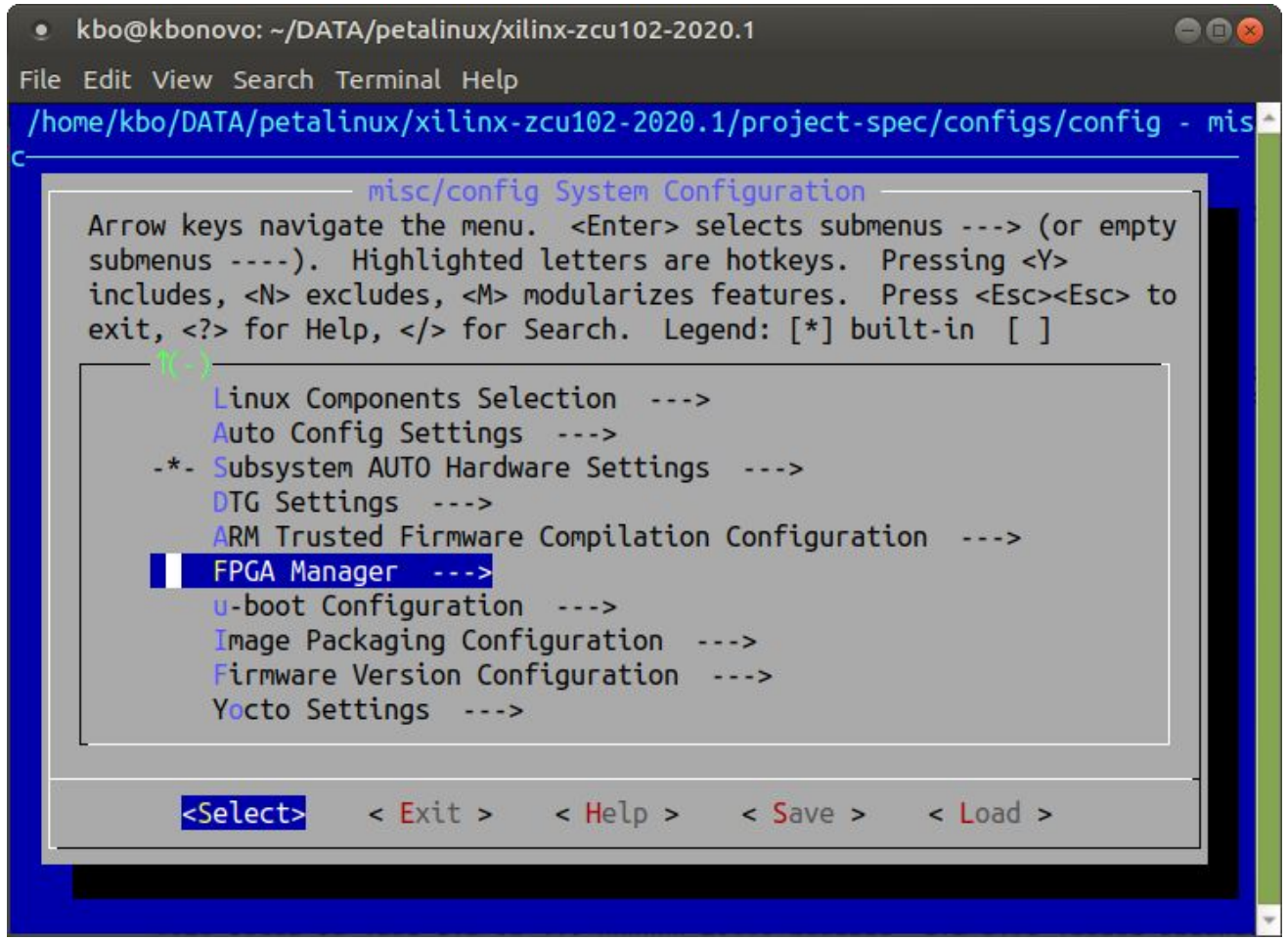
Scatter Gather DMA transfer

Deadtime between burst: 50 ns




BR_DMA_w_LEDS - [/media/kbo/DATA/my_gits/bitrate_test/BR_DMA_w_LEDS/BR_DMA_w_LEDS.xpr] - Vivado 2019.1.3
File Edit Flow Tools Reports Window Layout View Help
write_bitstream Complete
Dashboard
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
Open Target
Program Device
Add Configuration Memory Device
HARDWARE MANAGER - localhost/xilinx_tcf/Digilent/210308A75296
hw_ila_1
hw_ila_2
Waveform - hw_ila_1
ILA Status: Idle
Name
Value
slot_0 : axi_dma_0_M_AXI_SG : Interface
slot_1 : axi_dma_0_M_AXI : Interface
Active
slot_1 : axi_dma_0_M_AXI : R Channel
Data Beat
slot_1 : axi_dma_0_M_AXI : RVALID
slot_1 : axi_dma_0_M_AXI : RREADY
slot_1 : axi_dma_0_M_AXI : RLAST
slot_1 : axi_dma_0_M_AXI : RDATA
37363534
slot_1 : axi_dma_0_M_AXI : RRESP
OKAY
slot_1 : axi_dma_0_M_AXI : R_CNT
slot_1 : axi_dma_0_M_AXI : W Channel
slot_1 : axi_dma_0_M_AXI : WVALID
slot_1 : axi_dma_0_M_AXI : WREADY
slot_1 : axi_dma_0_M_AXI : WLAST
slot_1 : axi_dma_0_M_AXI : WDATA
8f8e8d8c
slot_1 : axi_dma_0_M_AXI : WSTRB
slot_1 : axi_dma_0_M_AXI : B Channel
Updated at: 2020-Jun-12 07:05:38
Tcl Console
Messages
Serial I/O Links
Serial I/O Scans
Reports

Linux environment setup



GtkTerm - /dev/ttyUSB0 115200-8-N-1

File Edit Log Configuration Control signals View Help

```
root@ubuntu:~# cp Carr_wrapper.bin /lib/firmware/
root@ubuntu:~# ls /sys/class/fpga_manager/fpga0
device    flags  key    of_node  state      uevent
firmware  iv     name   power    subsystem
root@ubuntu:~# ls /lib/firmware/
Carr_wrapper.bin  al5d.fw  al5d_b.fw  al5e.fw  al5e_b.fw
root@ubuntu:~# echo Carr_wrapper.bin > /sys/class/fpga_manager/fpga0/firmware
root@ubuntu:~# ls /dev/
autofs              ptyaa  ptyq3  ptyvc   snd     ttyae  ttyq7  ttyw0
block               ptyab  ptyq4  ptyvd   stderr  ttyaf  ttyq8  ttyw1
btrfs-control       ptyac  ptyq5  ptyve   stdin   ttyb0  ttyq9  ttyw2
bus                 ptyad  ptyq6  ptyvf   stdout  ttyb1  ttyqa  ttyw3
char                ptyae  ptyq7  ptyw0   tty     ttyb2  ttyqb  ttyw4
console             ptyaf  ptyq8  ptyw1   tty0    ttyb3  ttyqc  ttyw5
cpu_dma_latency     ptyb0  ptyq9  ptyw2   tty1    ttyb4  ttyqd  ttyw6
disk                ptyb1  ptyqa  ptyw3   tty10   ttyb5  ttyqe  ttyw7
dri                 ptyb2  ptyqb  ptyw4   tty11   ttyb6  ttyqf  ttyw8
fd                  ptyb3  ptyqc  ptyw5   tty12   ttyb7  ttyr0  ttyw9
full                ptyb4  ptyqd  ptyw6   tty13   ttyb8  ttyr1  ttywa
gpiochip0           ptyb5  ptyqe  ptyw7   tty14   ttyb9  ttyr2  ttywb
gpiochip1           ptyb6  ptyqf  ptyw8   tty15   ttyba  ttyr3  ttywc
gpiochip2           ptyb7  ptyr0  ptyw9   tty16   ttybb  ttyr4  ttywd
hugepages           ptyb8  ptyr1  ptywa   tty17   ttybc  ttyr5  ttywe
i2c-0               ptyb9  ptyr2  ptywb   tty18   ttybd  ttyr6  ttywf
i2c-1               ptyba  ptyr3  ptywc   tty19   ttybe  ttyr7  ttyx0
i2c-10              ptybb  ptyr4  ptywd   tty2    ttybf  ttyr8  ttyx1
i2c-11              ptybc  ptyr5  ptywe   tty20   ttyc0  ttyr9  ttyx2
```

/dev/ttyUSB0 115200-8-N-1 DTR RTS CTS CD DSR RI

Next steps

Full integration with MSADC

Dual MSADC test (ZCU102)

Multichannel DMA for data transmission.

Maximum data rate through Ethernet.

Performance comparison between APU and RPU